A Defuzzification scheme suitable for digital hardware implementation

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Abstract: This paper presents a practical approach for defuzzification in digital hardware based fuzzy inference systems . The proposed scheme is a modified version of the center average defuzzifier where instead of using a division stage a piece-wise linear function is implemented to reduce computational time and hardware implementation area. Some simulation probes are presented in order to compare the natural and modified defuzzifier in a fuzzy logic controller operating into a non-linear control system.

Key-Words: - Fuzzy Hardware , Defuzzifiers, Defuzzification , Fuzzy controllers , Fuzzy logic .

1. Introduction

One of the most critical parameters in Fuzzy inference systems is the defuzzification method when they are going to be implemented using digital hardware. Today, Center average defuzzifier has become in the most popular defuzzification scheme in practical applications because of its simple computational structure but its division stage increases the effective hardware implementation area and the propagation delay in combinational realizations. This work presents a modified version of the center average defuzzifier suitable for digital hardware implementation like FPGAs or Standard Cells.

The proposed scheme uses an approximation of the division operation using a piece-wise linear function. The first approach takes particular points of the non-linear division function in order to generate several linear combinations with their respective ranges. This defuzzification scheme has been probed as part of a fuzzy logic controller applied to the inverted pendulum balancing , the experiments show better results using the proposed scheme.

A constrain is introduced into the modified scheme, the coefficients of the linear combinations are replaced with fixed two's power numbers. According to some digital circuit principles , a multiplication by a two's power number can be viewed as a simple left shift then the necessary logic resources for implementing this function will be smaller than the required by a natural multiplication operation. this new approach is also probed with the same FLC getting some interesting results.

2. Modified center average defuzzifier

The commonly used center average defuzzifier is presented in (1) where y is the a center average , x the center of the $l'th$ fuzzy set and w its height .This defuzzification scheme is computationally simple and intuitively plausible [1] . Also small changes in its parameters will produce small changes in its output.

$$y = \frac{\sum_{l=1}^{N} x_l w_l}{\sum_{l=1}^{N} w_l} \qquad (1)$$

Fig. 1 Shows a graphical representation of the scheme with M=2.

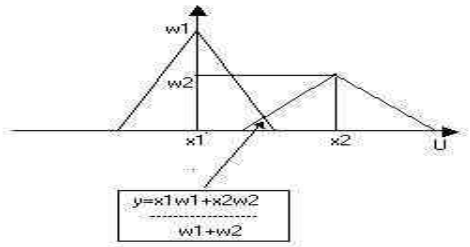


Fig. 1 Graphical representation of the center average defuzzifier

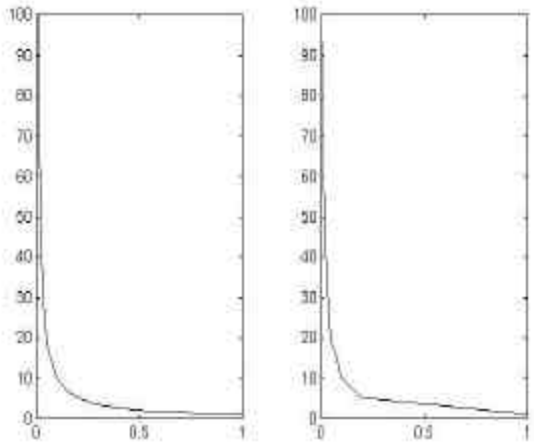
It is clear that y can be observed in (2) as the product of two functions and one of them has a non linear behavior.

$$\left(\begin{array}{l} y = \left(\sum_{l=1}^{M} x_l w_l \right) f(k) \\ f(k) = \dfrac{1}{k} \\ k = \sum_{l=1}^{M} w_l \end{array} \right) \qquad (2)$$

It is possible to make an approximation of *f(k)* expressing it as a set of linear combinations with defined ranges These linear combinations are simple functions of the form *y=mx+b* where the parameters *m* and *b* are computed taking into account particular values of *f(k)*. The approximation function *g(k)* is presented in (3).

$$\left(\begin{array}{l} g(k) = \begin{cases} m_1 k + b_1 & 0 < k \le k_1 \\ m_2 k + b_2 & k_1 < k \le k_2 \\ \vdots & \\ m_n k + b_n & k_{n-1} < k \le k_n \end{cases} \\ \\ m_n = \dfrac{f(k_n) - f(k_{n-1})}{k_n - k_{n-1}} \\ b_n = f(k_{n-1}) - m_n k_n \end{array} \right) \qquad (3)$$

A graphical interpretation of *g(k)* is presented in Fig 2b with a set of five linear functions, a bigger set will provide a better approximation for *f(k)*.



(a) *(b)*

Fig.2 (a) Graphical representation of f(k)
(b) Graphical representation of g(k)

3. Probe in a Fuzzy Logic Controller.

A FLC for balancing the inverted pendulum was implemented in order to probe the proposed defuzzification scheme and compare it with the center average defuzzifier.

The FLC is constructed using a classical approach [2] where the angular position *ap* and the angular velocity *av* of the inverted pendulum will be the input variables and the actuating force *af* will be the output variable of the FLC.A set of four fuzzy IF-THEN rules is used :

IF ap is positive and av is positive THEN af is negative (4)
IF ap is positive and av is negativeTHEN af is zero (5)
IF ap is negative and av is positive THEN af is zero (6)
IF ap is negative and av is negative THEN af is positive (7)

Where the fuzzy sets “positive “ and “negative” are presented in Fig. 3. In the other hand “ negative big “ , “ zero” and “ positive big “ are three singletons in –1 , 0 and 1 respectively . The scaling of discourse universes is between +100% and –100%.

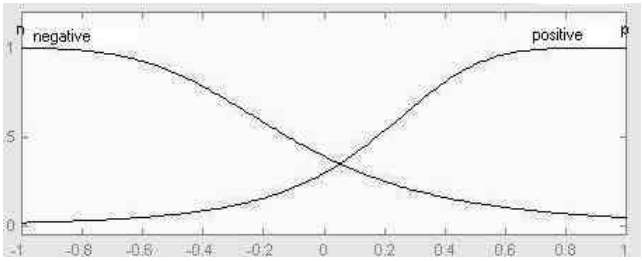


Fig. 3 Membership functions representing “negative” and “positive” fuzzy sets.

The FLC uses minimum inference engine, maximum aggregation and the proposed defuzzification scheme with the approximation function (8) :

$$g(k) = \begin{cases} -2500k + 100 & 0 < k \le 0.025 \\ -800k + 60 & 0.025 < k \le 0.05 \\ -200k + 30 & 0.05 < k \le 0.1 \\ -50k + 15 & 0.1 < k \le 0.2 \\ -0.5k + 5.1 & k > 0.2 \end{cases} \qquad (8)$$

Network representation [3] of the FLC is presented in Fig. 4, *u(k)* represents *f(k)=1/k* in the center average defuzzifier or *g(k)* in the proposed scheme.

4 Simulation Results

Three comparative results are presented , the angular position is measured in degrees and the control system model has the following parameters : Pole mass = 0.1Kg , Pole length = 0.5m , Cart mass = 1Kg , Acceleration due to gravity = 9.8m/s^{2}and an actuator with gain of 5N/100%. Fig. 5 shows some transient responses of the control system using the FLC with center average defuzzifier (Fig.

5a) and the FLC with the proposed defuzzification scheme (Fig 5b). The second FLC presents a better behavior in establishment time and its work range is greater than the range of the first FLC.

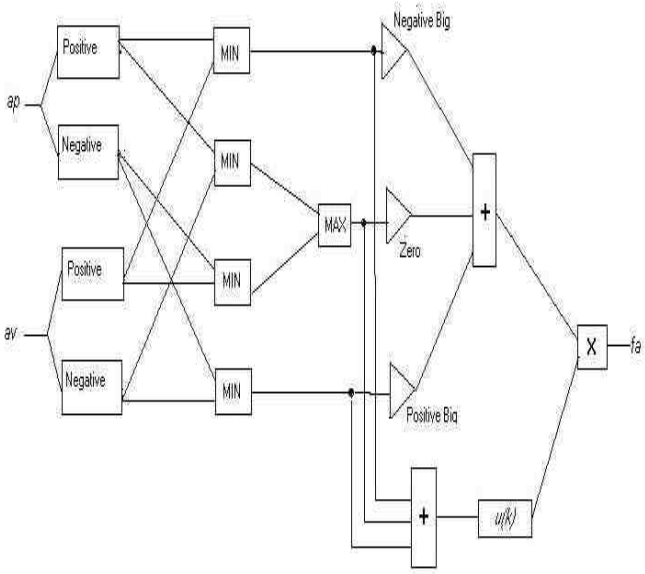
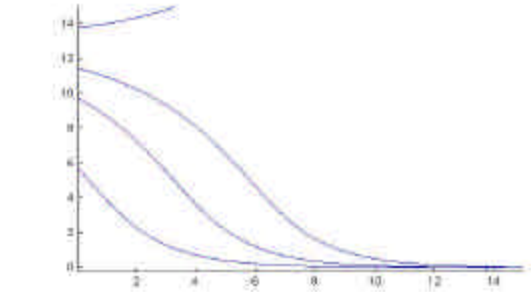
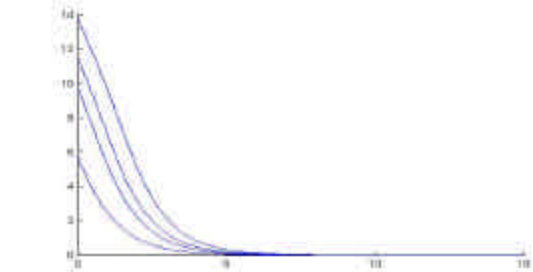


Fig 4. Network representation of the Fuzzy logic controller.

The control actions of the second FLC are greater at the beginning because of the excitation function *g(k)* then the controller can balance the pendulum faster avoiding instability. Controller output in the two cases is showed in Fig 6 with an initial condition $ap=11.5^{\circ}$.



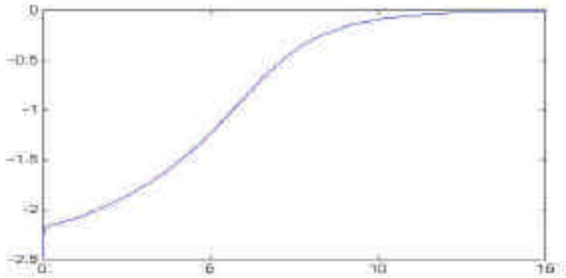
(a)



(b)

Fig 5.Transient responses. (a) FLC with center average defuzzifier . (b) FLC with the proposed defuzzification scheme.

The proposed defuzzification scheme increases the operative range of the FLC working with the same actuator, the upper limit is located at $ap= 45.83^{\circ}$.Fig 7 presents some probes in the common critical zone operation $ap>24^{\circ}$.



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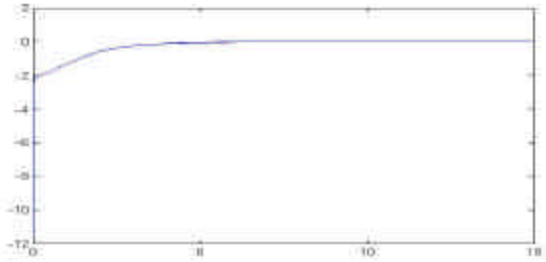


(b)

Fig 6. Controller output, Initial condition ap=11.8° . (a) FLC with center average defuzzifier (b) FLC with the proposed defuzzification scheme.

5 Digital hardware implementation .

Digital hardware realization of *g(k)* is presented in Fig 8a. The implementation uses a comparator-decoder module to get the respective range of the input digital signal *k* , this operation can be made with a total bit inspection or partial bit inspection of some significant bits.

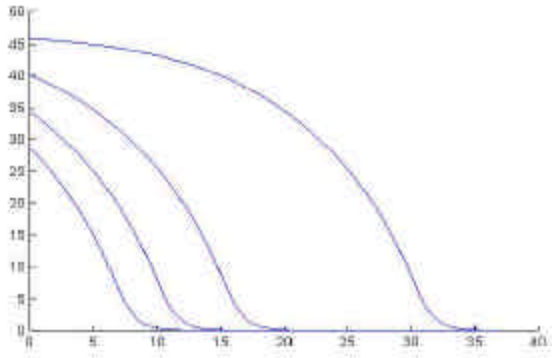
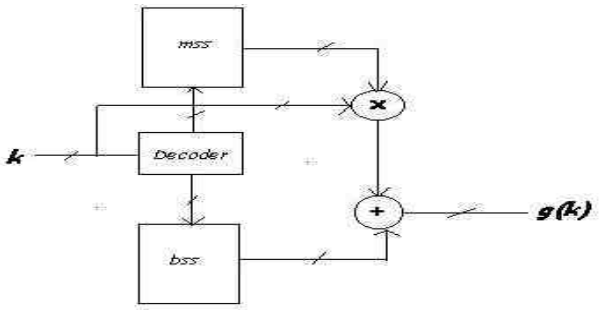
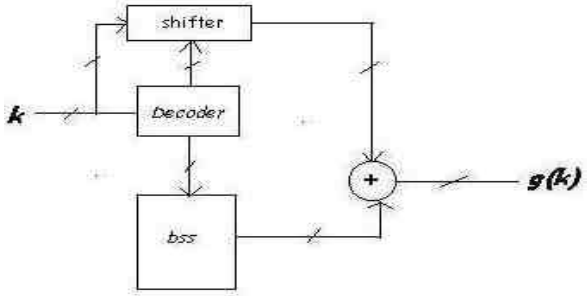


Fig 7. Obtained Transient responses in the critical zone ($ap >24^{o}$) using the proposed defuzzification scheme.

Decoder output works as the index of two storage systems, the first of them sets the value of m_n and the second the value of b_n. These systems can be register banks , RAM or ROM blocks. The output of the first storage system *mss* and the input signal *k* are multiplied (the multiplication operation can be made using a serial or parallel multiplicator) , the result of this operation is added to the present value *b* at the output of the second storage system *bss*.



(a)



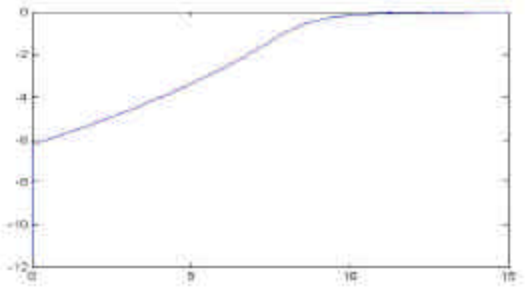
(b)

Fig 8. (a).Architecture of a natural g(k). (b) Hardware reduced g(k).

This implementation could be modified using a practical approach in order to optimize hardware resources , the modified scheme is presented in Fig 8b. The values of *m* can be fixed two's power numbers then the multiplication operation is transformed into a simple left or right shift. Using this principle the multiplicator and the first storage system *mss* are replaced by a combinational or sequential shifter that will require less logical circuits . The idea of using two's power number in the linear functions has been probed with the same FLC model ., the new *g(k)* is presented in (9) . This hardware reduced *g(k)* offers similar defuzzification results (controller output) that can be observed in Fig 9.

$$g(k) = \begin{cases} -4096\,k + 100 & 0 < k \le 0.025 \\ -1024\,k + 60 & 0.025 < k \le 0.05 \\ -512\,k + 30 & 0.05 < k \le 0.1 \\ -64\,k + 15 & 0.1 < k \le 0.2 \\ -0.5k + 5.1 & k > 0.2 \end{cases} \quad (9)$$

Real work operation probe of the proposed defuzzification scheme is still in progress.



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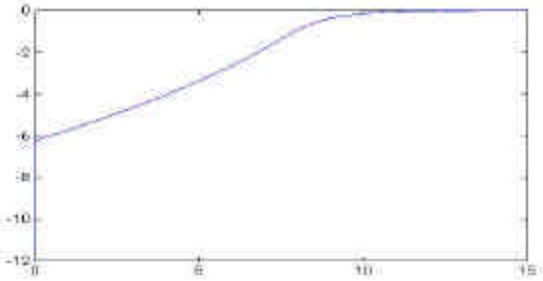

(b)

Fig 9.(a) FLC output with the natural g(k) . (b) FLC output with the hardware reduced g(k). Initial condition of the inverted pendulum 30^0

The natural and hardware reduced *g(k)* have been specified using VHDL (VHSIC Hardware Description Language) [4] and probed under functional simulation. As a prototyping platform a Xilinx® FPGA (Field Logic Programmable Gate Array) [5] is being used. Realization results show that defuzzification scheme based on a *g(k)* with five linear functions (16 bit precision) requires 80% of the logical resources used in a digital divider with the same word length. A hardware reduced *g(k)* like (9) with the architecture presented in Fig 9b is constructed using 30% of the hardware area required in the natural *g(k)* (8) due to the fact that shifters are constructed with simple digital structures.

6 Conclusions

A modified version of the center average defuzzifier was presented. The main objective of the modification was the reduction of hardware area cost which is achieved using practical principles of digital circuits.

A Fuzzy logic controller for the inverted pendulum problem was implemented in order to probe the proposed defuzzification scheme . Simulation results show better system responses and a greater operation range of the control system using this scheme.

It is necessary to probe the proposed scheme with other applications to validate its good behavior. The hardware reduced approach could be a good choice in practical applications like fuzzy navigation systems for autonomous robots and digital image stabilizers in video recorders where it is necessary the use of low logical size and energy consumption devices.

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