A Compact Carrier Quantization Model for Nanoscale MOSFETs Simulation

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Abstract: - Due to the advanced fabrication technology, the oxide thickness is now in the regime of 1.0 nm for nanoscale MOSFETs. The quantization effects and inversion charge density displacement away from the interface of oxide and silicon can not be neglected. The most accurate model for such problem is solving the Schrödinger-Poisson (SP) equations with proper boundary condition in 1D structure. However, for 2D device characteristics and circuit dynamics, solution of the SP equations encounters numerical difficulty and is not ready for practical applications. Various quantum correction models have been proposed for theoretical exploration and verification. In this paper we study the quantization effects and for the first time develop a corresponding charge analytical model in terms of oxide thickness and applied voltage for ultrathin oxide MOSFETs. Based on a comprehensive investigation of charge peak location, peak value, averaged charge displacement, and charge density, the successfully derived compact model accounting for the quantization effects enables fast and accurate characterization of the effective charge density in nanoscale MOSFETs. This new model has computational superiority and can be directly applied for nanoscale device and circuit simulation without solving the SP equations. Compared with the measured C-V data of an ultrathin N-MOSFET, our simulation results demonstrate the model accuracy.

Key-Words: - Compact Model, Quantum Mechanical Effects, Ultrathin Oxide, MOS Devices, C-V Curves

1 Introduction

Modern nanoscale CMOS devices is with gate length of sub-0.1 μm and operating at 0.8 - 1.0 V, so an oxide thickness of the order 1.0 - 3.0 nm is considered, which corresponds to three to five layers of silicon atoms. From theoretical modeling point of view, one of important issues is the inversion charge lowing and transconductance loss due to the quantization of carriers in the channel as well as polysilicon gate depletion effects. In the quantum mechanical model, the density of inversion charge peaks at around 0.8 – 1.0 nm below the silicon surface such that gate capacitance and inversion charge are both effectively reduced to those of an equivalent oxide a few angstroms thicker than the physical oxide. Thus, characterization is needed to account for these effects in the choice of design parameters, especially for future 90 – 70 nm MOS technology. Furthermore, many research groups and laboratories have already fabricated N-MOSFETs with gate lengths around 30 – 50 nm [1-5], showing that these feature sizes are feasible in the recent years. As MOSFET devices are further scaled into this nanoscale regime, it has become vital to include quantum mechanical effects when modeling device behavior. In this nanoscale regime, quantum effects significantly dominate carrier transport. Various quantum mechanical approaches to studying quantum effects for nanoscle devices have been developed [6-13], but most of them are quite complicated.

In general, there have been two approaches to the modeling of these quantum effects: (1) employing full quantum mechanical transport model [14] and (2) adding quantum corrections to the classical transport equations, such as the Van Dort, Hansch, Modified Local Density Approximation (MLDA), Density-Gradient (DG), and effective potential models [6-11,15-17]. These models have their own merits, but still have some limitations in studying the multi-dimensional nanoscale MOSFETs. In computational electronics, the development of sophisticated and efficient Technology CAD (TCAD) tool [18] provides engineers significant leverage in conducting research into new integrated circuits technologies. For the most of ultrathin oxide MOS devices, it has

been well known that the approach with SP equations is the best one because it fully includes the quantum mechanics in a consistent fashion. However, the numerical solution of the SP equations intrinsically is a coupled problem between the system of nonlinear algebraic equations and matrix eigenvalue problem. Moreover, they tend to be unattractive from an industrial point of view since even the most advanced industrial simulation tools currently used are typically still particle based.

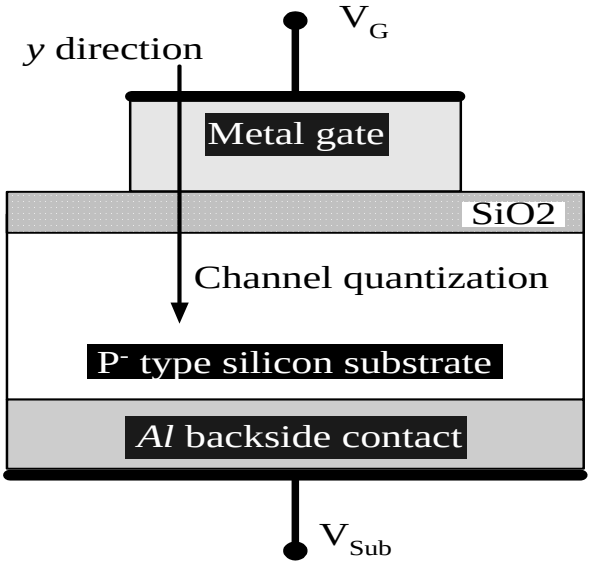

Fig. 1. A plot of 2D cross section for nanoscale N-MOS devices.

In this paper, we develop a novel carrier model for characterizing the nanoscale MOSFETs under inversion condition. This quantum correction model is ready for nanoscale MOSFETs device and circuit simulation without solving SP model or quantum correction differential equations. It can be extended for 2D device modeling simulation directly. Our approach to the compact model formulation is based on the exact numerical solution of the SP equations [16,17] and estimation of total charge density, average charge displacement, charge peak location, and peak value systematically. The generalized compact model has no any numerical difficult for incorporating into classical carrier transport models and has very good simulation results. The error for all results is controlled fewer than 5%. A detail comparison and test are presented in the paper. This paper is organized as follows. Sec. 2 states the novel compact charge model. Sec. 3 presents the characterization methodology. Sec. 4 reports and discusses the simulation and measurement for N-MOSFET devices. Sec. 5 draws the conclusions and suggests the future works.

2 Model Formulation

To compute the classical solution as a starting point, we first solve a MOS system as shown in Fig. 1 using the drift-diffusion (DD) approximation [2, 19-23]. The DD equation is then solved self-consistently with the SP equation. The SP equations (1-4) are assumed to have no wave penetration at the Si/SiO_2 interface. The details about the SP equations can be found, for instance [6-17]. It is discretized with the finite volume method; after the discretization we obtained the corresponding system of nonlinear algebraic equations and the matrix of eigenvalue problem. We iteratively solve the coupled problem to obtain the self-consistent solution. In each iteration loop, the discretized Schrödinger Equation leads to a matrix eigenvalue problem, and the corresponding eigenvalues and eigenvectors are then computed with a parallel divided and conquer algorithm together with the QR method [16,17]. Furthermore, the discretized nonlinear Poisson Equation is solved with the monotone iterative method instead of the Newton's Iterative method [19-23]. At least sixteen sub-bands are used in the Schrödinger equation solver, and various T_{ox} and V_G are applied.

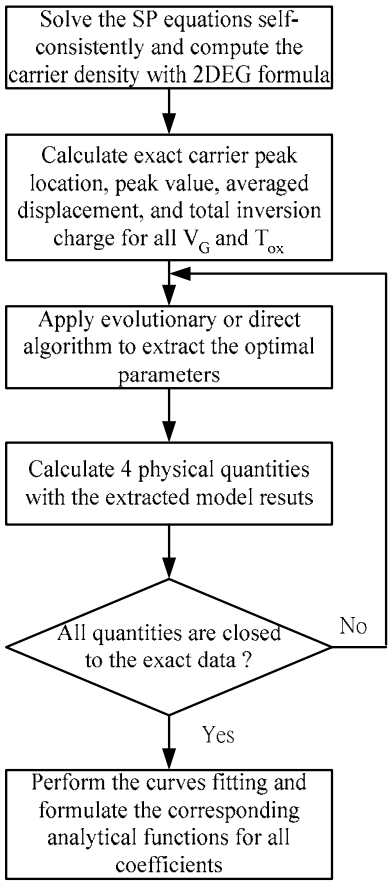

Fig. 2. An evolutionary procedure to extract the coefficients formula for the compact charge model for nanoscale N-MOS devices.

Fig. 2 shows the algorithm of extraction procedure to calculate the optimal parameters and the analytical expression for the coefficients [24]. The coefficients $a_0 - a_3$ are extracted subject to 4 different physical constraints.

$$-\frac{\hbar^2}{2}\frac{d}{dz}\frac{1}{m_{ni}^*(z)}\frac{d\Psi_{i,j}}{dz}+E(z)\Psi_{i,j}(z)=E_{i,j}\Psi_{i,j}(z) \quad (1)$$

$$\frac{d}{dz}(\varepsilon(z)\frac{d}{dz})\phi(z)=\frac{q}{\varepsilon_o}(n(\phi)-p(\phi)+N_A^-) \quad (2)$$

$$E(z)=-q\phi(z)+\Delta E_c(z) \quad (3)$$

$$n(\phi)=\frac{k_B T_L}{\pi\hbar^2}\sum_i g_i m_{di}^*\sum_j \ln[1+\exp(\frac{E_F-E_{i,j}}{k_B T_L})]\Psi_{i,j}^2(z) \quad (4)$$

With the proposed formulation procedure, the calculated inversion-layer charge densities are then cast into the form

$$n_{QM}=n_{CL}a_0[1-\exp(-a_1(\frac{x}{\lambda_{th}})^2+a_2(\frac{x}{\lambda_{th}})^4-a_3(\frac{x}{\lambda_{th}})^6)], \quad (5)$$

where n_{CL} is the classical electron density solved from the Poisson equation and $\lambda_{th}=(\frac{\hbar}{2m^* k_B T})^{1/2}$ is the thermal wavelength. As shown in Fig. 2, the optimal parameters a_0, a_1, a_2, and a_3 are calculated and calibrated from the SP equations for the proposed model. They are modeled as a function of V_G and T_{ox}. The fitting accuracy of the model to the data in terms of:

(i) the peak location,
(ii) the peak charge density,
(iii) the total inversion charge density, and
(iv) the average displacement from the interface

is within 5%. In our simulation, to evaluate stability of the model we define the averaged displacement <y> from the oxide-silicon interface.

$$< y >= \frac{\int_0 yn(y)dy}{\int_0 n(y)dy}, \quad (6)$$

where $n(y)$ is the quantum electron density in the bulk. Similarly, we define the total charge $Q(y)$ within the inversion layer, were

$$Q(y)=\int_0^{y_{inv}} -qn(y)dy, \quad (7)$$

where the y_{inv} is the interface point of the inversion layer. Four physical quantities are computed with the derived and SP models as the benchmarks for the coefficients extraction and model characterization.

3 Extraction and Simulation Results

In this section, we perform the extraction of the model coefficients, and the comparison between the proposed model and SP equations are also included. As shown in Figs. 3 – 6, we present the extracted coefficients for a_0, a_1, a_2, and a_3, respectively, versus applied gate voltage as well as various oxide thicknesses. Fig. 3a and 3b are the plots of the optimal extracted results for the coefficient a_0. Fig. 3a is the plot of a_0 versus the V_G, where the T_{ox} varies with 1.0, 1.3, 1.6, 2.2, and 3.0 nm, respectively. Fig. 3b indicates the a_0 versus T_{ox}, for V_G = 0.8, 1.0, and 1.2 V, respectively. Eq. (8) is the corresponding fitted formula for the coefficient a_0, and from Fig. 3a we find the a_0 is almost independent of T_{ox}, and has an exponential dependence in terms of V_G. For a given V_G, Fig. 3b again suggests that the a_0 is a constant for all T_{ox}. The variation of the coefficient a_0 versus applied voltage V_G is about 0.25.

As shown in Fig. 4, we plot the a_1 versus the V_G and T_{ox}, respectively. The fitting function is given in Eq. (9). We now have the a_1 is exponential dependence in V_G and linear relation in T_{ox}. The variation of the coefficient a_1 versus applied voltage V_G is about 1.0. The variation of the coefficient a_1 versus oxide thickness is about 0.8. As shown in Fig. 5, because the a_2 values are small and closed to zero, we simply set the a_2 equals 0 in this formulation, Eq. (10). To model the formula for a_3, as shown in Fig. 6, we find the behavior is more complicated then others. We here assume the a_3 is function of V_G^{α} and T_{0x}^{β}, where α and β are two exponents to be determined. The α and β in the coefficient a_3 in Eq. (11) are chosen as 2 and 1.23, respectively. The variation of the coefficient a_3 versus applied voltage V_G is about 4.0. The variation of the coefficient a_1 versus oxide thickness is about 1.2.

$$a_0 = 2.82 - 0.555\exp(-V_G), \quad (8)$$

$$a_1 = 2.22 - 1.79\exp(-V_G) - 0.21T_{ox}, \quad (9)$$

$$a_2 = 0, \text{ and} \quad (10)$$

$$a_3 = -0.00467 + 1.048V_G^2 / T_{0x}^{1.23}, \quad (11)$$

In Figs. 3 – 6, the symbols are the optimal extracted data for coefficients and lines are the fitted

functions for all cases. All above equation where V_G is in volts and T_{ox} is in nm. The model parameters given in Eqs. (8) - (11) are based on a p-type substrate with $N_A = 10^{17}$ cm^{-3}. For other substrate dopings, V_G should be adjusted by an amount equal to a shift in the threshold voltage due to the change in N_A. However, this adjustment is usually very small (~ 0.10 V). For different gate oxide thickness, Fig. 4 shows errors between the calculated optimal a's values and the fitted a's formula for the items (i) ~ (iv) with respect to V_G.

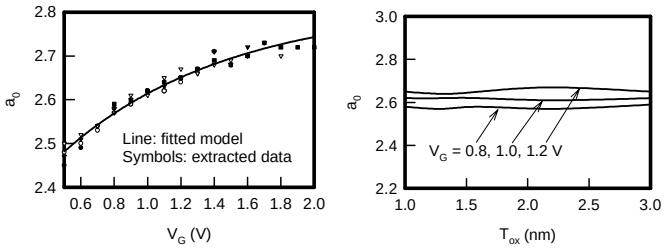

Fig. 3. (a) The plot of a_0 versus V_G. (b) The plot of a_0 versus T_{ox}. We note that the a_0 is exponential dependence on V_G and nearly constant on T_{ox}.

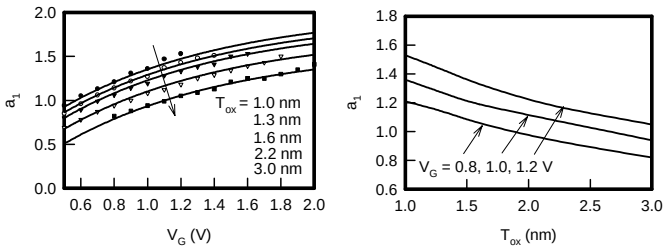

Fig. 4. (a) The plot of a_1 versus V_G. (b) The plot of a_0 versus T_{ox}.

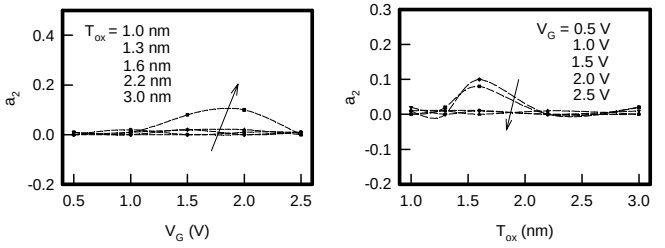

Fig. 5. (a) The plot of a_2 versus V_G. (b) The plot of a_0 versus T_{ox}. The a_2 is set to be zero constant.

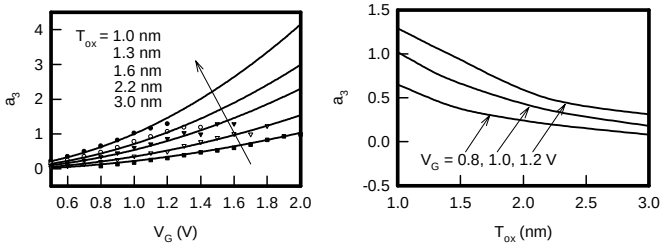

Fig. 6. (a) The plot of a_3 versus V_G. (b) The plot of a_0 versus T_{ox}.

4 Results and Discussion

This section presents the simulation results and gives a comparison of the measured data and calculated results for N-MOSFET capacitance. With the developed model and extracted coefficients, Fig. 7 demonstrates the electron density distribution versus distance away from the Si/SiO_2 interface. The oxide thickness is fixed at 2.2 nm and the applied voltage varies from 0.5 to 1.7 V. The error of the four different evaluation criteria is less than 5 %. For different oxide thicknesses, we have the same results. Fig. 8 shows the electron density distribution versus distance, where the oxide thickness varies from 1.0 nm to 3.0 nm and the applied voltage is at 0.5 V.

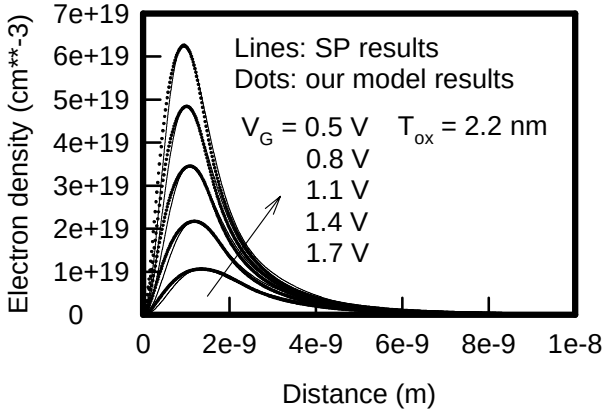

Fig. 7. The electron density distribution with the SP equations and our developed model, where the oxide thickness is fixed at 2.2 nm.

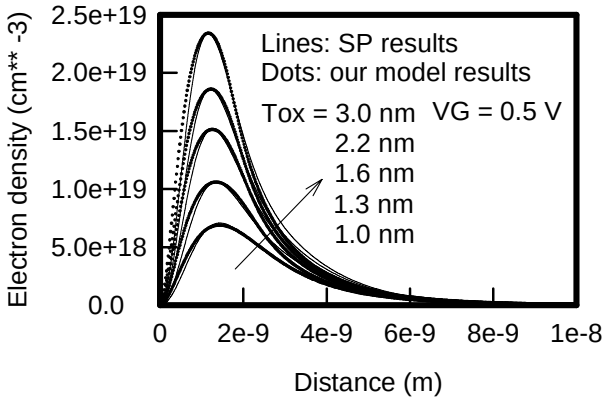

Fig. 8. The electron density distribution for different oxide thicknesses. The applied voltage is fixed at 0.5 V. The solid lines are SP results and dots are our model data.

Fig. 9 shows the achieved error control for the four type physical quantities: total charge density, average charge displacement, charge peak location, and peak value, we have found that the proposed model has good accuracy for the quantum effects

modeling and simulation. Fig. 10 is a primary result of the model and confirms the observation. We have applied our compact quantum correction model for the inversion charge to the calculation of C-V curves. A 20×20 μm^2 N-MOSFET with T_{ox} = 1.6 nm SiO_2 film is fabricated and is measured for the C-V curve measurement. The experimentally measured data is shown together with the classical and the SP result in Fig. 10. The classical result is away from the measured data. The SP result and our model result have very closed prediction along with the measured data. The agreement is excellent except for $V_G \geq 1.0$ V. This is expected as we have assumed zero penetration of the wavefunction into the oxide in our SP equation solver. The deviation of the calculated result from the measured data indicates that there is a substantial tunneling through the oxide taking place at $V_G \geq 1.0$ V.

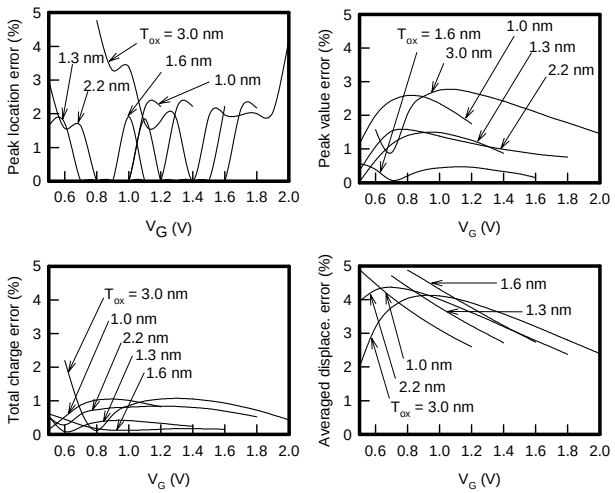

Fig. 9. The error plots of model for the four physical quantities. All errors are less than 5 %.

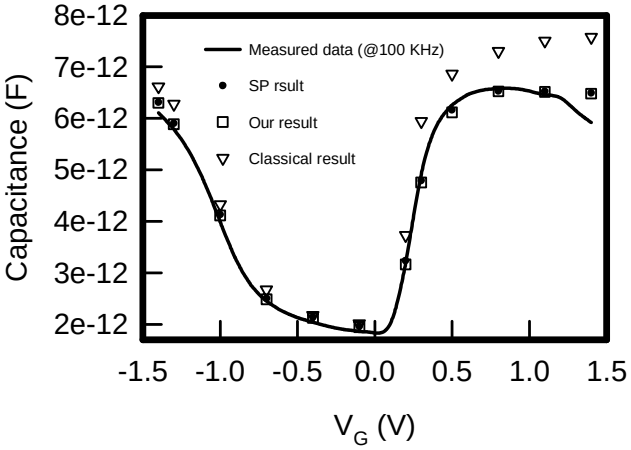

Fig. 10. A comparison of the simulated and measured C-V curves for the proposed compact model and the SP model.

We have presented an efficient compact carrier quantization model for nanoscale MOSFETs modeling in terms of gate voltage and oxide thickness. This model formulation also can be done with the model in terms of device surface electric filed and oxide thickness. Therefore the derived model can be extended into 2D/3D MOSFETs device modeling and circuit simulation. We would like to point out that our model is continuously differentiable and can be applied for circuit simulation.

5 Conclusions

In this paper, we have studied quantum confinement effects with the developed charge quantization model successfully. The charge analytical model was in terms of oxide thickness and applied voltage for nanoscale MOSFETs. Based on a comprehensive investigation of charge peak location, peak value, averaged charge displacement, and charge density, the successfully derived compact model accounting for the quantization effects enables fast and accurate characterization of the effective charge density in nanoscale MOSFETs. The error for the criteria is less than 5 %. This new model has computational superiority and can be directly applied for nanoscale device and circuit simulation without solving the SP equations. Compared with the measured C-V data of an ultrathin N-MOSFET, our simulation results have demonstrated the model accuracy. This compact quantum correction can directly couple with classical transport models to simulate the nanoscale device transport without additional numerical difficulties. Some future works also should be considered, such as the model can be in terms of the surface electric field, includes the gate current characteristics, and extends into 2D models.

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