Current State of Integrated Oscillator Design

Ali Hajimiri
California Institute of Technology MC 136-93, Pasadena, CA 91125, USA

Abstract

Different methods to build integrated resonators and frequency tuning elements are reviewed. Two new figures of merit are defined and used to compare voltage-controlled oscillators (VCO) reported by various authors. It is shown that bipolar and CMOS VCOs can achieve similar performances.

Introduction

A large number of integrated resonator-based oscillators have been reported during the last few years [1]-[19]. Different designers have tried to optimize different parameters using different circuit design techniques. These oscillators have been implemented using different process technologies (such as CMOS, BiCMOS and bipolar), operating at different frequencies (ranging from 900MHz [3][4] to 10GHz [19]). The power dissipation, tuning range and phase noise vary significantly from one design to another. It is therefore difficult to compare these designs unless a few parameter-independent figures of merit are defined to compare different oscillators.

In the next two sections, various resonators and tuning methods used in these designs will be reviewed. Next two different figures of merit are defined that will be used to compare the performance of various oscillators.

Resonators

High-frequency resonators can be built in many different ways. Here we will focus on resonators that require no explicit external component and are based on the elements that can be built in standard IC process technologies:

A. Spiral On-Chip inductors

To this date, spiral on-chip inductors are the most reliable, repeatable resonator available in standard IC process technologies. Recently, a lot of attention has been paid to accurate modeling [20], improvement [22] and optimization [21][23] of this kind of inductors. On-chip spiral inductors are reasonably repeatable and robust to changes in external parameters, however, they suffer from high loss (low quality factor, Q).

B. Wirebond Inductors

Bond wires can be used as inductors with reasonably high Q [5][10][14]. Although they offer good quality factors, they are more vulnerable to mechanical vibrations and have questionable repeatability due to the inaccuracy of wire bonding process. At higher frequencies, shorter lengths of wirebond is used, thereby further degrading the tolerance of the total inductor. Also the varactor Q becomes the limiting factor at higher frequencies, canceling the effect of higher inductor Q. Based on these observations it seems that bond wire inductors will have very limited use in the future.

C. Transmission Line Delay Elements

As the frequency of oscillation increases, on-chip transmission lines can be used as delay-lines to form a distributed oscillator [24]. The delay-based oscillators have better phase sensitivities since the passive delay elements introduce very little noise for a given delay forming a low noise ring oscillator [25].

Frequency Tuning

Frequency tuning is an essential feature in voltage-controlled oscillators. In discrete VCOs, frequency tuning is usually achieved by using high-Q abrupt or hyper-abrupt tuning diodes that can easily provide C_{max}/C_{min} ratios in excess of 4 which is enough for tuning over an octave. Unfortunately, such devices are not available in standard CMOS and bipolar process technologies and the designer is limited to a few sub-optimal options. In this section, we will review some of these tuning methods.

D. Junction Diode Tuning

The capacitance of a junction diode is a nonlinear function of the reverse bias given by [26]

$$C_j(V_{rev}) = \frac{C_{j0}}{\left(1 + \frac{V_{rev}}{\phi_0}\right)^m} \quad (1)$$

where C_{j0} is the junction capacitance with zero voltage drop across the diode, V_{rev} is the reverse bias on the junction, ϕ_0 is the junction built-in potential and m is an exponent determined by the doping profile of the junction. (For an abrupt junction m=0.5 while for a hyper-abrupt junction it is close to 2).

Quality factor of the varactor capacitance is given by

$$Q_{varactor} = \frac{1}{r_s C_j \omega} \quad (2)$$

where r_s is the series ohmic resistance of the varactor, C_j is the junction capacitance and ω is the angular frequency of interest. As can be seen from (2), the quality factor of a varactor decreases with increasing frequency. The quality factor of on-chip spiral inductors used to design oscillators is usually below 10. Therefore, for lower frequencies the quality factor of the resonator will be limited by the inductor. However, as the frequency increases, the quality factor of the inductors improve while the quality factor of the varactor degrades and will become an important factor. Because of this effect, it is imperative to minimize the series resistance of the varactor.

In CMOS process technologies, junction varactors are usually implemented using diode between the n-well and the p+ drain-source implants as shown in Figure 1a. The series resistance of this structure can be minimized using p+ patches surrounded by n+ rings as shown in Figure 1b [7].

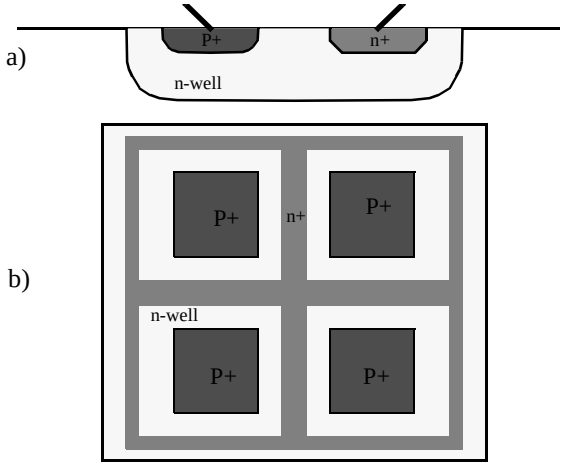

Figure 1An *n*-well p+ varactor in CMOS technology.

In bipolar and BiCMOS processes, the varactor is usually implemented using the base-collector junction of a BJT. This junction has a higher breakdown voltage which is desirable to achieve higher tuning range. Also extra care is taken to minimize the collector series resistance which directly affects the series resistance of the varactor. Unfortunately, the doping profile of the base-collector junction is not very abrupt and the exponent *m* in (1) is usually close to 0.3. This small exponent, together with the small supply voltage significantly limits the C_{max}/C_{min} ratio and thereby the tuning range.[13]

E. MOS Capacitors

The gate channel capacitance of MOS transistors can also be used for frequency tuning [10][13][14]. If the drain and source are connected together, the transistor will never enter the pinch-off region and will operate between cut-off, subthreshold and ohmic regions. Therefore, the capacitance has a minimum given by the gate-source (and gate-drain) overlap capacitance, *i.e.*,

$$C_{min} \approx 2fWL_{ov}C_{ox} \quad \textbf{(3)}$$

where *W* is the width of the device, L_{ov} is the gate-drain and gate-source overlap, C_{ox} is the gate capacitance per unit area and *f* is a fitting parameter to account for the fringing fields. As the gate voltage is raised above zero, channel inversion occurs and the capacitance will increase to its maximum value

$$C_{max} = 2W(fL_{ov} + L)C_{ox} \quad \textbf{(4)}$$

for V_{GS} in excess of the threshold voltage. In this kind of capacitor, the change in the capacitance with voltage is relatively steep. This is generally undesirable, as it results in a large sensitivity to the control voltage. Extra circuitry can be design to lower the slope, linearizing the transfer function.

F. Accumulation Mode Capacitor

An alternative metal-oxide-semiconductor structure known as accumulation mode varactor can be made in the standard CMOS process technology [27][28]. This structure is made in an *n*-well similar to a PMOS transistor, but *n+* regions are used in place of the *p+* drain and source as shown in Figure 2.

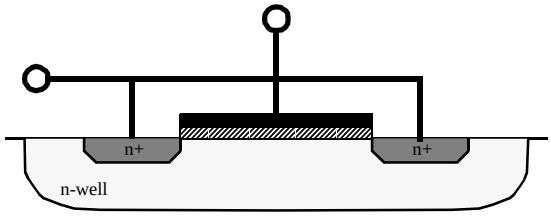

Figure 2 Accumulation mode varactor.

The capacitance of the accumulation varactor is controlled by the dc voltage between the gate terminal and the *n+* regions. For gate voltages above the flatband voltage, the extra majority carriers are attacked to the channel and therefore the capacitance will approach the gate capacitance given by (4). For small gate voltages, the total capacitance will consist of the series combination of gate capacitance and the depletion capacitance below the gate. In principle, the dc gate voltage controls the *center of the charge* of the accumulated charge in the channel.

Extra care should be taken when using this in varactor in VCO design, as the quality factor of the capacitor depends on the control voltage, having its lowest value in the middle of the tuning range. Unfortunately, middle of the tuning range is where the oscillator will be operating nominally and also has the highest VCO gain. Therefore, the phase noise will be the worst in the middle of the band. This frequency dependence of phase noise is an undesired characteristic, complicating the design.

G. Binary Weighted Capacitor Network

In many applications, the desired output frequency range of the VCO is just a few percent of the center frequency. However, due to process variations and inexact modeling, the output frequency of the VCO cannot be accurately predicted and a larger margin is required. If the center frequency of the oscillator could somehow be adjusted once in the beginning of the operation, the effective tuning range can be made much smaller and thereby improve the phase noise performance.

A binary weighted array of switches and capacitor, similar to that shown in Figure 3 can be used to adjust to center frequency in the beginning of the operation and making the varactor a smaller fraction of the tank capacitance. However, there are limitations on the size of the switches. The *W*/*L* of switches cannot be made very small size as its series resistance will introduce excess loss and hence degrade the quality factor of the tank. At the same time making the switch too large will increase the drain junction capacitor affecting the total tank capacitance.

H. Interpolative VCO

In this tuning method, the outputs of two resonators with slightly different resonant frequencies are added with different weights and fed back to themselves, as shown in Figure 4 [1][18]. If gain A_1 is set to zero, the oscillator will oscillate at

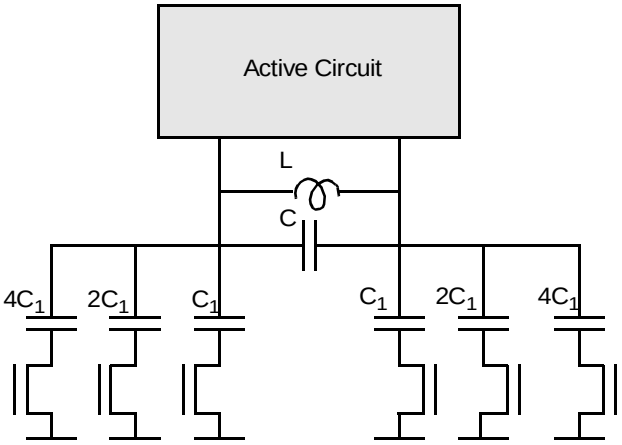

Figure 3 Binary weighted array of capacitors.

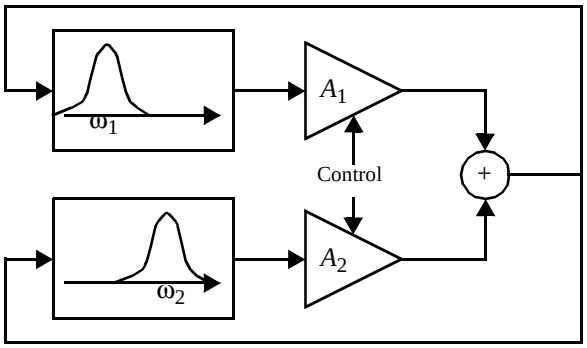

Figure 4 Interpolating VCO.

ω_2 and if A_2 is zero the output will be at ω_1. If ω_1 and ω_2 are close, for non-zero A_1 and A_2 the oscillator will oscillate at a frequency between ω_1 and ω_2 determined by the ratio of the gains. The necessary condition for single-mode oscillation is [1]

$$|\omega_1 - \omega_2| < \frac{\omega_1 + \omega_2}{2Q} \qquad \textbf{(5)}$$

where Q is the quality factor of the resonators.

Unfortunately, in this tuning scheme the phase noise has a strong dependence on the frequency, being the worst in the middle of the tuning range. This in turn results in a direct trade-off between phase noise and tuning range.

Comparison of Different Oscillators

It is a well known fact that phase noise of an oscillator measured at an offset f_{off} from a carrier at f_0 is proportional to f_0^2 and inversely proportional to f_{off}^2 [29], if all the other parameters are kept constant. Also phase noise is inversely proportional to the power dissipated in the resistive part of the tank. We would like to define a unitless quantity as the figure of merit. Therefore, we divide $(f_0/f_{off})^2$ by the phase noise. Also we would like to normalize the phase noise to the resistive noise energy, kT, divided by the power dissipated in the tank. However, the power dissipated in the resistive part of the tank cannot be easily calculated from the VCO specification. Therefore, we normalize phase noise to kT/P_{sup} where P_{sup} is the total dc power dissipated in the VCO. This way our figure of merit will also be a representative of the efficiency of the VCO in turning dc power to ac power.

Based on the above discussion we define *power-frequency-normalized* figure of merit as

$$PFN = 10\log\left[\frac{kT}{P_{sup}} \cdot \left(\frac{f_0}{f_{off}}\right)^2\right] - L\{f_{off}\} \qquad \textbf{(6)}$$

where $L\{f_{off}\}$ is the measured phase noise at the offset frequency f_{off} in units of dBc/Hz. Note that *PFN* is unitless and can be shown using dBs. A larger PFN corresponds to a better oscillator.

Although this quantity captures many of the important parameters in the design of a VCO, it completely ignores its tuning range. Generally, the relative turning range is the quantity of interest. It is defined as the ratio of the $f_{tune}=f_{max}-f_{min}$ to the center frequency, f_0. Since doubling the tuning range means making the C_{max}/C_{min} ratio 4 times larger, we should further normalize *PFN* is by $(f_{tune}/f_0)^2$. We therefore define *power-frequency-tuning-normalized* figure of merit as

$$PFTN = 10\log\left[\frac{kT}{P_{sup}} \cdot \left(\frac{f_{tune}}{f_{off}}\right)^2\right] - L\{f_{off}\} \qquad \textbf{(7)}$$

These two figures of merit are calculated and plotted in Figure 5a and b, respectively.

As can be seen from Figure 5, the designs using wirebond inductors achieve slightly better *PFN*s and *PFTN*s than those using spiral inductors. Also, designs using bipolar and CMOS process technologies are not much different in terms of their *PFN* and *PFTN*. This can be explained by the generally higher power dissipation in bipolar implementation which cancels their phase noise advantage over CMOS designs.

Conclusion

Currently available options to build integrated resonators and tuning elements were reviewed. Two new figures of merit, PFN and PFTN, were defined. It was shown that CMOS and bipolar VCOs have essentially similar normalized performances.

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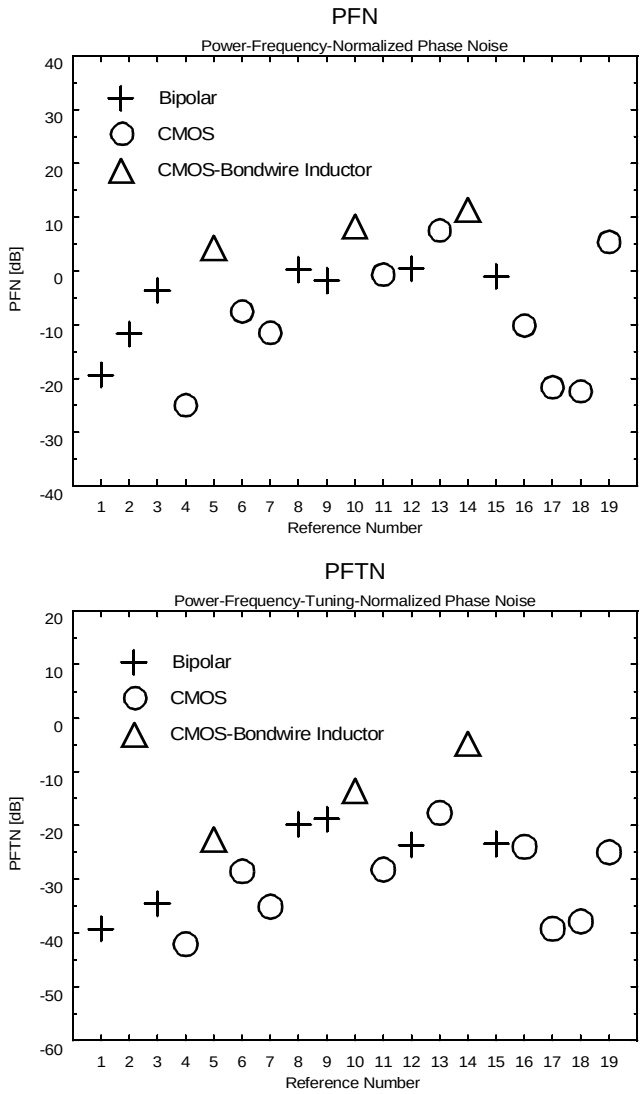

Figure 5 L_{PFN} and L_{PFTN} for various oscillators.

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