Low Power Design Methods Comparisons

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ABSTRACT

Three different low power design techniques are presented and compared in this paper. These are (1) the low-swing voltage technique, (2) the multithreshold voltage technique, and (3) the charge recycling technique. Comparison results between these techniques in terms of power dissipation, delay time, area and noise margin are examined. The proposed techniques can be used in applications with high load capacitance and long line interconnections such as bus architectures, clock designs and I/O's of chips pads. Using these techniques, SPICE simulation results show improvements in power savings as well as in power delay product.

INTRODUCTION

Low power design has become one of the most important issues in the modern microelectronic systems. The portable and hand held electronics are the most widely used low-power systems. Many techniques are used in order to decrease the power dissipation in different architectural levels. The main techniques in the circuit level are the capacitance minimization and the supply voltage reduction [1,2]. In general, the second technique is the most efficient to reduce power dissipation in digital circuits. But decreasing the supply voltage causes an increase in the delay time and the circuits become unsuitable to be used in modern applications where high throughput operation is the main feature.

An other efficient way to decrease the power dissipation in circuit level is to decrease the threshold voltage of transistors to less than *0.18*V. In this case, the low supply voltage (less than *2*V) is enough to open/close the transistors without reduction in operation speed. But it causes increase in the sub-threshold leakage current [3]. In order to decrease the supply voltage and increase the operation frequency, new technology in SPICE level should be used.

Multithreshold voltage, where high and low threshold voltage can be used in one chip, could be resolve the problem of leakage current and the fast operation.

In order to decrease the power dissipation in high capacitance load applications, low swing voltage technique could be used. Using this technique by inserting new transistor(s) in the conventional design causes in the decrease of the internal swing level voltage, where in sequence causes the decrease of the total power dissipation. *60%* of power saving are achieved.

An efficient technique in order to decrease the power dissipation is to recycle the charge in the output to the input of the circuits. This technique has also efficient results in applications where high load capacitance and bus architectures are used.

In order to compare between these three techniques, common example bus architecture that contains driver circuit, delay element and receiver circuit is designed and tested.

In section II the sources of the power dissipation are shown. In section III analysis for the three methods is introduced, in section IV discussion in the proposed techniques is given. Comparison results are given in section V and we conclude in section VI.

II. SOURCES OF POWER DISSIPATION IN CMOS CIRCUITS

Power dissipation in CMOS circuits is of three main types. Dynamic power dissipation is the result of charging and discharging of the circuit capacitances. It is the dominating one. Short-circuit power dissipation stems from the direct current from supply voltage to ground during the switching of a gate. Static power dissipation is normally very low and can therefore be neglected. For future processes technologies with possible very low threshold voltages of transistors the leakage currents may increase and become an important factor in the calculation of the power dissipation of the circuits.

III. LOW POWER TECHNIQUES

Many techniques are introduced in order to decrease the power dissipation over the different design levels. The three main techniques are the low swing technique, the multithreshold voltage technique and finally, the charge recycling technique. These techniques have the main common feature that can be used in applications with high load capacitance and long line interconnections, such as clock drivers, and I/Os chip's design.

A conventional CMOS bus architecture is shown in Fig.1. It consists of a driver, a delay element (interconnection line) and a receiver.

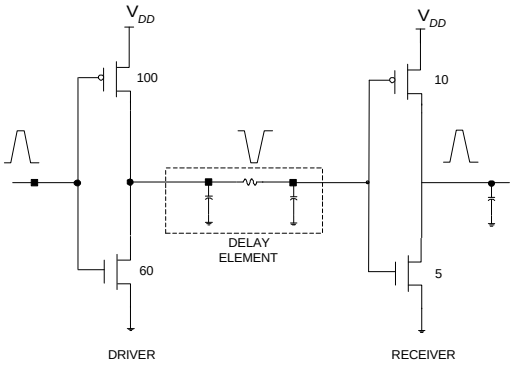

Fig.1: Conventional CMOS Bus Architecture

In this design, the driver and the receiver are both conventional CMOS inverters. The input/output voltage of the driver/receiver ranges between *0* and the power supply (V_{DD}).

The main source of power dissipation in this circuit is the dynamic current that occurs when current flows from the power supply (V_{DD}) to the output load. The power dissipation in this case can be calculated as:

$$P = C_{LOAD} \quad f \quad V^2_{DD}$$

From the above equation, lowering voltage is a direct way to reduce power dissipation, while decreasing the frequency causes a decrease in the performance of the circuits, and decreasing the capacitance causes decrease of the total area of circuits.

III.a LOW VOLTAGE SWING TECHNIQUE

An efficient technique to save power dissipation is to reduce the swing voltage in the internal nodes. It can be implemented by inserting n/pMOS transistors in some form in order to decrease the swing voltage in the output of the driver.

The input of the driver is full swing voltage that ranges between *0* and V_{DD}, so that the width of the swing is the absolute value of V_{DD}. But the width of the output of the driver V_{LS} is anyway less than the width of the conventional one. In this case, the previous equation of power dissipation could be modified as

$$P = f\, C_L\, V_{DD} * V_{LS}.$$

In order to re-pull up the low swing to full swing, a special circuit as receiver should be designed. The problem of the receivers is that the amount of current and power they dissipate in the duration of the re-pull up the swing voltage. Special attention should be taken in the receiver design.

Many papers with important results in saving power are published using this technique. Table I shows some of these results and the main characteristics of saving power, delay time, noise margin and number of transistors.

Table I

	Proposed Technique			
Paper	[4]	[5]	[6]	[7]
Saving Power	60%	60%	60%	60%
Delay Time	50%	20%	23%	20%
Area	200%	120%	150%	40%
Noise Margine	Low	High	High	Low
# of Transistors	12	8	18	16

As shown form the above table, more than *50%* of power dissipation could be saved, delay time is increased in every technique but it is less than (in any case) the power saving. Power delay product, which is the main result in low swing voltage technique is less than the power delay product of the conventional design. Area is an important factor in the current technology. Using low swing voltage technique, an increase in the area is noticed. This comes from inserting transistors in the conventional driver as in the receiver circuits where required to re-pull up the low swing to full swing.

Low swing voltage technique could be used also in other logic technology such as Complementary Pass Transistor Logic (CPL), CVSL Cascade Voltage Signal Logic, and Domino Logic. These logic technologies have the advantages that no special receiver is needed to re-pull up the low swing to full swing voltage in the last stage.

III.b MULTITHRESHOLD VOLTGE TECHNIQUE

Multi-threshold CMOS circuits, which have both high and low threshold voltage transistors on a single chip can be used to deal with the leakage problem in low power and high performance applications. The high threshold transistors can suppress the sub-threshold leakage current, while the low threshold transistors are used to achieve high performance.

Lowering the supply voltage is the most effective way to achieve low-power performance because power dissipation in digital CMOS circuits is approximately proportional to the square of the supply voltage. Reducing supply voltage from *3.3*V to *1* V means about *1/10* of the power dissipation. The low threshold voltage in this technology ranges between *0.2 - 0.3*V and high threshold voltage ranges between *0.5* and *0.65*V. The common way used by this technique is that the supply power terminals are not connected directly to the power supply lines V_{DD} and GND, but rather to the virtual power and ground lines. Table II shows some of the published papers using this technique and their main characteristics. Using MTCMOS gate delay is much smaller than that of a conventional CMOS gates.

Table II

	Proposed Technique		
Paper	[8]	[9]	[10]
Power Dissipation (ì mW/MHz)	200	220	240
Delay Time	-50%	20%	-30%
Area (mm)	2.4 õ 2.3	15 õ 15	$(6.5)^2$

III.c CHARGE RECYCLING TECHNIQUE

Charge recycling technique is also used in order to decrease the power dissipation over the circuits. It is obvious that more benefits are expected if charge recycling is used in bus and I/O designs due to their large power shares. The idea of this technique is based on reusing the charge on the capacitive output node instead of charging it in the ground. Saving power by this technique occurs because there is no direct way from the supply voltage to the ground, so that the short circuit current of the transistors is eliminated. This technique has also advantages of saving power as high-speed operation. Table III shows some published papers using this technique and the main characteristics comparing with conventional architecture.

Table III

	Proposed Technique			
Paper	[11]	[12]	[13]	[14]
Saving Power	25%	10%	24%	40%
Delay Time	-15%	20%	5%	10%
Area	200%	240%	220%	300%

In this technique, noise margin technique could not be noticed because no reducing in internal voltage is noticed. The disadvantage of high used area is noticed. From the above table at least two times the area of the conventional design is required to implement this low power technique.

IV. DISCUSSION

As mentioned before, these techniques are used in common applications such as bus architecture. Combination between these techniques could be applied in order to have more efficient results in saving power. Such as this combination, charge-recycling technique is used in low swing voltage technique as shown in [12].

Combination between the multithreshold voltage and the low swing could be applied in order to achieve the power saving in high-speed operation.

New design of driver circuit in order to decrease the power dissipation using the multithreshold voltage technology in low swing voltage technique is shown in Fig. 2. The new multithreshold CMOS driver is composed by one nMOS transistor with low threshold voltage (Low-V_T), as the conventional CMOS driver, and by a new high threshold voltage of nMOS transistor (HV_T) inserted in the design. The inserted transistor with high threshold voltage almost completely suppresses the leakage current. SPICE simulation results show improvement in power savings as well as in delay time. Table IV shows some simulation results using this technique (the number of transistors includes also the receiver circuit).

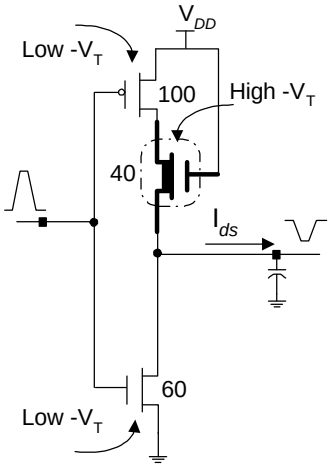

Fig. 2: High Threshold Voltage Low Swing Technique

Table: IV

	Proposed Technique
Saving Power	70%
Delay Time	10%
Area	110%
Noise Margine	High
# of Transistors	8

V. COMPARISON RESULTS

As shown from the presentation of the three low power dissipation techniques, they are efficient in decreasing the power as in power delay product of circuits.

For the low swing and charge recycling techniques, 0.5-ìm HP CMOS process technology was used. Comparison results have been derived using *0.5-ì*m double metal MTCMOS process. The device parameters are summarized in Table V.

TABLE V: Technology Device Parameters

Parameter	**High V_T Transistor**	**Low V_T Transistor**
Gate Length	0.55 ìm	0.65 ìm
Gate Oxide Thickness	110 Å	110 Å
N-Channel: Vth	0.55 V	0.25 V
P-Channel: Vth	-0.65 V	-0.35 V

In order to compare between these techniques, we designed a bus architecture using a driver circuit, a delay element, and a receiver circuit, using the three proposed techniques. For charge recycling technique, bus architecture proposed in [11] is used. Fig. 3 shows the normalized power dissipation. From this figure, it is showed that the bus circuit using multithreshold voltage dissipates least power than other two techniques, while the low swing technique using conventional technology saves more power than the charge recycling technique. For the measurements of the power dissipation the powermeter circuit proposed in [15] has been used.

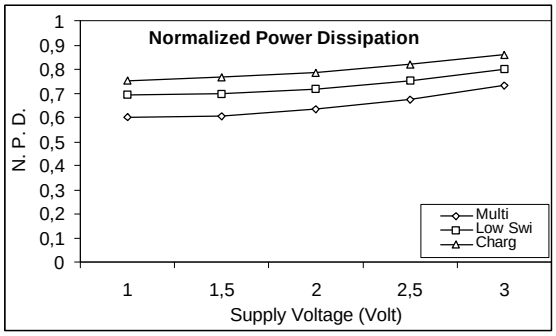

Fig. 3: Normalized Power Dissipation

Delay time is an important factor in the new high performance applications, for the three proposed bus architectures simulation results shown that the delay time of the driver in Fig. 4 is less than the other two drivers.

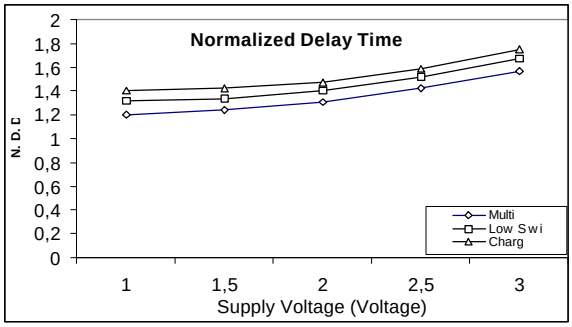

Fig. 4: Normalized Delay Time

Area is also an important factor in the low power design applications. Increasing the area causes an increase in silicon area and the capacitance. From general designs for the three bus architectures, the proposed two techniques required special design for the receiver in order re-pull up the low swing of the driver to full swing. The charge recycling required special design to re-use the charge in the output of each driver design. For different design architectures, the charge recycling required more area than the other two techniques.

Noise margin is also an important factor for the correct operation of circuits. It grows mainly when applied at the low swing voltage technique. The sources of the noise existing in logic circuits come from reasons such as ground and voltage supply noise, serial voltage noise, parallel current noise, and the interconnect noise. Noise Margin defined as the amount of noise that the system can tolerate and still maintain correct [16].

There are many ways to increase the noise margin. The designer should maintain a low ac impedance from each circuit's V_{CC} to ground. In one model for a supply bus, both V_{CC} and ground traces exhibit inductance, resistance. To reduce voltage transients, we have to keep the supply line's parasitic inductance as low as possible by reducing trace lengths, using wide trace, ground planes, strip-line or microstrip transmission-line techniques and by decoupling the supply with bypass capacitances.

In worst case of noise margin in either low noise margin or high noise margin are reduced to $0.1V_{DD}$[1]. For the correct operation of the bus architectures, the designer should be attained to not decrease the internal voltage node less than this value.

VI. CONCLUSIONS

Three types of low power design that are used widely in applications where high load capacitance and long line interconnections are occurred techniques are discussed in this paper. Combination between low swing and charge recycling has been discussed. Also discussed the combination between the low swing technique and the multithreshold voltage technique. Important results in saving power as well as in delay time occurred using the multithreshold voltage in low swing voltage technique. The near future will show many applications using multithreshold voltage in low swing technique. Disadvantages of area and noise margin have also been discussed. Power savings, delay time are also discussed. Saving power and power delay product are the main results of these techniques.

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