A 2-V CMOS IF Amplifier with Improved Single-to-Differential Signal Converter

G. Palmisano and S. Pennisi
DEES (Dipartimento Elettrico Elettronico e Sistemistico)
UNIVERSITÀ DI CATANIA
Viale Andrea Doria 6, I-95125, CATANIA
ITALY

Abstract: - This communication presents a novel CMOS IF amplifier with improved single-input differential-output converter which is able to work in low-voltage applications. The proposed solution is based on a differential stage whose output load is a folded diode-connected transistor. Thanks to it, low-voltage operation, gain accuracy, and high operating frequency are achieved. Moreover, the circuit includes an auxiliary inverting follower which increases gain, without degrading frequency response. The amplifier can inherently be used as variable-gain amplifier with the gain value set by aspect and bias current ratios. The overall circuit performance is confirmed by simulations using a 0.8-μm CMOS process. *IMACS/IEEE CSCC'99* Proceedings, Pages: 5101-5104

Key-Words: - CMOS, Low voltage circuits, IF amplifiers, Differential amplifiers, Variable-gain amplifiers

1 Introduction

Fully differential approach is usually required in high-frequency applications [1-3], due to its attractive and well-known properties of immunity to common-mode disturbances, rejection to parasitic couplings and increased dynamic range [4-5]. However, there are cases in which a single-ended source comes from an external filter although the differential approach must be preserved into the chip. Examples are the circuits which are placed in cascade to RF image filters and IF filters. In addiction, there are circuits, such as four-quadrant multipliers, that require pure differential signals to perform their function. In all these cases, a stage able to convert a single-ended signal into a differential one is needed.

A simple high-frequency amplifier with the traditional single-to-differential converter is the differential stage with one input grounded illustrated in Fig. 1. In this schematic the bias voltage to the non-used input (i.e., the gate of M2) is provided through an RC network (*R1* and *C1*). Unfortunately, this solution heavily reduces the input impedance of the circuit which is now set by *R1*. This is a limitation in CMOS circuits since capacitive source are often used.

Recently, an innovative CMOS topology that avoids this drawback has been presented by authors in [6]. Now, this solution has been greatly improved in terms of gain accuracy and low-voltage capability, thanks to the use of a folded diode-connected transistor and a high-performance single-to-differential converter. The proposed circuit was designed with a 0.8-μm CMOS technology. By using a power supply of 2 V and a current consumption of 0.3 mA, a gain of 19 dB and a cut-off frequency of 150 MHz were achieved.

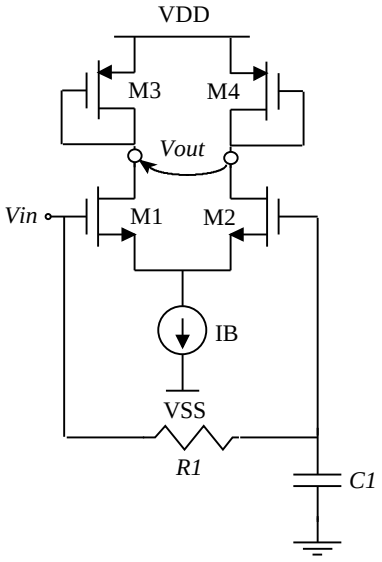

Fig. 1 - Amplifier with traditional single-to-differential converter.

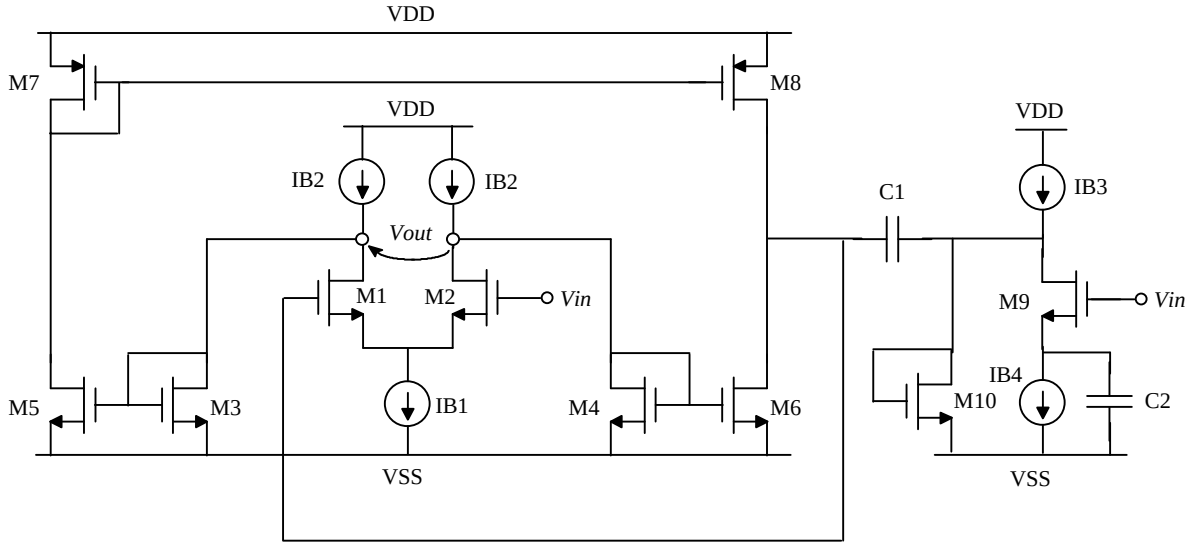

Fig. 2 - Proposed amplifier with an improved single-to-differential converter.

2 Proposed Solution

A schematic of the proposed amplifier is shown in Fig. 2. The main circuit is made up of transistors M1-M4 which implement a differential stage with a folded diode active load. Compared with circuits like the one in Fig. 1 which use PMOS diode-connected transistors, the circuit in Fig. 2 can operate with a reduced power supply and exhibits a better gain accuracy, as will be shown below.

To preserve the high value of the input impedance, the bias voltage at the gate of M1 is provided by the feedback loop made up of M5-M8. Although the offset voltage of the source-coupled pair affects in the same way the biasing accuracy, it is slightly worse than that in Fig. 1 due to the current mirror tolerances. Capacitor *C1* provides the dominant-pole compensation for the feedback loop stability and is also utilized to ground the gate of M1 at the operating frequency. Moreover, it provides the AC connection path to the auxiliary circuit made up of transistors M9-M10. This additional stage was included to increase the gain value [7]. By setting equal the aspect ratios of M9 and M10, at high frequency the stage performs an inverting voltage follower. It needs current sources IB3, IB4 and bypass capacitor *C2* to meet bias requirements.

To understand the circuit behavior, let us first consider the amplifier neglecting the contribution of the follower in the frequency response. In this case, capacitor *C1* must be assumed to be grounded rather than connected to the inverting follower output.

At low frequencies, i. e. lower than the dominant pole of the transconductance amplifier (M1-M8), the frequency response exhibits a strong attenuation due to the feedback loop around the main amplifier. At frequencies higher than the gain-bandwidth product, the loop no longer affects the transfer gain and the amplifier response is simply that of the differential stage M1-M4, that is

$$A = \frac{v_{out}}{v_{in}} = \frac{g_{m1,2}}{g_{m3,4}} = \sqrt{\frac{(W/L)_{1,2}}{(W/L)_{3,4}\left(2\frac{IB2}{IB1}-1\right)}} \qquad (1)$$

where g_{mi} is the transconductance of the *i*-th transistor. In principle, very high gains are achieved by setting IB2 close to IB1/2, but these gains would not be controlled due to the biasing tolerances. Moreover, the operating frequencies would strongly be reduced with high gain due the low transconductance of M3 and M4. However, the above equation reveals the inherent attitude of the circuit to realize a variable gain amplifier (VGA) with a large gain range. Note that gain is accurately set by both aspect and bias current ratios.

The frequency response is characterized by a zero and a pole which are placed at the dominant pole and at the gain-bandwidth product of the transconductance amplifier, respectively. Hence, the low cut-off frequency of the main amplifier is equal to the gain-bandwidth product of the transconductance amplifier and the high cut-off

frequency is set by the high-frequency poles at the amplifier outputs. The value of the low and high cut-off frequencies are

$$f_L = \frac{g_{m1,2}}{2pC_1} \quad (2)$$

$$f_H = \frac{g_{m3,4}}{2pC_O} \quad (3)$$

where C_O is the total capacitance at one of the output nodes.

Consider now the effect of the inverting follower. At low frequencies, it does not contribute to the frequency response due to capacitors *C1* and *C2* which are open circuits. At high frequencies *C1* and *C2* are shorted and a replica of the input signal but with opposite sign is supplied to the inverting amplifier input. Therefore, a balanced behavior takes place at high frequency which gives an extra gain of 6 dB.

3 Simulations

The circuit was simulated using SPICE and the model of a 0.8-μm p-well CMOS technology with threshold voltages for *n*- and *p*-channel transistors of about ±0.7 V. The supply voltage and the analog ground were set to 2 V and 1.5 V, respectively, while the quiescent current of the input pair, IB1, was set to 140 μA. From the discussion in Section 2, it follows that a good trade-off between gain, frequency response and power dissipation is achieved by adopting minimum geometry and moderate quiescent currents for M3 and M4. To take into account process tolerances and mismatches between current generators, the drain currents of M3-M4 cannot be chosen arbitrarily low. In our design they were selected equal to 20 μA by setting bias currents IB2 to 90 μA. Moreover, current IB3 and IB4 were set to 80 and 40 μA. Transistor dimensions and other electrical parameters of the circuit are summarized in Table 1.

The frequency response of circuit in Fig. 2 without and with the inverting follower are compared in Fig. 3 (curves *a* and *b*, respectively). The maximum gain values are 11 dB and 19 dB and the high cut-off frequencies are 140 MHz and 150 MHz, respectively. In the same figure, curve *c* illustrates the frequency response of the inverting follower only. Note that M9 and M10 have been slightly differently sized to account for the coupling effect between the inverter output and the transconductance amplifier output. With this expedient, it can be observed that the inverting buffer produces a nearly 0-dB response at the operating frequencies. In conclusion, the complete amplifier achieves a gain which is 8-dB higher than that of the non-enhanced version without a reduction in the frequency performance.

Finally, the proposed circuit was used as a variable-gain amplifier. Fig. 4 depicts the frequency responses obtained by varying the bias current IB1 from its nominal value, 140 μA, to 21 μA while keeping the value of IB2 equal to 90 μA.

Table 1
Main electrical parameter

Component	Value
VDD-VSS	2 V
M1 M2	20/0.8
M3 M4	6/0.8
M5 M6 M7 M8	2/0.8 μm/μm
M9	20/0.8
M10	10/0.8
IB1	140 μA
IB2 IB3	80 μA
IB4	40 μA
C1	1 pF
C2	3 pF

References:

[1] A. Rofougaran et al., “A 1 GHz CMOS RF front-end IC for a direct-conversion wireless receiver” IEEE J. Solid State Circuits, vol. 31, pp. 880-889, July 1996.

[2] A. R. Shahani, D. K. Shaeffer, T. H. Lee, “A 12-mW wide dynamic range CMOS front-end for a portable GPS receiver” IEEE J. Solid State Circuits, vol. 32, pp. 2061-2070, Dec. 1997.

[3] S. Wu, B. Razavi, “A 900-MHz/1.8 GHz CMOS receiver for dual-band applications” IEEE ISSCC Dig. Tech. Paper, San Francisco, California, 1998.

[4] R. Gregorian, G. C. Temes, *Analog MOS Integrated Circuits for signals processing*, John Wiley & Sons, 1986.

[5] K. Laker, W. Sansen, *Design of Analog Integrated Circuits and Systems*, Mc Graw-Hill, 1994.

[6] G. Palmisano, S. Pennisi, "A 20-dB CMOS IF amplifier with embedded single-to-differential input converter" accepted to IEEE ISCAS'99.

[7] N. Larciprete, F. Loriga, P. Marietti, A. Trifiletti, "A High CMRR GaAs single-input to differential convertor," Proc. Eur. GaAs Symp. 96, Paris 5-7 June 1996, paper 4C9.

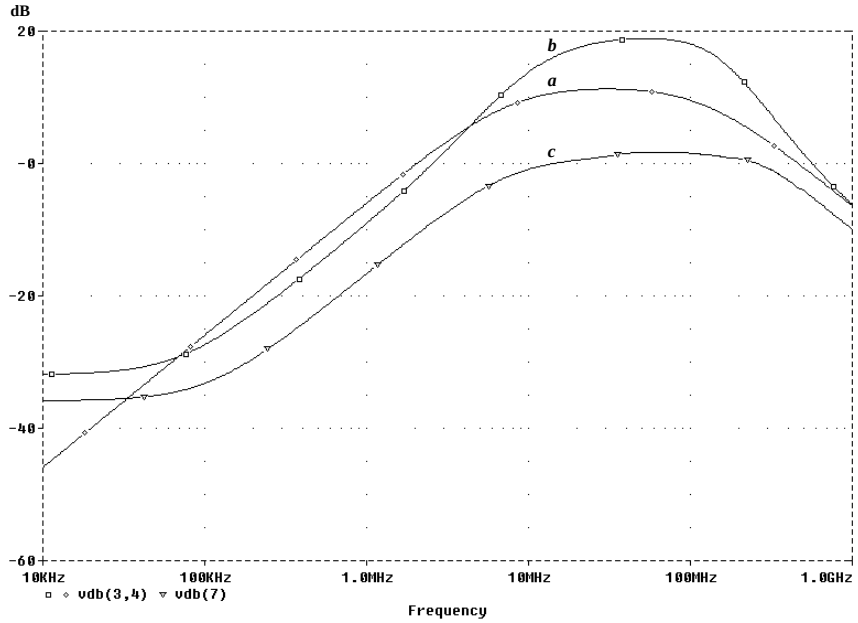

Fig. 3 - Frequency responses of circuit in Fig. 2: *a*) without the inverting follower, *b*) with the inverting follower, and *c*) the inverting follower only.

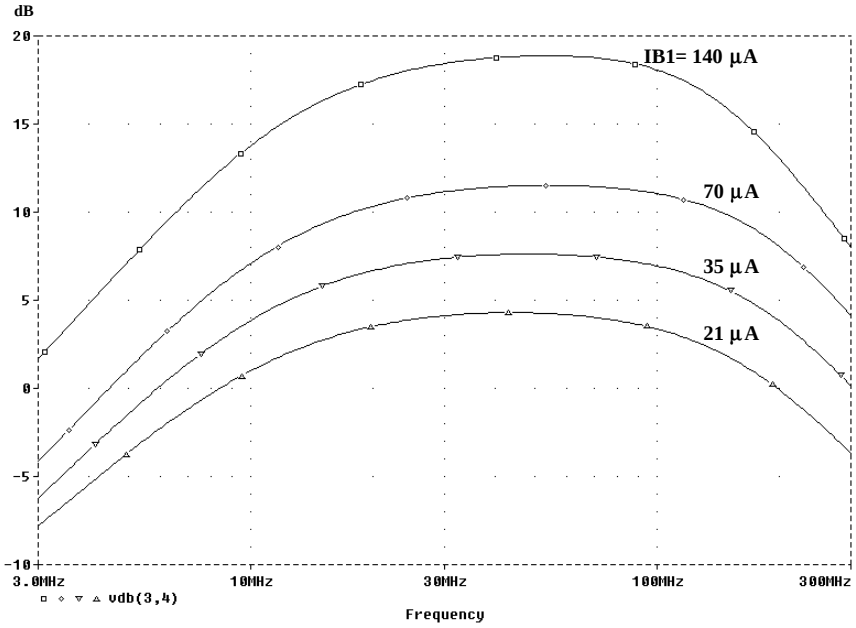

Fig. 4. Frequency response of the proposed circuit for different values of IB1