Analog Implementation of Neo-Fuzzy Neuron and Its On-board Learning

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Abstract: - A hardware implementation of the neo-fuzzy neuron with the learning mechanism by the analog technology and its application to the on-board real-time prediction of time series are described.

A neo-fuzzy neuron (NFN) is proposed for a learning machine of non-linear relations and dynamics. The NFN is produced by a fusion of the fuzzy logic and the neuroscience. The NFN describes the non-linearity of a system with a linear conjunction of the non-linear functions which is described by the fuzzy if-then rules. Its advantages are the high-speed learning exceeds more than 100 times of that of a conventional multi-layer neural networks and the guarantee for the convergence to the global minimum on the error-weight space.

In this paper, the NFN hardware system with the learning mechanism can be implemented by using the analog fuzzy inference chip developed by the authors and discrete components. The mechanism for weight updating in learning can be implemented to the simple circuit by using the characteristics of MOS transistor. The operation speed faster than $1\mu\mathrm{sec}$ has been achieved. The performance of the proposed hardware has been confirmed by the experimental results of the on-board prediction of time series. Its efficient learning ability is shown for the adaptive estimation of signals that are generated by non-linear dynamical systems. The maximum error of the on-board prediction of one-step ahead is under several percentages in full scale of input range. Furthermore, the NFN acquires system dynamics of unknown systems as linguistic rules.

Key-Words: - analog hardware, prediction, on-board learning, fuzzy system, neural networks, adaptation, global minimum, high-speed learning *IMACS/IEEE CSCC'99 Proceedings*, Pages:4401-4406

1 Introduction

Recently, an acquisition of the system dynamics from unknown systems by using the observed data is concerned by the researchers [1]. The machine learning is used as the popular way to obtain the rule of unknown system. An artificial neural network is used as a learning mechanism. Its drawbacks, from the real-time viewpoint, are a consumption of a large amount of learning time and low convergence to the global minimum.

On the other hand, several approaches combining the fuzzy logic with the artificial neural networks have been proposed by many researchers [2,3,4]. Almost of them are just combination of each technology. Therefore, the drawbacks of the artificial neural networks are still remained.

The authors focused on the special features of fuzzy logic and neural networks such as the rule-based approximate reasoning and the learning ability. The neo-fuzzy neuron (NFN) has been proposed [5], which is produced by a fusion of the fuzzy logic and the neuroscience and not just a combination of them. Its advantages are the high-speed learning of more than 100 times of that of the conventional multi-layer neural networks and the guarantee for the convergence to the global minimum on the error-weight space [6]. Since almost applications of the NFN execute on a digital computer in serial manner, the ability can not be shown efficiently.

In this paper, a hardware implementation of NFN with the learning mechanism by the analog technology is proposed. It operates in massively parallel. The performance of the proposed hardware for real-time applications has been confirmed by

experimental results of the on-board prediction of a discrete time-series.

2 Structure of the Neo-fuzzy Neuron

The NFN describes the non-linearity of a system with a linear conjunction of non-linear functions, each of which is represented with a set of fuzzy if-then rules. The structure of the n-input 1-output NFN model is shown in Fig.1. When the complementary membership function is employed in the antecedent and the singleton in the consequent, the output of the NFN y can be expressed as

$$y = \sum_{i=1}^{n} f_i(x_i) = \sum_{i=1}^{n} \sum_{j=1}^{m} \mu_{ij}(x_i) w_{ij} \ , \qquad (1)$$

where $f(\cdot)$ is a non-linear function, so called the non-linear synapse, μ_{ij} and w_{ij} is the matching degree between the input x_i and the antecedent and the weight of j-th fuzzy rule of the i-th non-linear synapse, respectively.

The gradient decent method [2,7] is used for learning of the NFN. The weight w_{ij} is updated by Eq.(2).

$$\Delta w_{ij} = -\eta \cdot (y_k - d_k) \cdot \mu_{ij}(x_{ik}) \ , \qquad (2)$$

where η is a positive number called the learning constant which determines the rate of learning and x_{ik}, y_k and d_k are the input, output and teacher's signal of the NFN at time *k*, respectively. For Eq.(2), the weights should be properly initialized (e.g., by assigning 0 as the initial weights) before the learning precedes.

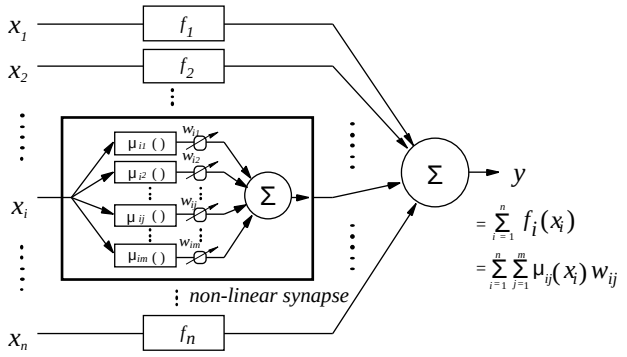


Fig.1 Structure of a n-input 1-output NFN.

3 Hardware Implementation of the NFN with a Learning Mechanism

The n-input 1-output neo-fuzzy neuron hardware with a learning mechanism is described with a linear conjunction of n single-input single-output non-linear synapses. So the single-input single-output non-linear synapse model with a learning mechanism has been implemented in this paper. The proposed hardware consists of three blocks, the non-linear synapse unit, the summing unit and the learning unit, as shown in Fig.2.

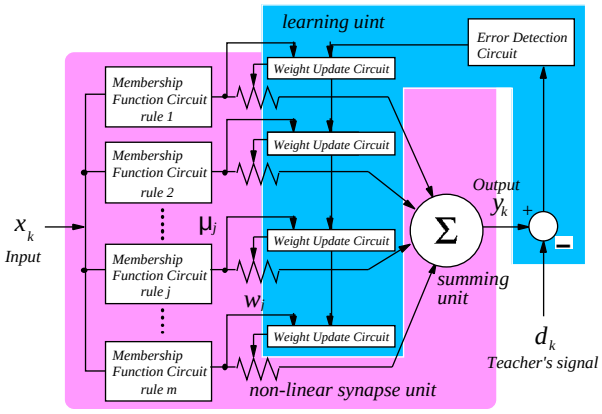


Fig.2 Single-input single-output NFN hardware with a learning mechanism.

3.1 Non-linear Synapse Unit

The non-linear synapse unit employs a fuzzy inference, which consists of the membership function circuit [8] and the weight circuit.

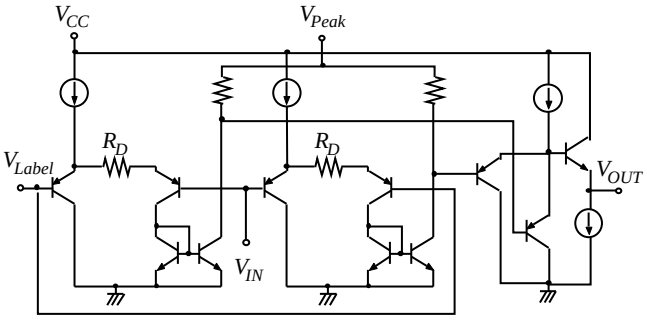


Fig.3 Membership function circuit.

The membership function circuit is shown in Fig.3, which is realized by using a part of the analog fuzzy inference chip FP-9000 developed by the authors in 1993[8].

The weight circuit designed by using a digital potentiometer [9] that works as a pulse-controlled variable resistor and a memory device. Fig.4 shows the block diagram of the weight circuit. The resistance of the potentiometer can be changed by the pulse signal labeled $\overline{INC}$. When a $U/\bar{D}$ is high, its resistance is increased and low decreased. The $\overline{INC}$, $U/\bar{D}$ are produced by the weight update circuit and the error detection circuit, respectively. The accuracy of the NFN hardware mainly depends on the resolution of the weight circuit.

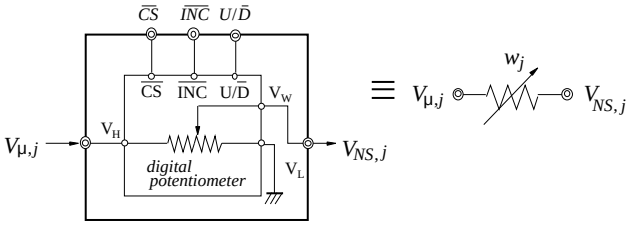


Fig.4 Weight circuit employing a digital potentiometer.

3.2 Summing Unit

The summing unit aggregates outputs of all the non-linear synapse units, which is realized by an ordinary adder circuit with op-amps. For input-expansion of the NFN, no additional summing unit is necessary because that can be used commonly.

3.3 Learning Unit

The learning unit updates the weights by the gradient decent method, which consists of the error detection circuit and the weight update circuit.

The error detection circuit, as shown in Fig.5, generates the error voltage V_{ERR} corresponding to a difference between the output of NFN and the teacher's signal and a sign of the error $U/\bar{D}$. V_{ERR} and $U/\bar{D}$ are represented as

$$V_{ERR} = -V_{B1} - \left| V_d - V_y \right| , \quad (3)$$

$$U/\bar{D} = \begin{cases} 1 & (V_d - V_y > 0) \\ 0 & (V_d - V_y \le 0) \end{cases} , \quad (4)$$

$$-V_{B1} = 5 - \left| V_{TH1} \right| , \quad (5)$$

where V_y, V_d and V_{B1} are the output of the NFN hardware, the voltage corresponding to the teacher's signal d_k and a bias voltage for compensating of a threshold voltage V_{TH1}, respectively.

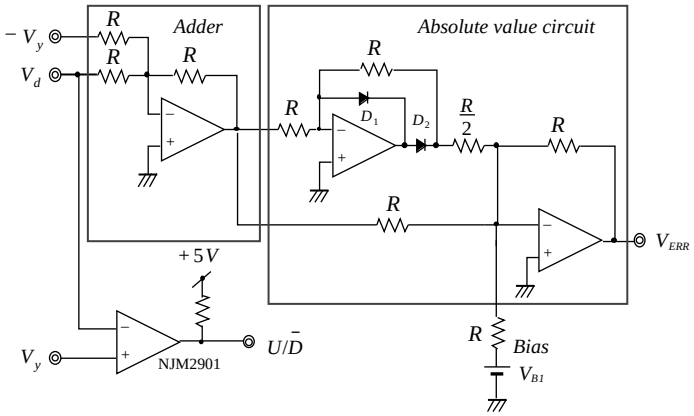


Fig.5 Error detection circuit.

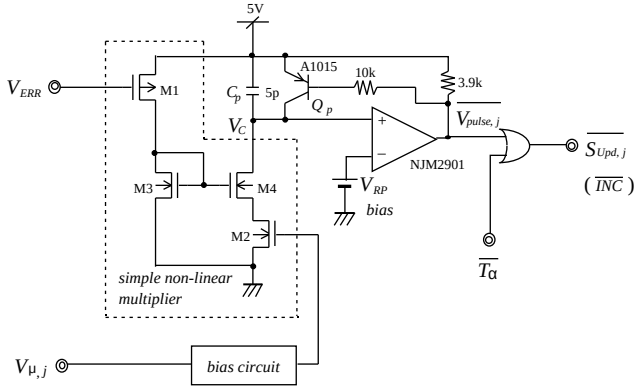


Fig.6 Weight update circuit.

For the gradient decent method, the weight can be updated according to Eq.(2). The update of each weight should be achieved in parallel with learning. Since Eq.(2) contains a multiplication, its implementation causes an increase of hardware size and a decrease of the operation speed. We propose the weight updating mechanism constructed with the simple non-linear multiplier by using the characteristics of MOS transistor as shown in Fig.6. The weight resistance can be represented as the following Eqs. ,

$$\Delta R_j = SGN \cdot \Delta R \cdot P_{Upd,\,j} , \quad (6)$$

$$SGN = \begin{cases} +1 & (U/\bar{D} = 1) \\ -1 & (U/\bar{D} = 0) \end{cases} , \quad (7)$$

where ΔR_j, ΔR are an update resistance corresponding to j-th rule of the non-linear synapse and a unit resistance of the digital potentiometer, respectively. $P_{Upd,\,j}$ is a number of updating pulses during a learning period with $\overline{T_\alpha}$ remaining low. Since the input of NFN is fixed for learning (updating weights), $V_{\mu,\,j}$ corresponding to matching grade of the input and the antecedent is constant. Therefore, the frequency of the updating pulse can be a function of V_{ERR}, as described by Eq.(8).

$$f_{Pulse,\,j}(V_{ERR}) = K \cdot g(V_{ERR}, V_{\mu,\,j}) = K' \cdot g(V_{ERR}) \ , \qquad (8)$$

where $g(\cdot)$ is a non-linear function, as shown in Fig.7, is composed of pMOS's and nMOS's $V_{GS} - I_D$ characteristics [10], and *K*, *K'* are coefficients.

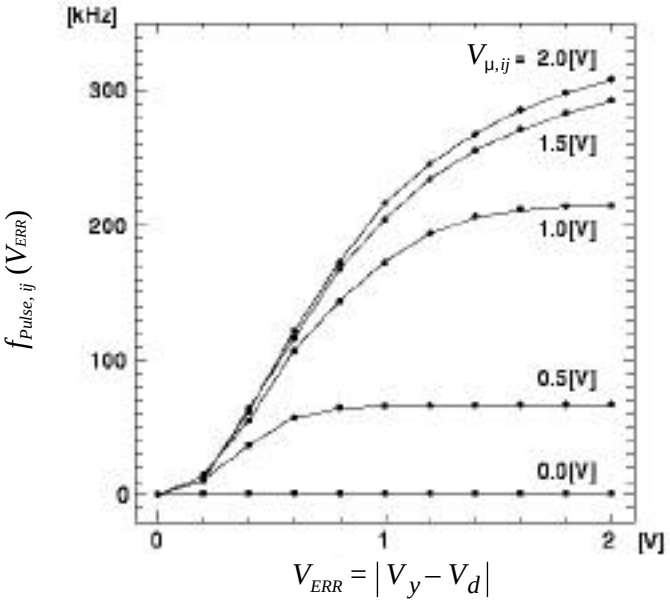
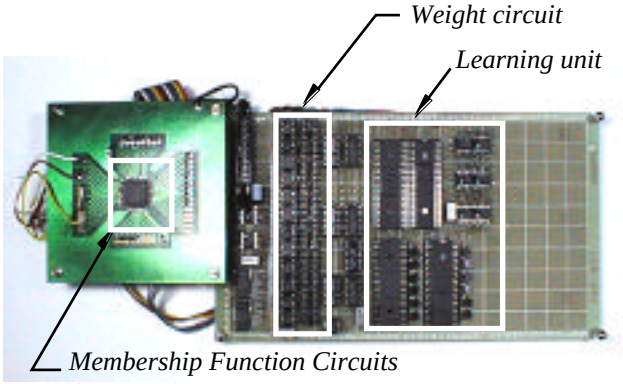


Fig.7 Relations between the frequency of weight updating pulse and the error voltage.

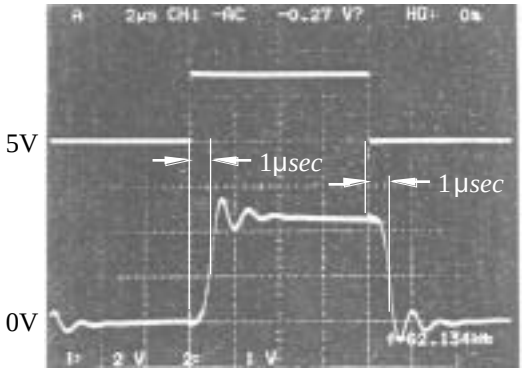
3.4 Single-Input Single-Output Neo-Fuzzy Neuron (NFN) Hardware

The single-input single-output NFN (non-linear synapse) hardware with the learning mechanism has been developed as shown in Fig.8 (a). The membership function in the antecedent is programmable and can be assigned up to twelve labels. The input signal of the NFN hardware ranges from 2.5-7.5V. The teacher's and the output signals are represented by voltage ranging from 0-2V.

The operation speed of the proposed hardware achieves faster than 1μsec as shown in Fig.8 (b).



(a)



Upper: Input (V:2V/div.)
Lower: Output (V:2V/div.)
*H: 2*μ*sec/div.*

(b)

Fig.8 (a) Single-input single-output NFN hardware with the learning circuits; twelve labels in the antecedent are available and (b) its step response.

4 Experimental Results

In order to confirm the performance of the proposed hardware, the on-board prediction of the time series is examined.

4.1 Prediction System

Fig.9 shows the prediction system of one-step ahead where the single-input single-output NFN hardware is employed for the learning mechanism.

When $y(k)$ is fed to the NFN hardware, the hardware produces the predicted value $y(\hat{k+1})$ at time k+1. At the next time k+1, the true value of time k+1 is observed. So the NFN hardware updates the weights by learning with $y(k+1)$ as a teacher's signal. After that, the NFN hardware repeats with prediction and learning in the same manner. In this learning procedure, the system converges to the optimum state as time goes on. Therefore, this method is called the adaptive prediction.

The time series, as shown in Fig.10, can be created from the non-linear dynamical system described by Eq.(9) on a personal computer.

$$y(k+1) = 4\{1 - y(k)\} \cdot y(k) \quad k = 0,1,2, \ldots . \qquad (9)$$

This non-linear function is so called the logistic function, which is well known to generate a chaotic behavior [11].

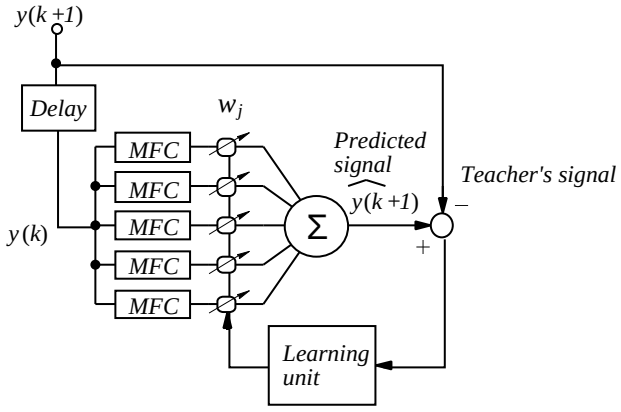


Fig.9 On-board real-time prediction system.

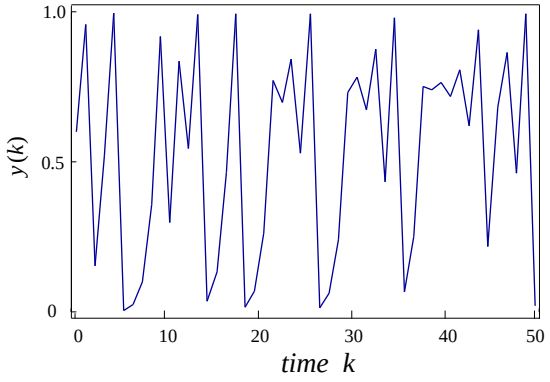
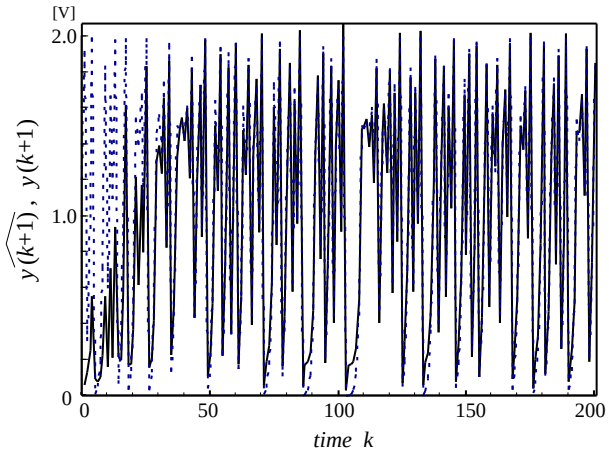


Fig.10 Time series for learning and prediction.

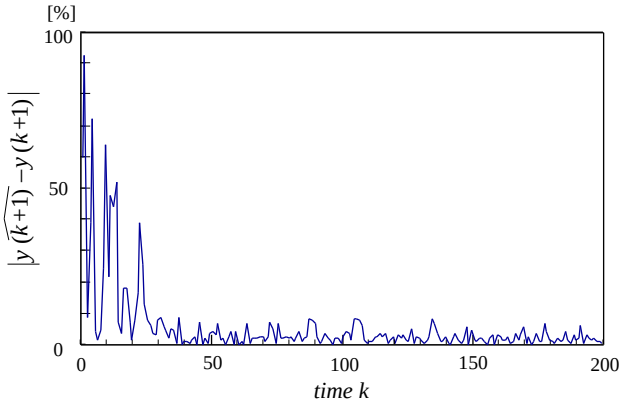
First several steps of the time series are used for the learning to identify the system. That data set of digital signal is converted to analog voltages through a 12-bit D/A converter, and fed to the NFN hardware.

4.2 Adaptive Prediction of Time Series

Experimental results of the on-board prediction of one-step ahead and its error are shown in Fig.11 (a) and (b), respectively. In the experiments, five labels are used in the antecedent of the non-linear synapse.



(a)



(b)

Fig.11 Prediction results of one-step ahead by the proposed single input single output NFN hardware with five labels in the antecedent. (a) Predicted results; ----, true time series; ——, predicted time series, and (b) its error.

The prediction error is decreased quickly as shown in Fig.11(b). Finally the error converges to about several percentages in full scale of an input range, which depends on the resolution of the potentiometer (equivalent to 7bits in this case).

The prediction time of one-step ahead is about 0.6msec, almost of which is spent for data transferring between the proposed hardware and the personal computer. The net operation speed (which includes the learning, and excludes the data transferring) is less than $160\mu\mathrm{sec}$. Therefore, the proposed hardware seems available for practical applications of an analog signal processing in real time.

5 Conclusions

The analog mode NFN hardware with the learning mechanism is described. The proposed hardware achieves high-speed operation enough for the real-time applications and its performance was confirmed by experimental results for the prediction of time series that is produced by the non-linear dynamical system.

The advanced version of the NFN hardware is now under implementation to a silicon chip for practical applications and will be reported in the near feature.

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