Reliability in VLSI Electronics for Space: The Case of The Flash ADC

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Abstract:

Ignoring the specific constraints applied to Integrated Circuits functioning in a radiation environment - like high atmosphere and space - may have some invaluable consequences for flights or human missions. Indeed, phenomena like ionizing effects, collision with heavy ions or neutrons cause failures and erroneous responses in microelectronics if no hardening is provided.

To prevent the failures, some arrangements are currently put into place at the *system level*. They take advantage of redundant circuits with voting procedure. Another method is to improve the reliability at the *technology level* using rad-hard processes, like SOI. This appropriate answer appears expensive and so, is not always desired.

Facing with the new needs of electronics in space systems, a tendency has emerged coming with a best knowledge of the degradation phenomena. It consists to act at the *design level* employing the standard technologies. The interest of this plan is to save, at the same time, weight, silicon area, power consumption, performances and cost.

Flash Analog to Digital Converter (Flash ADC) is a key element in the high speed data acquisition process. It has been proved to be highly sensitive to both of the radiation effects: the total ionizing dose due to electromagnetic radiation and the electrical upsets induced by heavy ions (SEU) in some specific areas of this circuit.

Nevertheless, at our knowledge, no viable ADC hardening solution using design has been proposed excepted for total dose. The presence of analog parts, functioning constraints and a complex architecture are probably the causes of this lack of solutions (notably for the SEU hardening of ADC).

In this paper, we propose a partitioning of the Flash ADC architecture in different blocks for the purpose to identify each behavior and responses to perturbations. Then, we expose the way to reach the robustness individually, allowing an improved reliability of the whole structure. Two complementary methodologies are initiated: a reconfiguration technique of the logical structure coupled with the hardening by design of the individual blocks.

A double 6 bits ADC has been implemented in a standard technology (bulk-CMOS 0.6 µm). The post layout simulations performed on each block and the whole structures have demonstrated the hardening efficiency of the proposed solutions, resulting in an increase of the reliability. Moreover, the performances of the ADC are maintained owing to our methodology. IMACS/IEEE CSCC'99 Proceedings, Pages:2901-2905

Key-Words: VLSI, Flash ADC, Reliability, Space, Robustness, Hardening, Restructuring, Design.

1 Introduction

The devices functioning in space are submitted to specific constraints related to the radiation environment. Consequently, the use of standard systems and circuits non dedicated to space in this harsh environment may cause inestimable consequences for flights or human missions due to their deficiencies and faulty responses [1,2].

Coming with this prerequisite, performances, size reduction, low power and *low cost* stay always essential for integrated systems. As a consequence, the hardening of circuits by acting at the design level in a standard technology received since some years a greater amount of attention [2-7]. It was in particular

the case with memories, due to their sensitivity to heavy ions. In that case, authors have demonstrated that solutions can be found [3-7].
The purpose is to realize a Flash ADC with an improved reliability. So, this work must also go into the consideration of the analog circuits sensitivity established by the previous works [8-12]. Our hardening methodology is based on design solutions and supports a CMOS standard technology. This approach saves the ADC performances and satisfies all the specifications.

2 Space Effects Description

Among the observed effects, one of the major outcomes is the "Total Ionizing Dose" (TID). The dose effect is permanent and so, cumulative. It intensifies principally leakage current in nMOS and modifies the threshold voltages of nMOS and pMOS [2]. In the long term the TID induces a circuit failure. The direct effect of the TID on a bulk-CMOS inverter is shown Figure 1. We can see a distortion of the transfer curve with as a consequence a noise margin decrease.

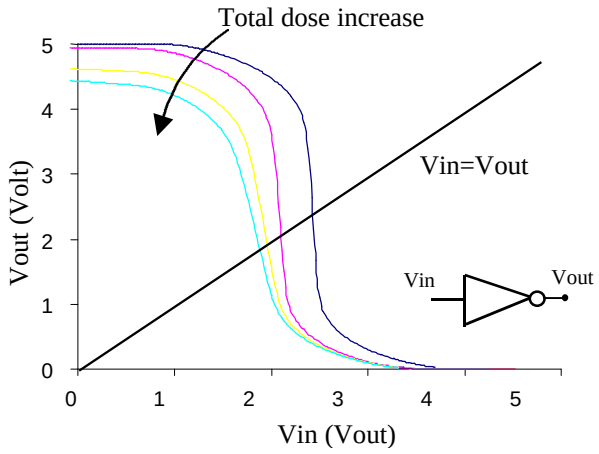

Figure 1: Transfer curves of the CMOS inverter following an increase of the total ionizing dose (Bulk-CMOS technology).

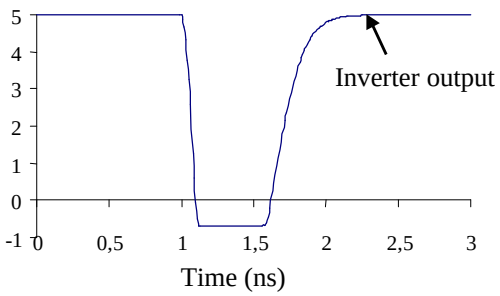

Fig.2: SEU effect at an inverter output.

Another major effect is the Single Event Upset (SEU). This effect is caused by heavy ions striking a sensitive area of the circuit. When such a particle hits a reverse biased junction, the charges generated along the ion track are collected and a transient current pulse is induced at the electrical node. Then, the electrical response shows a temporary disturbance of the voltage level with all the definitive consequences attached to the logical states of the memory type circuits (Figure 2).

3 Set of problems in Analog Circuits Hardening

We have seen that the *SEU hardening* by a restructuring has been probed in the past for digital circuits [3-7]. On the other hand, even though some authors have shown the strong SEU sensitivity of analog circuits [8-10] and ADC [11-12], no satisfactory hardening solution using design has been proposed. This lack of proposals for circuits like ADC can be explained by the basic differences existing between the digital and analog consequences of the perturbations. When an uncontrolled upset happens in digital circuits, only a logical level has to be saved. So, concepts like redundancy, high impedance state, RC filtering allow the protection or a recovery of the true state. Such principles cannot be used with efficiency on analog circuits for which the exact voltage level has to be maintained. Indeed, the time necessary to react against the very rapid increase of charges coming from ion hit is too short to allow to keep accurately the voltage safe. In conclusion, the SEU hardening using a new analog structure seems to be an insurmountable task. So, a most obvious solution has to be found.
At the same time, considering the dose effect, analog cells are the more sensitive circuits. So comparators stage has to be designed taking account the total dose.
Based on this discussion, we shall use a specific analog comparator to improve the dose tolerance of Flash ADC. For the SEU hardening, we shall suggest a corrective logic.

4 Flash ADC Structure

The functional diagram of a standard flash Analog to Digital Converter circuit is sketched in Figure 3. The architecture of this high speed converter includes a set of blocks: a resistor ladder generating the reference voltages, comparators, latches, encoder that we will analyze now. The comparators (block 1)

bring into comparison the analog input signal with the reference voltages and generate a thermometer code latched by flip-flops. This code is changed for a 1 of N code by using AND gates (block 2). Then, an encoder (block 3) generates the corresponding output binary code.

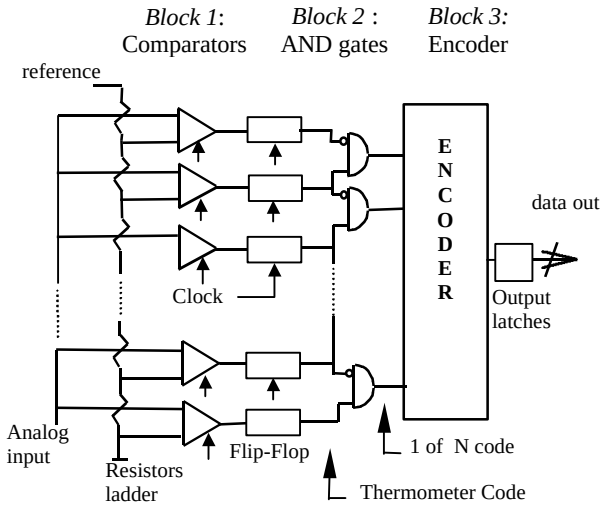

Figure 3: Flash ADC block diagram.

Let us see now the sensitivity of the different blocks depending on the nature of the effects - dose or SEU - :

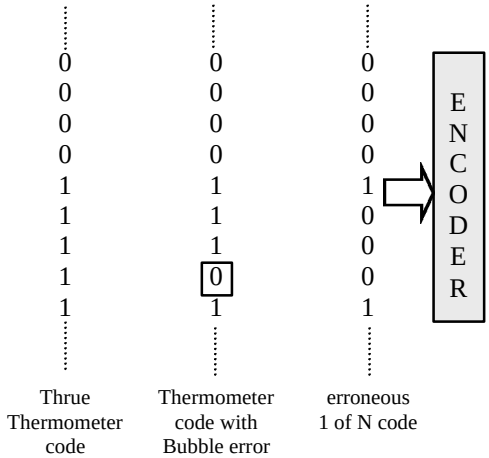

Figure 4: Bubble error induces erroneous ADC outputs.

- The comparators are elements easily affected by the both phenomena. As usual, the total dose causes a rapid increase of the imprecision followed after a long time by a permanent ADC failure (due to a prohibitive consuming). In the SEU case (when a heavy ion hits a sensitive area of a comparator), a wrong comparison can appear. In this case, the event causes a "bubble error" in the thermometer code, as illustrated in the Figure 4. Then a conflict exists at the encoder inputs and results in wrong ADC outputs.

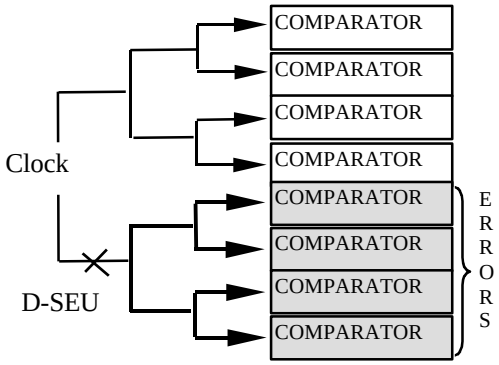

Figure 5: upset arisen at a binary tree inverter output inducing several comparison errors.

- The clock is highly critical in Flash ADC. To avoid problems related to jitter and rise/fall times [13,14], the clocks of the comparators are necessarily issued from a binary tree. So, if an upset surges at any inverter-output of the binary tree, it propagates (Fig. 5) [15] and the clocks of a high number of comparators can switch at the same time. This effect induces a *set* of bubble errors in the thermometer code (Fig. 5).
- A ROM is generally used for the encoder. This block is susceptibly to be affected by the total dose if the leakage current and/or the threshold voltage shift of nMOS become also important. In that case, the high level established on buses can be destroyed [16].
- The latches and flip-flops are too SEU sensitive. Their loop structure yields to the storage of an erroneous bit [3-7]. In spite of this disadvantage, they remain key elements to reduce flash ADC metastability and to synchronize signals [13,14].

4 Hardening Solutions

4.1 Dose effect hardening of the comparators

An improvement of the total dose hardening is obtained using the advantages of the cyclic Auto-Zero Comparator [16-18]. The schematic is given Figure 6.

Before each conversion (first half of a cycle), TG1 and TG3 are switched ON (TG2 OFF). The inverter is set in its auto-zero mode with the B input voltage equal to the C output voltage. The transistors characteristics variations due to the total dose are automatically compensated (see Figure 1). So, the comparator is always "self-biasing" in the maximum gain region of the inverter. At the same time, reference voltage (Vref) is applied at node A.

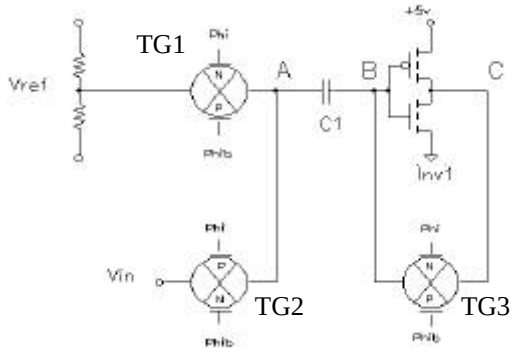

Figure 6: Cyclic Auto-zero comparator improving total dose hardening.

During conversion (second half of a cycle), TG2 is switched ON while TG1 and TG3 are OFF. Then the input voltage Vin of ADC is applied to the node A. If Vaz is the autozero potential, the voltage at node B is:

Vaz-(Vref-Vin)

Then the inverter amplifies (Vref-Vin), and the comparison step is over.

Often, a second auto-zero inverter at node C is used to increase gain and reduce metastability problems [13-14].

4.2 SEU hardening of comparators

To rectify a bubble error due to a heavy ion hitting a sensitive area of a comparator (Figure 4), a built-in redundancy technique has been used. Usually, the transformation of the thermometer code to 1 of N code needs simple gates realizing the operation: $\overline{C_n}.C_{n+1}$, where C_n and C_{n+1} are respectively the output logic levels of the n and n+1 comparators (Bloc 2, Figure 3). Instead of it, a different logic structure is used: $C_{n-1}.\overline{C_{n+2}}.(C_n \oplus C_{n+1})$. In that case, the presence of a bubble error will no more affect the 1 of N code.

4.3 SEU hardening of the Binary Tree

To overcome the previous defined problem of upset propagation in the binary tree (Figure 5), we propose to use a Dissociated Binary Tree (DBT, Figure 7). In this case, if upset arises at a binary tree inverter, the wrong comparisons induced by the upset propagation are separated by more than 3 comparators. Then, the previous corrective logic $C_{n-1}.\overline{C_{n+2}}.(C_n \oplus C_{n+1})$ is apt to maintain the true 1 of N code (Figure 7).

The “root inverter” of the DBT stays the only sensitive inverter able to transmit errors. We have check that the immunity can be attained using a large transistor sizing (like an input pad inverter), and loading the inverter with enough large capacitance (RC filtering technique).

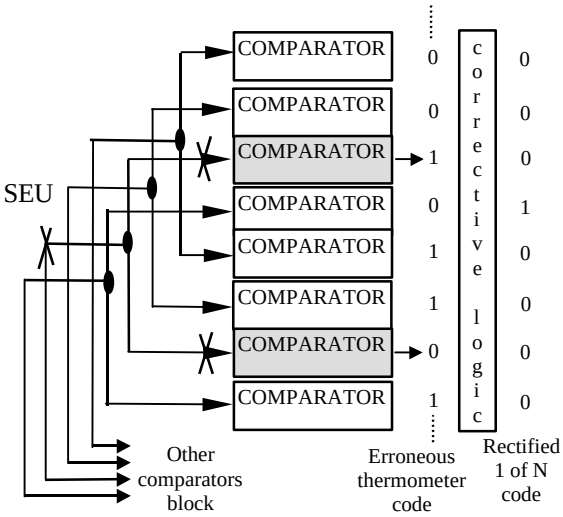

Figure 7: correction of false comparisons due to a SEU arising on a binary tree inverter.

4.4 Encoder hardening

If a special preventive rule is considered during design, the ROM used as an encoder becomes a structure propitious to resist to the radiation effects. This rule consists in the exclusion of the usual bus precharge [16] and its high impedance state. This last condition is obtained by producing the 1 level through a pMOS and the 0 level through a nMOS. So, any increase in the nMOS leakage current and threshold voltage shift are prevented.

5 Conclusion

The SEU hardening solutions proposed in this paper, successively corrective logic, dissociated binary tree and ROM, only use standard technology, restructuring, and design. In the same way, and not detailed hereupon, some complementary works permit to improve even more the SEU hardening of flip-flops and latches used formerly [6,7].

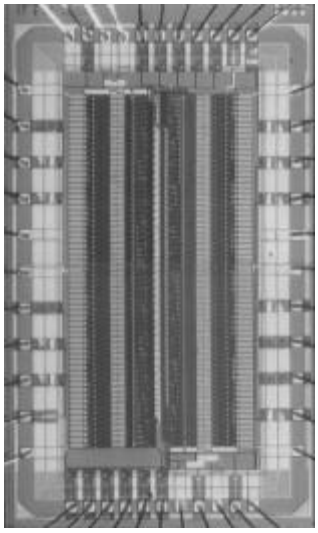

Figure 8: Microphotograph of the two 6 bits Flash ADC (AMS 0.6 µm technology).

The first interest of this approach is to save performances, area, and consumption of the Flash ADC. Another interest is that the designer stays free to choose an analog design for the comparator adapted to the environment. So the use of any total dose hardened analog structure becomes possible. This has been made effective with the implementation of the rad-tolerant flash ADC (Figure 8).

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