# Branching Effects of Ideal Switching

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*Abstract:* - The ideal single-switching, i.e., the zero duration change of the state of a switch between ideal short-circuit and ideal open-circuit conditions is an instantaneous event with a unique well defined outcome in what concerns the effect on the state dynamics of an electric circuit. On the contrary, an ideal multiple-switching -- consisting in the "simultaneous" zero duration change of the states of a set of switches -- can have several outcomes. The state trajectory of an ideal electric circuit with inconsistent initial conditions (IIC) at $t = 0^-$ can branch into several possible paths after such an event, even when the overall duration of the multiple-switching decreases to zero. In fact, there are several consistent initial conditions (CIC) at $t = 0^+$, immediately after the switching, which correspond to the same inconsistent initial conditions (IIC) at $t = 0^-$, immediately before the switching. Each of these consistent initial conditions corresponds to another state trajectory of the circuit after the switching. This ambiguity can be removed if the multiple switching is described not as an instantaneous event, but as a process consisting of a sequence of elementary single switching events. When the overall duration of this process is shorter than any chosen arbitrary small positive boundary, i.e., when the multiple switching becomes "instantaneous," still the order of the elementary switching events remains significant.

The paper continues the previous work of the authors in the analysis of the multiple ideal switching, by using a DEDS approach to systematically establish the full range of distinct classes of multiple switching processes leading to different values of the state variables at $t = 0^+$. It is shown that the number of distinct classes of multiple switching processes is far less that the number of all such possible processes, which results from the permutation of the sequence of component elementary single switching events.
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## 1. Introduction

In most practical cases, the details of the rapidly changing signals during a switching are not relevant for the analysis of a switched circuit in the intervals between the moments of the switching. Consequently, many tools for the analysis of switched networks consider idealized models of the switches (short- or open-circuit elements), and treat the switching itself as an instantaneous event. It is well known [9] that, despite being conceptually simpler, this approach often leads to circuits with excess storage elements and inconsistent initial conditions (IIC), which in turn determine the discontinuity of the network variables at the moments of switching. As a consequence, Dirac impulses and their various order derivatives can occur in the circuit variables than are proportional to the derivatives of the discontinuous variables (e.g., the currents of the capacitors with discontinuous charges/voltages, and voltages of the inductors with discontinuous magnetic fluxes/currents). These impulses "instantaneously" adjust the IIC at $t = 0^-$ to consistent initial conditions (CIC) at $t = 0^+$.

The difficulties caused by these discon-tinuities and impulses in the numerical analysis of switched circuits prompted a considerable work dedicated to study of IIC [1–8]. Two problems have been identified in connection with the ideal switching of the circuits with excess storage elements [1-8]: (1) finding the CIC after the switching ($t = 0^+$), when knowing the IIC before the switching ($t = 0^-$), (2) computing the area of the Dirac impulses that occur at a switching moment. In previous papers [10-14], we identified a third problem that has to be considered in this context:

(3) In the case of ideal multiple-switching, when the state of several ideal single-switches change “simultaneously”, the switching can not be described as an instantaneous event, but as a process specified by the sequence in which the individual single-switching occur. This is the result of the “infinitely fast” variations (discontinuities) caused by the ideal switches placed in *C*-loops when going into the *ON* state (short-circuit) and by the ideal switches placed in *L*-cut-sets when going to the *OFF* state (open-circuit).

The rest of the paper is organized as follows: Section 2 briefly recalls the problem of IIC in circuits with excess elements; Section 3 describes idealized switching seen as a process; and Section 4 presents a method of exploring the range of distinct transitions in an idealized switched network based on an untimed discrete event dynamic system model. Some conclusions are formulated in section 5.

## 2. IIC in circuits with excess elements

The IIC problem arises for ideal switching in ideal circuits, when the circuit after the switching contains excess elements. The IIC cause difficulties in the numeric analysis of switched circuits, because the Dirac impulses disturb the normal operation of the circuit simulators. It is desirable to separate the study of the switching from the integration of circuit equations over the intervals between the switching moments. Replacing the switches with short- or open- circuits reduces the complexity of the problem and makes it numerically better conditioned. Two reduced circuits, containing only the capacitors and the independent voltage sources, and only the inductors and the independent current sources from the original network, respectively, can be used to directly find the conditions at $t = 0^+$ from the conditions

of $t = 0^-$ [6-10]. Let establish the equations of a circuit that has *C*-loops and/or *L*-cut-sets. For each independent *C*-loop one of its capacitors is considered an excess element, and for each independent *L*-cut-set one of its inductors is considered an excess element. The storage elements that are not in excess are essential elements. The essential storage elements are denoted by $\boldsymbol{C}$ and $\boldsymbol{L}$, the excess ones by $\boldsymbol{C'}$ and $\boldsymbol{L'}$, and the independent voltage and current sources by $\boldsymbol{e}$ and $\boldsymbol{j}$, respectively. The remaining linear resistive multiport, that can contain controlled sources of any type, is described [9] by the multiport equations:

$$\begin{bmatrix} \boldsymbol{i}_C \\ \boldsymbol{u}_L \\ \boldsymbol{u}_{C'} \\ \boldsymbol{i}_{L'} \end{bmatrix} = \begin{bmatrix} \boldsymbol{a} & \boldsymbol{c} \\ \boldsymbol{d} & \boldsymbol{0} \end{bmatrix} \begin{bmatrix} \boldsymbol{u}_C \\ \boldsymbol{i}_L \\ \boldsymbol{i}_{C'} \\ \boldsymbol{u}_{L'} \end{bmatrix} + \begin{bmatrix} \boldsymbol{b} \\ \boldsymbol{f} \end{bmatrix} \begin{bmatrix} \boldsymbol{e} \\ \boldsymbol{j} \end{bmatrix} \qquad (1)$$

The matrices $\boldsymbol{a}$, $\boldsymbol{b}$, $\boldsymbol{c}$, $\boldsymbol{d}$ and $\boldsymbol{f}$ contain the transfer functions of the resistive multiport. From the definition of the excess elements, it follows that the sub-matrix linking the complementary variables of the excess elements is zero, and that the entries of the sub-matrices $\boldsymbol{d}$ and $\boldsymbol{f}$ are restricted to {-1, 0, 1}. For linear networks, the voltages $\boldsymbol{u}_C$ of the essential capacitors (or their charges) and the currents $\boldsymbol{i}_L$ of the essential inductors (or their fluxes) are chosen to form the state variable vector $\boldsymbol{x}=(\boldsymbol{u}_C,\ \boldsymbol{i}_L)^{\mathrm{T}}$. The parameters of the independent voltage and current sources form the input vector $\boldsymbol{y}=(\boldsymbol{e}\ ,\ \boldsymbol{j})^{\mathrm{T}}$. The equations of the essential and excess storage elements are:

$$\begin{bmatrix} \boldsymbol{i}_C \\ \boldsymbol{u}_{L'} \\ \boldsymbol{u}_{C'} \\ \boldsymbol{i}_{L'} \end{bmatrix} = \begin{bmatrix} \boldsymbol{C} & & & \\ & \boldsymbol{L} & & \\ & & \boldsymbol{C'} & \\ & & & \boldsymbol{L'} \end{bmatrix} \frac{\mathrm{d}}{\mathrm{d}\,t} \begin{bmatrix} \boldsymbol{u}_C \\ \boldsymbol{i}_L \\ \boldsymbol{i}_{C'} \\ \boldsymbol{u}_{L'} \end{bmatrix} = \begin{bmatrix} \boldsymbol{P} & \\ & \boldsymbol{P'} \end{bmatrix} \frac{\mathrm{d}}{\mathrm{d}\,t} \begin{bmatrix} \boldsymbol{u}_C \\ \boldsymbol{i}_L \\ \boldsymbol{i}_{C'} \\ \boldsymbol{u}_{L'} \end{bmatrix}. \qquad (2)$$

From relations (1, 2), the state equations of the circuit can readily be established:

$$\dot{\boldsymbol{x}} = \boldsymbol{A}\,\boldsymbol{x} + \boldsymbol{B}\,\boldsymbol{w}\,, \qquad (3)$$

where

$$\boldsymbol{A} = (\boldsymbol{P} - \boldsymbol{c}\boldsymbol{P'}\boldsymbol{d})^{-1}\boldsymbol{a} \qquad (4)$$

is the system coefficient matrix,

$$\boldsymbol{B} = (\boldsymbol{P} - \boldsymbol{c}\boldsymbol{P'}\boldsymbol{d})^{-1}\left[\boldsymbol{b} \quad \boldsymbol{c}\boldsymbol{P'}\,\boldsymbol{f}\right] \qquad (5)$$

is the input coefficient matrix, and

$$\boldsymbol{w} = \left[\boldsymbol{y} \quad \dot{\boldsymbol{y}}\right]^{\mathrm{T}} \qquad (6)$$

is the input vector. It is interesting to notice that for circuits with excess elements, the input vector of the state equations contains the parameters of the sources and their derivatives.

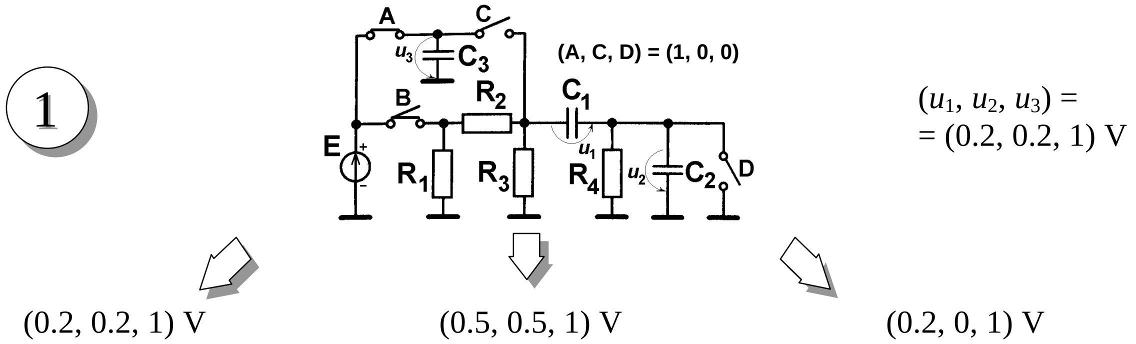
## 3. Switching as a process

Any process that is characterized by a sequence of elementary events can be considered to converge towards an instantaneous event as its overall duration tends to zero, if and only if the set of final states determined by all the permutations of the elementary events converges towards a unique well defined limit - the final state of the limit instantaneous event. Short processes can be arranged in classes. A class of switching processes is a set of equivalent switching paths, i.e., of paths that have the same initial and the same limit final state (characterized by the configuration of the switches and the values of the state variables, i.e., the IIC at $t = 0^-$ or the CIC at $t = 0^+$, respectively), despite the different order of the elementary switching events along each switching path. Two classes that start from the same initial state (characterized by the configuration of the switches and the IIC at $t = 0^-$) and arrive to the same final configuration of switches, but to different CIC at the moment $t = 0^+$ are distinct. A problem directly related to the problem (3) is to establish all the possible limit final states, i.e., all the distinct classes corresponding to the same initial state and to the same final configuration of switches.

Consider the idealized switched network shown in Fig. 1 for which in the initial phase 1, the ideal switches A and B are in state *ON* (1), while the ideal switches C and D are in the state *OFF* (0). Because switch B is not a part of a *C*-loop for any configuration of the switches, its state does not influence the initial conditions at $t = 0^+$, when given the initial conditions at $t = 0^-$. The state of the switches can be described by the relevant switch state vector (A, C, D), which is (1, 0, 0) in the initial phase. At the moment $t = 0$, a multiple switching occurs: all the switches change their states and the network passes in the phase 2, for which the relevant switch state vector is (0, 1, 1). In [2] the CIC at $t = 0^+$ are computed for the element parameters: $R_1$ = 1Ω, $R_2 = R_3 = R_4$ =2, $C_1 = C_2$ = 1F, $C_3$ = 3 F, $E$ = 1V, and the IIC at $t = 0^-$: $(u_1^{(1)}, u_2^{(1)}, u_3^{(1)}) = (0.2, 0.2, 1)$ V. Only one solution for the CIC at $t = 0^+$ is found in [2]: $u_1^{(2)} = u_3^{(2)} = 0.8$V, $u_2^{(2)} = 0$. In fact, the solution is not unique. Because there are *C*-loops that contain ideal switches, with zero resistance in the *ON* state, the switching can not be considered an instantaneous event. Disregarding how short the duration of the switching is, there are three distinct switching processes passing from 1 to 2, which result in different CIC at $t = 0^+$ as shown in Fig.1. Switching in practical *RC* circuits with very fast switches of nonzero *ON* resistance can often be modeled adequately by a process involving an intermediate state with all switches open - the relevant switch state vector (A, C, D) = (0, 0, 0) for the example - but in the case of *RL* circuits with finite *OFF* resistance, the complementary case (all switches closed) can better describe the real behavior of the circuit. The fact that the order of the individual switching events can change the state of the circuit at $t = 0^+$, for the same initial state at $t = 0$, rises the problem of the range of distinct transitions in an idealized switched circuit.

## 4. Distinct switching processes in an idealized switched circuit

Consider a circuit in which $n$ switches change state in the same multi-switching event. At the time scale of the processes that occur in the circuit between the successive multi-switching i.e., the scale of the time constants determined by the parameters of the other circuit elements besides the switches), the switching event is almost instantaneous. If the switches approach the ideal models, the duration of the switching process tends towards zero. As it has been shown in [9, 10], the order of the elementary events consisting in the change of the state of each individual switch can result in a different final state, even when the total duration of the multi-switching process approaches zero. If oscillating switching is ignored, there are $n$ elementary events that build-up the overall



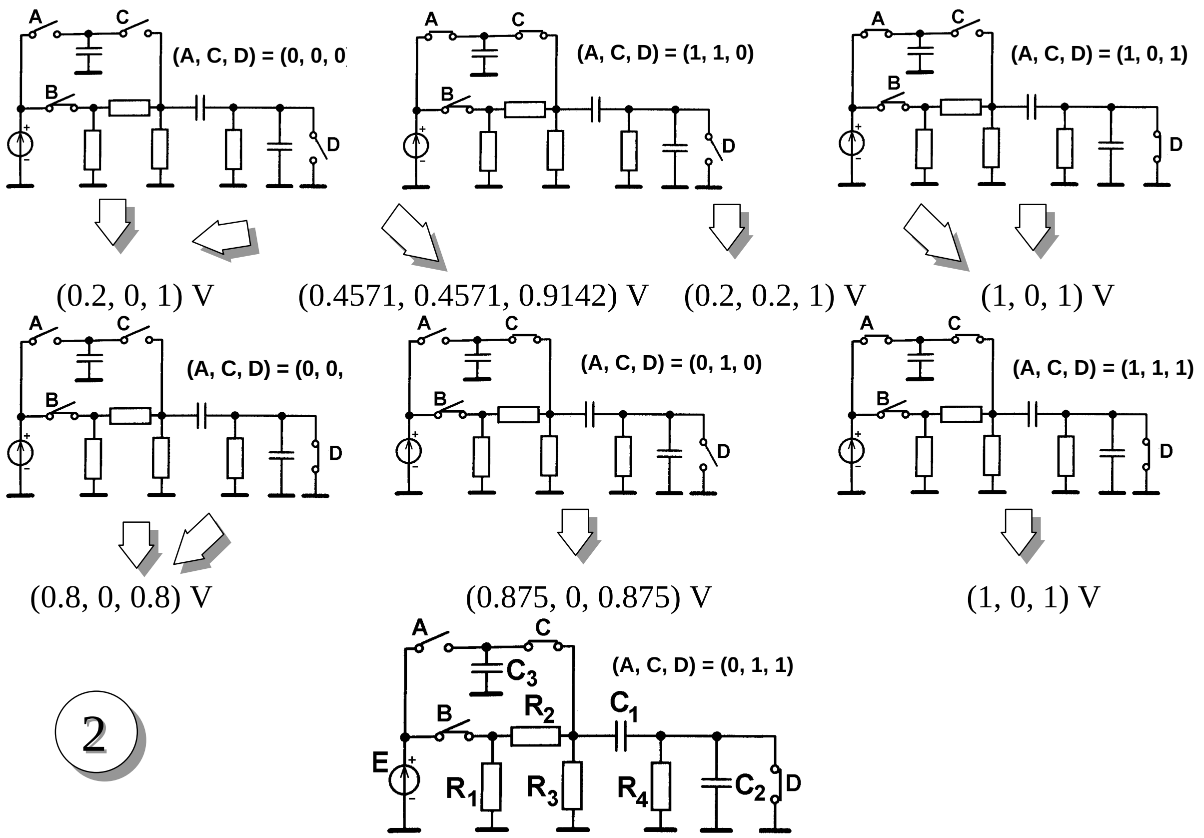



Fig. 1. Example of a switching process that can not be reduced to an instantaneous event

switching process. For the example network, there are n = 4 elementary switching events: the opening (transition from short-circuit to open-circuit) of switches A and B and the closing (the inverse transition, from open-circuit to short-circuit) of switches C and D. The duration of the intervals between the elementary switching events is irrelevant; only the order is significant. This allows the analysis of the network as an un-timed discrete event dynamic system (DEDS) in which the (partial) state is determined by the state of the switches. A Veitch–type map of the states can be used, like in Fig. 2, to represent the states of the switches and the transitions induced by the switching process. The standard denotation is used: the symbol $A$ (A = TRUE, or A=1) designates the state in which A is closed (short-circuited), while the symbol $\overline{A}$ designates the state when A is opened (open-circuit). The total number of switching states for the network in Fig. 1 is $2^n = 16$. The elementary transitions involve the change of state for one switch, and are represented by the edges of the graph in Fig. 2. The initial state, corresponding to the phase 1 is represented by the node 1 (A = B = 1, C = D = 0). The final state of the switching process, phase 2 of the network in Fig. 1, is represented by the node 2 (A = B = 0, C = D = 1). There is a total of $n! = 24$ permutations of the elementary switching events, giving as many possible switching processes, when passing from 1 to 2. But not all these processes lead to different CIC at $t = 0^+$.

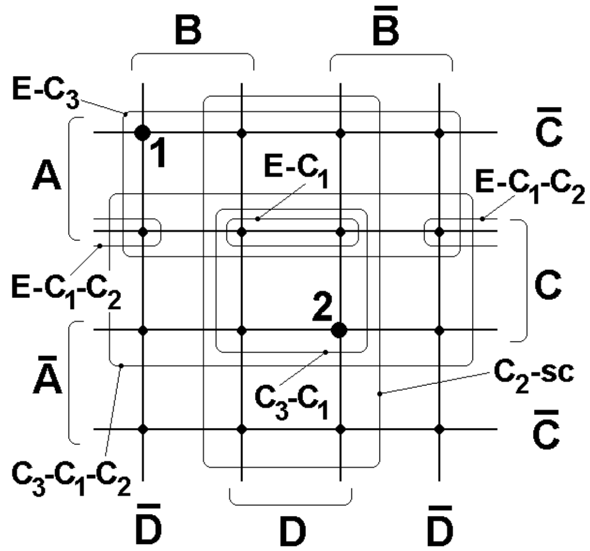



Fig. 2. Switch state Veitch diagram for network in Fig.1

Actually, it turns out that there are only three distinct classes of switching processes. The state variable values change after an elementary switching event, if and only if the configuration of the *C*-loops and/or of the *L*-cut-sets changes, so that different restrictions are imposed on the state variables [9]. One can identify such changes by using the *C-E* and *L-J* graphs of the network. The *C-E* graph of a network is obtained by maintaining only the capacitors, the ideal independent voltage sources, and the ideal switches existing in the analyzed circuit, while replacing all the resistors and all the inductors with open circuits. The *C*-loops of the network are the loops of the *C-E* graph. Similarly, the

*L-J* graph of a network is obtained by maintaining only the inductors, the ideal independent current sources, and the ideal switches, while replacing all the resistors and all the capacitors with short-circuits. The *L*-cut-sets of the network are the cut-sets of the *L-J* graph.

For the network in Fig. 1, the corresponding *C-E* graph is given in Fig. 3.

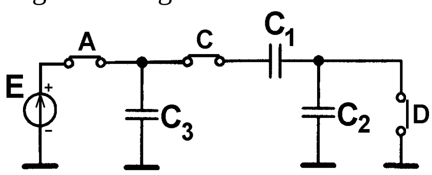



Fig. 3. The *C-E* graph of the network in Fig.1

The *C*-loops of the circuit in Fig. 1 and the states of the switches for which the loops are established are shown in the table. The first three loops can be chosen as a set of independent loops.

| *C-loops* | *State of the switches* |
|---|---|
| $E$-$C_3$ | A = 1 |
| $C_3$-$C_1$-$C_2$ | C = 1 |
| $C_2$-sc | D = 1 |
| $C_3$-$C_1$ | C = 1, D = 1 |
| $E$-$C_1$ | A = 1, C = 1, D = 1 |
| $E$ -$C_1$-$C_2$ | A = 1, C = 1, D = 0 |

The table below summarizes the construction of *C-E* loops and of *L-J* cut-sets.

| | Resistors | Capacitors | Inductors |
|---|---|---|---|
| *C-E* graph | o.c. | maintained | o.c. |
| *L-J* graph | s.c | s.c. | maintained |
| | Ideal voltage sources | Ideal current sources | Switches |
| *C-E* graph | Maintained | o.c | maintained |
| *L-J* graph | s.c. | maintained | maintained |

The state of the switch B is not relevant for the process of switching, as it does not affect the configuration of the *C*-loops. As a consequence, the reduced switching map in Fig. 4 can readily be obtained, by taking into account only the states of the three other switches.

The analysis of the changes in the restrictions imposed on the variables of the excess storage

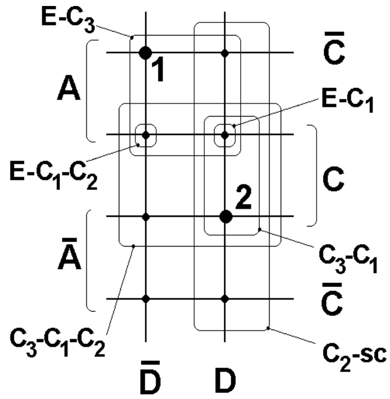



Fig. 4. Reduced switch state Veitch diagram for the network in Fig.1

elements (only capacitors for the considered example network) is performed by using this reduced Veitch diagram. One identifies the passages of the switching paths from one cluster of switching states - corresponding to a certain *C*-loop (or *L*-cut-set), to another cluster of switching states - corresponding to a distinct *C*-loop (or *L*-cut-set). This allows finding the changes of the restrictions on the circuit state variables, i.e., the classes of switching paths that lead to distinct CIC at $t = 0^+$. It can be seen from this diagram that the total of 3! = 6 possible switching processes fall into only three distinct classes from the point of view of the restrictions imposed on the voltages of the capacitors.

## 5. Conclusions

It has been shown that an ideal multiple-switching event, consisting of the almost simultaneous change of state of several ideal switches in a network with excess elements, can not be considered as an instantaneous event. In certain conditions, such a switching must be described as a process consisting of a sequence of elementary switching events. At the time scale of the processes that occur in the circuit from one switching to the next, the multiple-switching event is of negligible duration, but the order of the elementary single-switches still determines the final state, even when the total duration of the multiple-switching event approaches zero. The total number of distinct final states at $t = 0^+$ is usually much lower than it would result from the number of permutations of the elementary switching events. The distinct classes of the switching paths are determined only by the change of the restrictions imposed on the capacitor voltages by the configuration of the *C*-loops, respectively on the inductor currents – by the configuration of the *L*-cut-sets. The scanning of the independent switching process classes can be done using the discrete event system approach.

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