

# Current-Starved Pseudo-Floating Gate Amplifier

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**Abstract:** In this paper we present a 2 input analog Current-Starved Pseudo-Floating Gate (CSPFG) inverter with capacitive feedback. The analog CSPFG inverter suppresses low frequencies due to the active, local feedback. This inverter can be used in designing filters where a narrow band pass or reject is the main goal. Typical applications are detection of high frequency components in sensor signals, i.e. airbag sensors. AC simulation of the inverter is presented to show that the circuit is suited for high performance filter design. Linearity simulations of 2 input analog CSPFG inverters shows the good transient properties suited for inverter design.

**Key-Words:** CMOS, Floating gate, Inverter, Amplifier, Analog

## 1 Introduction

Since the birth of transistors and analog electronics, many techniques have been presented to improve the analog amplifiers and circuits, these improvements include power consumption, accuracy, noise, bandwidth and speed. Examples are Switch cap [1], Auto-Zero Amplifiers(AZA) [2], chopper-stabilized amplifiers [3] and in some extend neuromorphic electronics [4]. These systems often use a digital clock as a tool to achieve these improvements. In this paper we present a new type of amplifier based on Pseudo-Floating Gate (PFG)[5] inverter [6]. These amplifiers are purely analog, high speed and power conservative. The first analog Circuit based on PFG was a band pass filter presented by Y. Berg et al [7]. The filter was designed using CSPFG inverters. One important property of that filter was that the pass area could vary simply by changing a few bias voltages.

In section 2 we present more detailed simulation results of a 2 input analog CSPFG inverter. Section 2.1 covers the transient properties of the analog CSPFG inverter. The gain and linearity of the inverter is discussed. In section 2.2 AC simulations of the analog CSPFG inverter is shown and discussed. In section 3 a band pass amplifier is presented. In this filter we have implemented the 2 input analog CSPFG inverter to improve its properties. In section 3.1 the AC simulation results are shown. Section 3.2 discusses the effect of the 2 input analog CSPFG inverter on the amplifier gain. Section 4 concludes the work presented in this paper. The simulations presented in this paper are being done in the cadence environment

with 90 nm CMOS transistor models from the AMS with a VDD equal 1.2 volts and threshold voltage of 0.25volts.

## 2 2 input analog CSPFG inverter

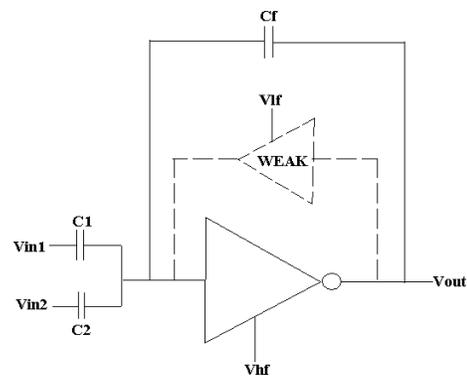


Figure 1: 2 input analog CSPFG inverter

The 2 input analog CSPFG inverter is shown in figure 1. This circuit is an inverter with a weak positive feedback. The positive feedback circuitry is basically a current starved inverter where the PMOS transistors are connected between the output and GND and the NMOS transistors between output and VDD, the opposite of the inverter. This positive feedback has 2 important functions in the circuit, it sets the operational point (DC level) of the circuit and it decides the lower cutoff frequency. Bias voltages on Vhf and Vlf limit the current flowing through the inverter

and the feedback circuitry respectively. Input capacitances, C1 and C2, block DC signals from the other circuitry connected to the inputs and make the circuit floating. C1 and C2 can also be used for weighting the input [8] signals compared to each other simply by choosing the right values. The gain of the circuit can be adjusted by changing the value of the feedback capacitor, Cf.

## 2.1 Transient response

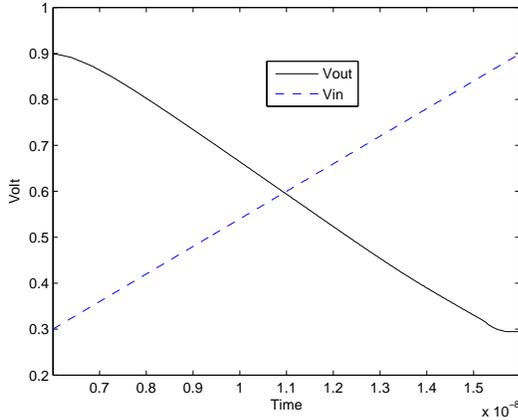


Figure 2: *Transient response of the analog CSPFG inverter*

Figure 2 shows the transient response of the 2 input analog CSPFG inverter. In this simulation the voltage on vhf is set to 0.42V and Vlf 0.40V. The inputs Vin1 and Vin2 are shorted and swept from 0.3 to 0.9 volts in a time period of 10ns (50MHz). The solid line represents the circuit response and the dashed line the input stimuli. The time delay of the circuit is neglected because the aim of this simulation is the voltage response of the circuit. The time delay of the circuit is not constant because of its dependent on the bias voltage, Vhf. This is discussed in more details in section 3.1. From the figure we see that the circuit has a linear response in the range 0.3 to 0.9 volts and flats out for voltages above and below this region. The operating voltage (dc level) of the circuit is  $VDD/2$ , where the 2 lines cross.

Figure 3 shows the linearity of the amplifier. This graph is the derivate of the output voltage divided by the derivate of the input voltage. The negative sign is due to the circuits inverting property. We can see that the Gain is increasing until the input is ca 0.4 volts. Then the circuit is linear until 0.8 volts where the Gain is decreased again. Between 0.5 volts and 0.7 volts we have an almost flat area.

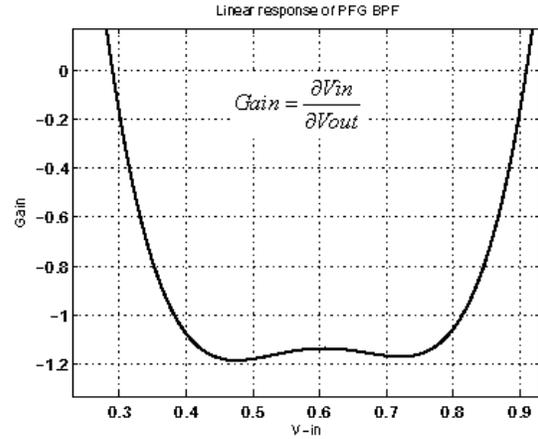


Figure 3: *The gain of the analog CSPFG inverter*

## 2.2 AC response

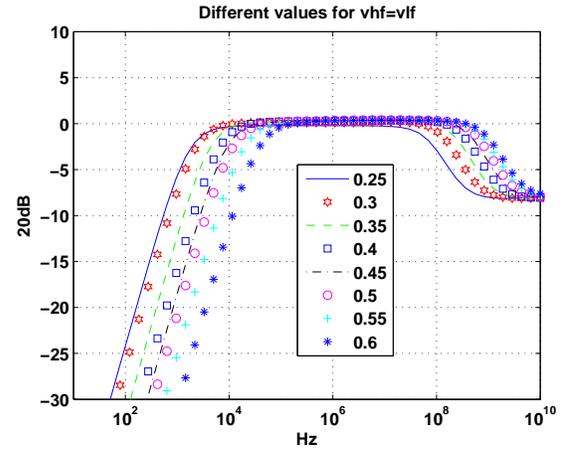


Figure 4: *The AC response of the analog CSPFG inverter for different values of Vhf, assuming  $Vlf = Vhf$*

Figure 4 Shows the AC response of the 2 input analog CSPFG amplifier when the bias voltages, Vhf and Vlf are varied from 0.25 to 0.6 volts simultaneous. We can see that the forwarding inverter suppresses high frequencies depending on the value of Vhf, but it can operate on frequencies as high as 800 MHz. The positive feedback suppresses low frequencies based on the voltage on Vlf. The lowest frequencies that can pass are as low as 3 KHz. We can estimate the cutoff frequencies by using simple transistor models and assuming that the starving transistor operates in the linear region:

$$f_{max} \approx \frac{\beta_{wb} V_{hfeffective}^2}{2C_l VDD} \quad (1)$$

where  $V_{hfeffective} = Vhf - Vt$ . A reasonable

value for the forward limiting current is 10uA yielding a max frequency of approximately 800MHz for  $C1 = 5fF$  and  $VDD = 1.2$ .

### 3 CSPFG Band pass amplifier

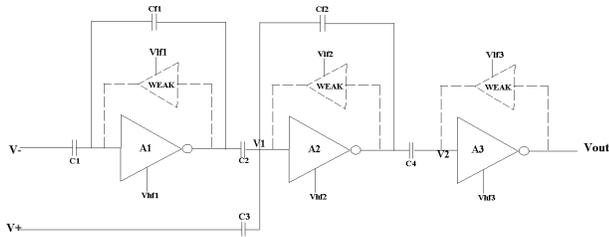


Figure 5: Differential CSPFG amplifier

The differential CSPFG amplifier shown in figure 5 becomes a single input band pass filter simply by connecting the 2 inputs,  $V+$  and  $V-$  together. The input signal goes through 2 branches, the first branch is  $C1$ , the CSPFG amplifier  $A1$  and  $C2$ , the other branch is  $C3$ . These branches are once again connected to each other at  $V1$ . The amplifier  $A1$  determines the lowest cutoff frequency of the filter by inverting all the signals in its pass band. The result is attenuation of the signal at  $V1$  and a signal equal to the input signal for frequencies higher than the pass band. The amplifier  $A3$  determines the highest cutoff frequency. The bias voltages  $Vhf_1$  and  $Vhf_3$  can be used to change the bandwidth of the filter as they change the highest cutoff frequencies of the  $A1$  and  $A3$  respectively. The amplifier  $A2$  is used to increase the gain of the filter. We may express the cutoff frequencies as:

$$f_{max} \approx \frac{\beta_{Wb} V_{hf3}^2}{2C_1 VDD} \quad (2)$$

$$f_{min} \approx \frac{\beta_{Wb} V_{hf1}^2}{2C_1 VDD} \quad (3)$$

The frequency width is

$$f_{width} \approx \frac{V_{hf3}^2}{V_{hf1}^2} \quad (4)$$

#### 3.1 AC response

Figure 6 shows the AC response of the filter shown in figure 5. In this simulation we have tested the circuits' AC response for various voltages on  $Vhf_1$ .  $Vhf_2$  is biased as  $Vhf_1$  and  $Vhf_3$  is biased 20 mV larger than  $Vhf_1$ . The legend box in the figure lists the  $Vhf_1$  values, increasing from 250mV to 600mV with a step of 50mV.

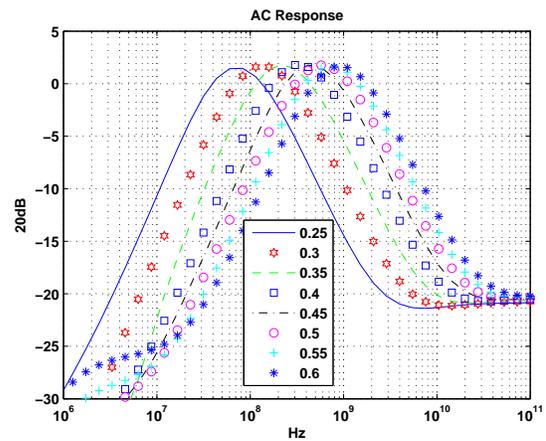


Figure 6: Band pass simulation of the CSPFG amplifier for different values on  $Vhf_1$ , assuming that  $Vhf_3 = Vhf_1 + 20mV$

#### 3.2 Transient response

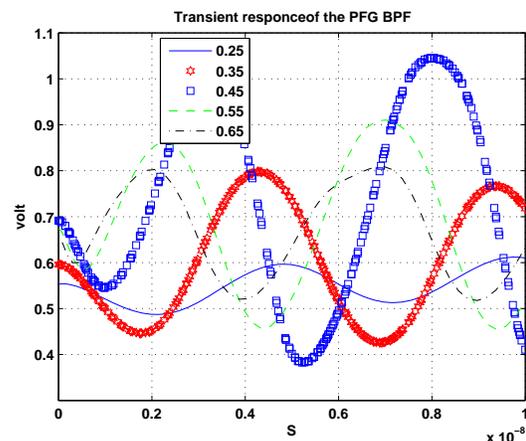


Figure 7: Time delay simulation of the CSPFG amplifier for different values on  $Vhf_1$ , assuming that  $Vhf_3 = Vhf_1 + 20mV$

In figure 7 we see the circuits' response to a sinusoidal signal with a frequency of 200 MHz and amplitude of 300 mV. It is easy to see that the filter suppresses the sinus wave for biases other than 450mV. The blue line (boxes) is the output result when the voltage on  $Vhf_1$  is 450mV (in the pass area according to figure 6). A phase shift is also observed for each bias voltage. The phase shift increases as the bias voltage  $Vhf$  is lowered. Another phenomenon that is observed is that the DC level of the signal is changing due to changes in the bias voltages  $Vhf_3$ . This is more likely caused by the unmatched transistors in the

analog CSPFG inverter. The DC level change has no effect on the operation of the circuit due to the capacitive coupling between each CSPFG amplifier and can be neglected.

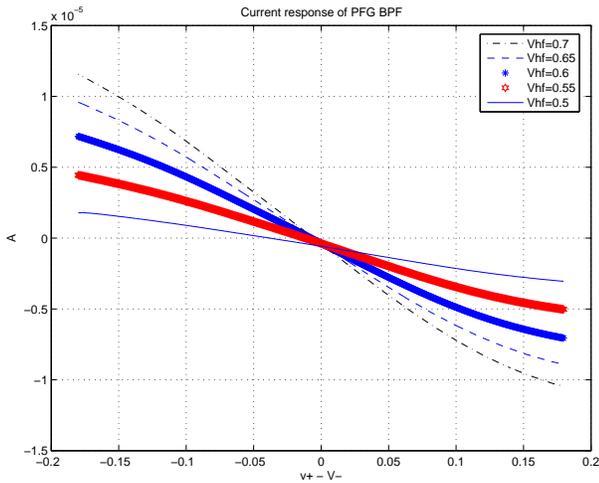


Figure 8: The output current of the CSPFG amplifier for different values on  $V_{hf1}$ , assuming that  $V_{hf3} = V_{hf1} + 20mV$

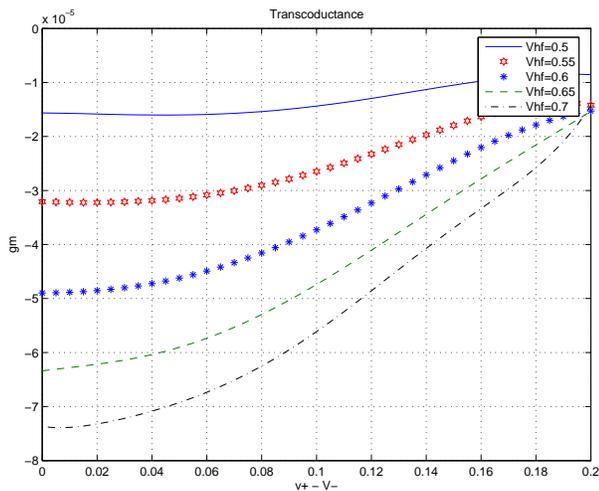


Figure 9: The Transconductance of the CSPFG amplifier for different values of  $V_{hf1}$ , assuming that  $V_{hf3} = V_{hf1} + 20mV$

Figure 8 shows the output current of the amplifier for different values  $V_{hf}$ . The current exhibit a tanh shape for large input values and a sinh shape for small inputs. In this figure we see the effect of the 2 input analog CSPFG inverter on the Filter compared to the filter published in [5] as increasing gain. This can also be observed in the transconductance of the CSPFG amplifier shown in Figure 9. The transconductance

has increased from  $2 \times 10^{-7} gm$  to  $5 \times 10^{-5} gm$  for  $V_{hf1} = 0.6V$ . The combination of sinh and tanh shaped output current is evident, and the linear region is determined by  $V_{hf1}$  and  $V_{hf3}$ . We can observe that the linear range for  $V_{hf1} = 0.6V$  and  $V_{hf3} = 0.58V$ , assuming 3% distortion, is close to  $160mV$  ( $80mV$ ).

## 4 Conclusion

The CSPFG amplifier presented in this paper is useful in application where a narrow band is to be detected. One important area is detecting frequency in resonating sensors. Other good properties of the CSPFG filters are simplicity and versatility. The ability to choose pass area simply using a few bias voltages allows tuning even after production and installation.

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