Hierarchical Symbolic Analysis of Analog Circuits Using Two-Port Networks

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Abstract: This paper presents a method towards hierarchical symbolic analysis of linear analog circuits using two-port networks. The important difference to the ordinary flat symbolic analysis is, that we treat the transistor pairs as blocks and then derive the transfer function with network analyzer without to setup and solve a complicated DAE system for a whole analog circuit. The hierarchical idea can be even used to large circuits in divide and conquer manner. Experimental results obtained with some applications of this method are presented.

Key–Words: Symbolic analysis, Two-port network

1 Introduction

Symbolic analysis have been developed to help designer get a better understanding of circuit behaviors using the symbolic expressions for the circuit performances in dependence of design parameters. This technique is quite mature in analysis of linear circuits, especially in the small-signal analysis with differential algebraic equations (DAE). The DAE system can be transformed in frequency domain and furthermore yields the transfer function, with which certain performances and stability of circuits can be easily derived [1]. The common rational expression of transfer function is shown below

$$H(s) = \frac{\sum_{i=0}^{M} a_i s^i}{\sum_{j=0}^{N} b_j s^j} \tag{1}$$

Up to now several symbolic simulators [2] [3] were developed: 1) ISAAC [4], ASAP [5],SYNAP [6] and Insydes [7] which are based on the node equations of circuits and applied to small circuits. 2) RAINIER [8] used the simplification before or during generation technique to deal with more complicated circuits. 3) Hierarchical approaches [9] [10] [11] made the analysis of larger circuits possible with different algorithms.

In this paper a new hierarchical symbolic analysis approach is presented. It combines the two-port network theory and the hierarchical representation of analog circuits with transistor pairs together to achieve a symbolic analysis without to setup and solve differential-algebraic equations (DAE) for the whole analog circuit. The results have exact the same accuracy as the common symbolic analysis. The hierarchical idea can be even used to large circuits in divide and conquer manner.

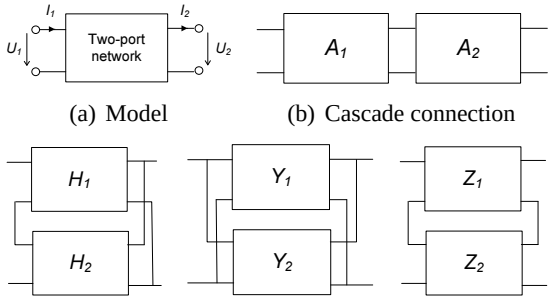
The paper is organized as follows. Section II provides the foundational knowledge of two-port network. In section III the previous work about hierarchical representation of analog circuits is described. Section IV focuses on the hierarchical symbolic method. Section V presents experimental results, and finally conclusions are drawn.

2 Two-Port Network Analyzer

A two-port network is a circuit with two pairs of terminals and represented by four external variables: voltage and current at the input and output port, so that the two-port network can be treated as a black box modeled by the the relationships between the four variables. In this paper we use the model with output current arrow pointed away from network (Fig. 1(a)). There are several types of matrices used to describe a two-port network [13] [14]. Of particular interest of this paper are the A-, H- , Y- and Z-matrices.

The A-matrix, also known as chain or transmission matrix, is used in the cascade connection of two networks shown in Fig. 1(b). The A-matrix of the connected networks is given by the product of their A-matrices as:

$$A_{total} = A_1 \cdot A_2 \tag{2}$$



(a) Model (b) Cascade connection

(c) Hybrid connection (d) Parallel connection (e) Series connection

Figure 1: Two-port network analyzer

In the hybrid connection of two networks it is better to use the H-matrix as illustrated in Fig. 1(c). We express the H-matrix of connected networks as

$$H_{total} = H_1 + H_2 \tag{3}$$

In the parallel connection of two networks (Fig. 1(d)) the Y-matrix can be used to express them with

$$Y_{total} = Y_1 + Y_2 \tag{4}$$

The Z-matrix can be used in the series connection of two networks depicted in Fig. 1(e). The connected networks exhibit a Z-matrix as

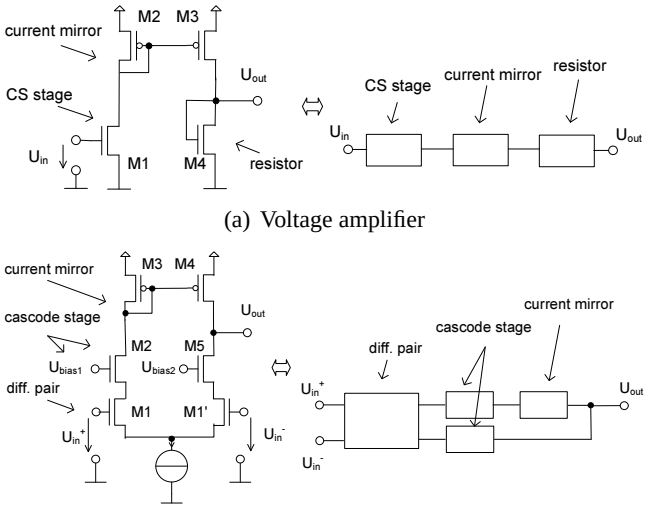
$$Z_{total} = Z_1 + Z_2 \tag{5}$$

3 Previous Work

One approach to topology synthesis of analog circuits [12] provides the idea, that a circuit topology can be represented by a block-chain in one dimension or a block-net in two dimensions, which is a connection of several blocks and each block represents a netlist of a single transistor or a transistor pair, such as differential pair, cascode stage, current mirror, etc. Its advantage is that the signal flow of analog circuit can be expressed in the flow of block-chain or block-net, generally from left to right.

Two example circuits are given in Fig. 2. The first circuits is a single input voltage amplifier built with common-source stage, current mirror and a transistor with connected gate and drain, which operates as a small-signal resistor. At the right of Fig. 2(a) is the corresponding block representation of this circuit. The other example is a cascode op amp with four different blocks as shown in Fig. 2(b).

Our approach is based on this hierarchical representation idea, which can be connected with two-port network in order to enable the hierarchical symbolic analysis.



(a) Voltage amplifier

(b) Cascode op amp

Figure 2: Hierarchical representation method

4 Hierarchical Symbolic Analysis

We develop a new symbolic method with following features:

- It can be applied to small/medium circuits without to setup and solve the complicated DAE system for a whole circuit, yet with the exact results as the flat symbolic analysis.
- It can be also applied to large circuits in divide and conquer manner.
- It is easy to be implemented in Maple, Mathematica even in C++, since no complicated symbolic algebra operation is needed.

The method mentioned in Section 3 provides the idea, that we can derive the transfer function of a circuit from its block-chain/block-net. The two-port network theory maintains the interaction between electrical connections, for example, the current feedback for voltage signal connections for the blocks in Fig. 2(a). Hence our method is able to do an accurate symbolic analysis in a hierarchical way.

In our method the A-matrix defined as

$$\begin{bmatrix} U_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{bmatrix} \begin{bmatrix} U_2 \\ I_2 \end{bmatrix} \tag{6}$$

with the model in Fig. 1(a) is one of the standard matrices mentioned in Section 2. Since the hierarchical block representation of analog circuits is generally cascade connection of blocks as illustrated in Fig. 2, we prefer to use the A-matrix. In the following subsections we discuss the calculation of an A-matrix and the derivation of the transfer function of a whole circuit from blocks.

4.1 A-matrix

The blocks containing few transistors, such as differential pair and current mirror, are the building blocks of circuits. In order to be convenient for the definition of two-port network, one terminal connected to ground is added to each side of the blocks defined in Section 3 except for the differential pair. Then we can compute the A-matrix of each block using flat symbolic analysis and save them in a user-defined A-matrix library. Especially we can put structural and matching informations into the A-matrix, e.g. in differential pair two transistor have the same size, therefore they have the same design parameters.

The next step is to calculate the whole A-matrix for a given analog circuit. We study three cases, which we may meet in calculation step.

- *Cascade connection*: the easiest case is that two blocks are cascade connected as shown in Fig. 3(a). The equation for the whole A-matrix A_{12} is

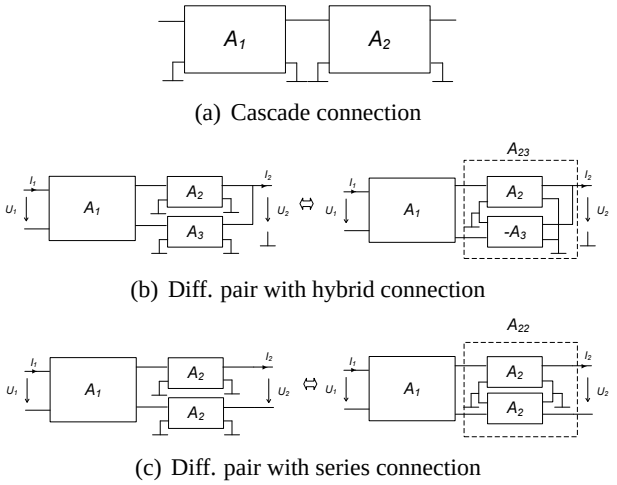
$$A_{1,2} = A_1 \cdot A_2 \tag{7}$$

- *Diff. pair with hybrid connection*: Circuits containing differential pair make the calculation complicated. A special connection is illustrated in Fig. 3(b). The differential pair A_1 has symmetric structure with two inputs and outputs can be combined with two other blocks A_2, A_3 separately and independently, whose outputs can build a common output terminal. For the simplification, block A_2 and A_3 are treated together as one block A_{23}. Recognizing that the connection between A_2 and A_3 is similar to the hybrid connection in Fig. 1(c), we interchange the two inputs and get a negative A-matrix $-A_3$. Hence we get the following:

$$\begin{aligned} A_{2,3} &= f_{hy}(A_2, A_3) \\ &= \mathit{HtoA}(\mathit{AtoH}(A_2) + \mathit{AtoH}(-A_3)) \\ &= \begin{bmatrix} \frac{K - det(A_2) - det(A_3)}{a_{3,22} - a_{2,22}} & \frac{a_{2,12}a_{3,22} + a_{2,22}a_{3,12}}{a_{3,22} - a_{2,22}} \\ \frac{a_{2,21}a_{3,22} + a_{2,22}a_{3,21}}{a_{3,22} - a_{2,22}} & \frac{a_{2,22}a_{3,22}}{a_{3,22} - a_{2,22}} \end{bmatrix} \end{aligned} \tag{8}$$

where *AtoH, HtoA* are the translation functions from A-matrix to H-matrix or vice versa and $K = a_{2,11}a_{3,22} + a_{2,12}a_{3,21} + a_{2,21}a_{3,12} + a_{2,22}a_{3,11}$. Thus, the A-matrix for the whole system can be written as:

$$A_{1,2,3} = A_1 \cdot f_{hy}(A_2, A_3) \tag{9}$$



(a) Cascade connection

(b) Diff. pair with hybrid connection

(c) Diff. pair with series connection

Figure 3: Calculation of the A-matrix

- *Diff. pair with series connection*: Another case with differential pair is illustrated in Fig. 3(c). The differential pair A_1 can be combined with two identical blocks A_2, whose outputs can build differential voltage output terminals. The identical A_2 can ensure that the output of this system is a symmetrical differential signal to fit the definition of two-port network. For the simplification, two block A_2 are treated together as one block A_{22}. Recognizing that the connection between two blocks is similar to series connection in Fig. 1(e), we interchange the two inputs and outputs of the lower block and get a same A-matrix A_2. So, we get following:

$$\begin{aligned} A_{2,2} &= f_{se}(A_2) \\ &= \mathit{ZtoA}(\mathit{AtoZ}(A_2) + \mathit{AtoZ}(A_2)) \\ &= \begin{bmatrix} a_{2,11} & 2a_{2,12} \\ 0.5a_{2,21} & a_{2,22} \end{bmatrix} \end{aligned} \tag{10}$$

where *AtoZ, ZtoA* are the translation functions from A-matrix to Z-matrix or vice versa. Thus, the A-matrix for the whole system can be written as:

$$A_{1,2,2} = A_1 \cdot f_{se}(A_2) \tag{11}$$

4.2 Transfer function

A symbolic formula of the transfer function can be easily derived from an A-matrix. If a two-port network is loaded with Z_L, the voltage transfer function can be expressed as:

$$H(s) = \frac{U_2(s)}{U_1(s)} = \frac{1}{a_{11} + \frac{a_{12}}{Z_L}} \tag{12}$$

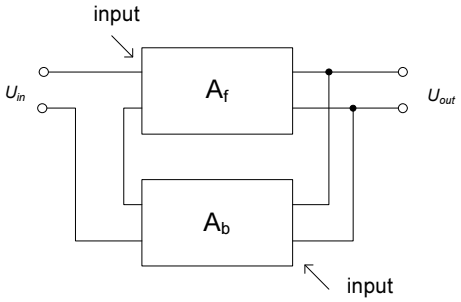


Figure 4: Voltage-voltage feedback

Furthermore, the linear performances of a circuit, such as DC gain, GBW, phase margin, and input/output impedance, can be derived from the A-matrix.

4.3 Feedback

Considering often occurred feedback in analog circuits, the A-Matrix can be also combined with the feedback theory in [15]. There are generally four feedback topologies. We demonstrate here one topology, and other topologies can be derived in a similar way.

The concept of voltage-voltage feedback is illustrated in Fig. 4 with one feedforward network A_f and one feedback network A_b. Please note the inputs of two networks. We can therefore write voltage gain of two networks as $\frac{1}{a_{f,11}}$ and $\frac{1}{a_{b,11}}$, respectively. And hence:

$$\frac{U_{out}}{U_{in}} = \frac{\frac{1}{a_{f,11}}}{1 + \frac{1}{a_{b,11}}\frac{1}{a_{f,11}}} \tag{13}$$

4.4 Divide and conquer

The ideal of hierarchical symbolic analysis can be even used for large circuits in divide and conquer manner. When a circuit can be divided into several sub-circuits in form of cascade, hybrid or series connection, the two-port network theory can be applied to analyze the circuit. Furthermore, if the sub-circuits can be split into several blocks, we can analyze a complete large circuit using hierarchical symbolic analysis without dealing with a large DAE system. Considering a huge A-matrix for the exact analysis and the limitation of symbolic expression in programming, the simplification of a matrix described in [16] by eliminating insignificant terms can be applied.

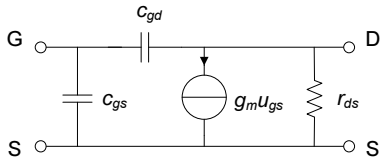


Figure 5: MOS transistor small-signal model

5 Results

In this section we will present the analysis results for some real circuits. The A-matrix library is built, extend and maintained by user. Once an unknown block with few devices is found, its A-matrix should be calculated and saved in library. The basic size of such a library is between 20-30 blocks for fundamental analog blocks. We used a PC with a 3GHz processor to implement this method in Maple.

Example 1: The single input voltage amplifier (Fig. 2(a)) is built with three cascade connected blocks. We used a simple small-signal MOS Transistor model shown in Fig. 5 to do the calculation. Thus we have the A-matrix for the whole circuit:

$$A_{total} = A_{CS} \cdot A_{CM} \cdot A_R \tag{14}$$

For this circuit, the run time for exact A-matrix calculation is in 0.04 CPU seconds. Because of limited space we present only the DC-gain A_{DC} of this amplifier without load. From (12) we have:

$$\begin{aligned} A_{DC} &= H(s=0) = \frac{1}{a_{11,total}(s=0)} \\ &= (r_{ds1}r_{ds2}r_{ds3}r_{ds4}g_{m1}g_{m3})/(r_{ds1}r_{ds3} + r_{ds2}r_{ds4} \\ &\quad + r_{ds1}r_{ds4} + r_{ds2}r_{ds3} + r_{ds2}r_{ds3}r_{ds4}g_{m4} \\ &\quad + r_{ds1}r_{ds2}r_{ds3}g_{m2} + r_{ds1}r_{ds2}r_{ds3}r_{ds4}g_{m2}g_{m4} \\ &\quad + r_{ds1}r_{ds2}r_{ds4}g_{m2} + r_{ds1}r_{ds3}r_{ds4}g_{m4}) \\ &\approx \frac{g_{m1}g_{m3}}{g_{m2}g_{m4}} \text{ if } r_{ds} \to \infty \end{aligned} \tag{15}$$

Example 2: The cascode op amp (Fig. 2(b)) contains a differential pair, whose block representation is not a simple linear cascade connection. Using the function described in (8) we have:

$$A_{total} = A_{Diff} \cdot f_{hy}(A_{Cas} \cdot A_{CM}, A_{Cas}) \tag{16}$$

and we got the exact symbolic expression of A-matrix within 1.8 seconds. The $a_{11,total}$ contains more than 500 symbolic terms. The simplification was done after generation. We allowed 1.2% error for each term of

the A-matrix. (12) and (16) leads to the simplified transfer function with load impedance Z_L:

$$H = \frac{0.5(g_{m3}+g_{m4})g_{m1}}{\frac{g_{m3}}{r_{ds4}} + \frac{g_{m3}}{Z_L} + (g_{m3}c_{gd4} + c_{gd4}g_{m4} + c_{gd5}g_{m3})s} \tag{17}$$

Example 3: A low-voltage op amp with output buffer containing 16 transistors is shown in Fig. 6. It can be generally divided into three parts A_I, A_{II} and A_{III} with total of 10 blocks. The connection between part A_{II} and A_{III} is the same as the parallel connection in (4). Each part contained several blocks. With the detailed partition illustrated in Fig. 6(b), we have:

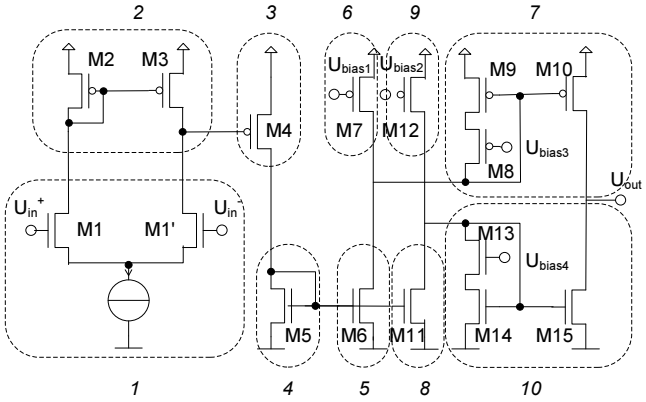
$$\begin{aligned} A_I &= A_{1,2,3,4} = A_1 \cdot f_{hy}(A_2, I_2) \cdot A_3 \cdot A_4 \\ A_{II} &= A_{5,6,7} = A_5 \cdot A_6 \cdot A_7 \\ A_{III} &= A_{8,9,10} = A_8 \cdot A_9 \cdot A_{10} \\ A_{II,III} &= \mathit{YtoA}(\mathit{AtoY}(A_{II}) + \mathit{AtoY}(A_{III})) \\ A_{total} &= A_I \cdot A_{II,III} \end{aligned} \tag{18}$$

where I_2 is 2×2 identity matrix, which denotes the A-matrix for a piece of wire. Functions *AtoY*, *YtoA* are the translation functions from A-matrix to Y-matrix or vice versa.

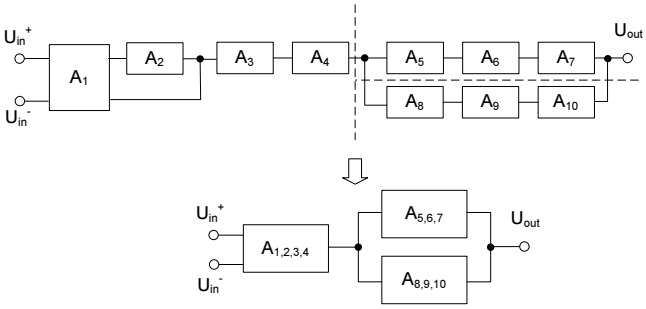
The exact symbolic expression of $A_{II,III}$ was simplified with an error margin of 2% before multiplication with A_I. Such simplifiction is done during generation (SDG) in the late step to ensure a higher accuracy. The final expression of A_{total} with more than 2300 product terms was obtained in 0.6 seconds. We allowed 3% error to calculate the approximated poles of transfer function (without load). One pole is expressed as:

$$\begin{aligned} p_1 = & \frac{g_{m14}g_{m9}(r_{ds15}+r_{ds10})}{r_{ds15}r_{ds10}(g_{m14}c_{gd10}g_{m10} + g_{m14}c_{gd10}g_{m9} \\ & + g_{m9}c_{gd15}g_{m15} + g_{m9}c_{gd15}g_{m14})} \end{aligned} \tag{19}$$

A comparison between the common flat symbolic analysis and our method for above mentioned three examples is shown in Table 1. Because they have the same accuracy, we compare them with the run time to calculate the A-matrix. The simplification before generation (SBG) [17] was used to reduce the complexity of common symbolic analysis for the third example, which is more complicated than the simplification we used.



(a) Schematic and its partition



(b) Block-net

Figure 6: Low-voltage op amp with output buffer

Table 1: Comparison of run time

	Ex. 1	Ex. 2	Ex. 3
symbolic analysis without simplification	0.16s	3.7s	-
symbolic analysis with simplification	-	-	8.8s 5%
hierarchical method without simplification	0.04s	1.8s	-
hierarchical method with simplification	-	-	0.6s 2%

6 Conclusions

We have presented a new hierarchical way to do symbolic analysis of small analog circuits, as well as large circuits. It uses the interaction feature of two-port network theory and the hierarchical representation of circuits with blocks. In our approach we do not need to set up a DAE system for a whole circuit or deal with a high dimensional matrix to solve the DAE system. All matrices are in 2×2, therefore the complexity and run time of calculation can be reduced. In addition to being able to handle large circuits, the simplification can be applied well controlled during the hierarchical evaluation process enabling a good runtime/accuracy trade-off. We have successfully demonstrated three

applications.

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