Design and Optimization of ÷8/9 Divider in PLL Frequency Synthesizer with Dynamic Logic (E_TSPC)

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Abstract-Selection of dynamic dividers in CMOS PLLs for GHzs applications allows remarkable reduction in power loss without affecting phase noise and power supply sensitivity. Frequency dividers are combination of classic TSPC logic (true-single-phase-clock) and E_TSPC logic (extended TSPC). The designed PLL with % 8/9 prescaler is used for wireless LAN applications and synthetic of frequencies between 5.14 to 5.70 GHz. In this paper a % 8/9 prescaler has designed at 0.25 micrometers process for 2.5_3 GHz band width. This prescaler has been designed with 2.5*v* power supply with using E_TSPC logic. In this circuit in addition to decrement of power consumption, divider can work in a nearly high speed. Subsequently the dimensions of transistors have been improved and power consumption has been reduced from 3.8*mw* to 2.9*mw*. Then, the layout of circuit has been designed with L-Edit software. The simulation results of are identical to that we expect according to earlier Spice simulations.

Key Words- Dynamic logic, Frequency divider, Low power E-TSPC, TSPC, Frequency synthesizer, Hyper LAN, Wireless LAN.

1 Introduction

Wireless LAN systems at 5-6 GHz band like *Hyper-LAN II* and *802.11a IEEE* are known as successful standards for high rate transmission of information[1]. A frequency synthesizer which is usually realized by a PLL is one of the crucial blocks in average current losses, because this block is frequently used as a transmitter and receiver.

Basically, the most power loss is related to the primary layers of frequency divider that consumes half of the total power. Because of the high input frequency in prime layer, the divider can not be realized by conventional static CMOS logic [1]. Instead, it is generally realized by source-coupled-logic (SCL) that allows execute in higher frequency but with higher power consumption in practical circuits.

Dynamic latches are more lumped and quicker than static ones. By designing with TSPC, it will be possible to activate dynamic latch with a single phase clock hence there will no problems related to skew [2]. Anyway, selection of these latches at frequency dividers, restricts the PLL frequency to 900MHz [3],[4].

Employing dynamic logic not only can allow work till 60GHz, but also is extremely effective in power loss reduction in synthesizers. Using this type of divider neither increases phase noise nor effectively decreases performance of PLL 0[1].

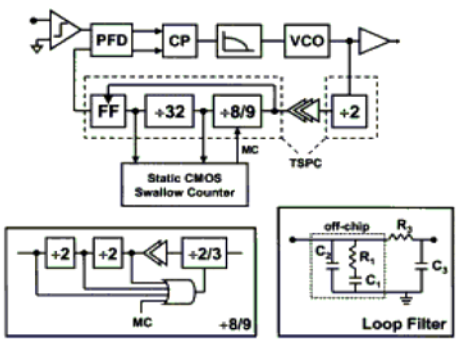

Fig. 1.. Block diagram of frequency synthesizer, *÷ 8/9 prescaler topology and filter*

2 Structure of synthesizer

Fig. 1 shows the block diagram of under-discussion frequency synthesizer. The programmable divider uses the pulse swallow structure in feedback path. Blocks that are surrounded by dotted lines in Fig.1 are realized by TSPC logic while swallow counter realized by static CMOS logic. The most crucial block in programmable divider is *"÷ 8/9 prescaler"* which structure has been shown in Fig.1. ÷2 divider

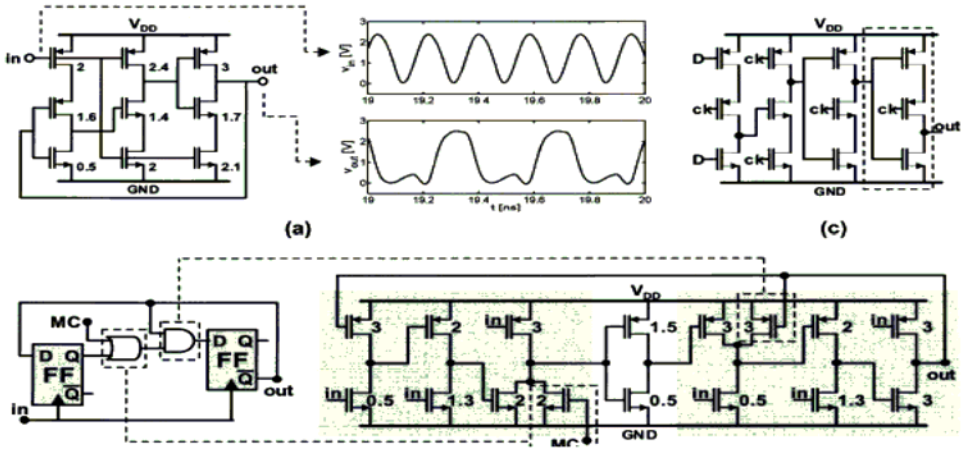

Fig. 2. A power divider with TSPC logic
(a) Simulated output of ÷2 divider, (b) Schematic diagram of a ÷2/3 divider, (c) Power divider

is directly connected to VCO output and after that ÷ *8/9-prescaler* and *÷32 program counter* are connected sequentially. A TSPC logic flip-flap (FF) performs the task of synchronization of the output of programmable divider with output of the first divider. This FF passes over the time jitter that is related to ÷8/9 prescaler and ÷32 program counter [5]. Three cascade reversers with CMOS logic -placed from beginning to end- is connected after the first ÷2 divider to drive synchronizer FF and ÷8/9 prescaler.

3 Dynamic Frequency Divider

The advantage of dynamic logic in comparison common SCL logic, is less power loss because in dynamic logic, capacitor loads are decreased. One ÷2 divider in SCL logic is realized by 18 transistors. In SCL logic, while designing of its layout, even with a much possible precision, the capacitor noises of middle contacts are greater than that in input capacitors of transistors. So, it needs one buffer between VCO and SCL divider which increases the power loss [6].

A power divider with TSPC logic has been shown in Fig. 2-a. The divider only includes 9 transistors. So the number of middle contacts between them significantly decreases in comparison to SCL divider. Since capacitors of intermediate connections became smaller in each transistor, we can minimize the W/L to decrease the power loss. For this reason, our dynamic divider is used as a first divider stage in PLL and all of transistors have their minimum length (0.25 micrometers). Width of the transistors (at micrometer) is shown in Fig. 2-a. Fig. 2-a, in addition, depicts the simulated output of ÷2 divider for mentioned VCO output in *5.4 GH* frequency. To

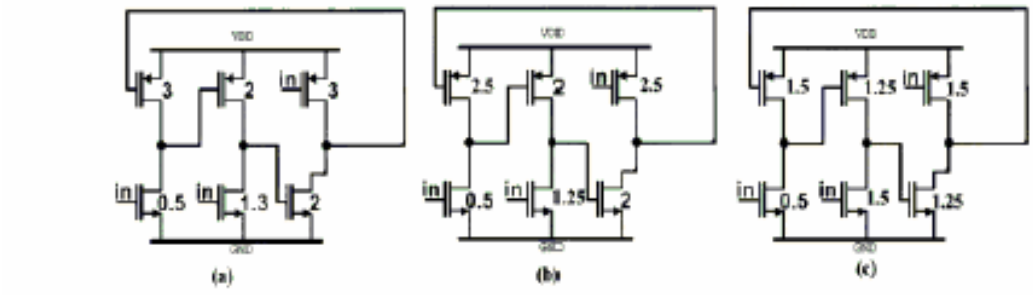

Fig. 3. *E-TSPC* logic *÷2* dividers concerning to ÷8/9 prescaler
(a) Unimproved divider, (b) Improvement of second divider, (c) Improvement of third divider

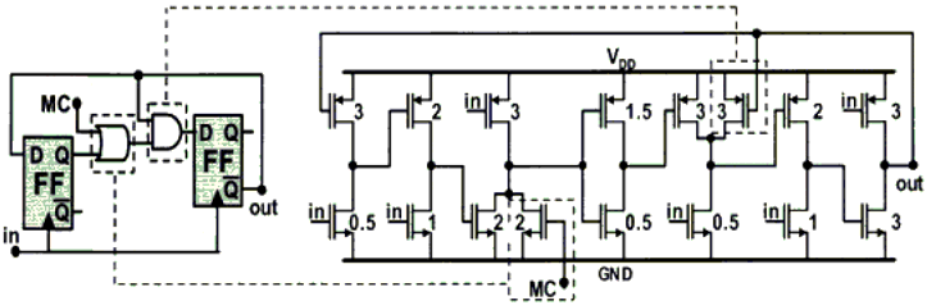

Fig.4. Improved ÷2/3 divider

drive the ÷8/9 prescaler and the final synchronized stage, output of ÷2 divider has connected to three CMOS logic reverser that have located sequentially from beginning to the end.

÷8/9 prescaler has includes one ÷2/3 synchronized divider and two ÷2 asynchronized divider (see Fig. 1). In [1] the ÷2 and ÷2/3 dividers have been re-implemented using TSPC logic E_TSPC logic, respectively. Fig. 2-b shows a schematic diagram of a ÷2/3 divider where width of transistors has been illustrated in micrometers. Since the structure of *stacked MOS* reduces the speed of switching in E_TSPC logic -in spite of classic TSPC logic- stacked MOS structure is avoided. Also the effects of body do not appear in any transistors because Vsb becomes zero. Although the E_TSPC logic shows static power loss, according to mentioned reasons E_TSPC logic allows working in higher frequencies. This static power loss causes small increase in power loss, because at mentioned frequencies dynamic power loss is dominant to power loss of stationary current.

Thus, E_TSPC logic permits to place complex functions at latches which leads to implement very complicated circuits and causes decrease in number of transistors. This concept is employed in designing of ÷2/3 dividers where OR and AND gates are implemented by just one transistor. On the other hand, in *E-TSPC* logic there is no problem related to *glitch* which is an important bottleneck in classic TSPC [7].

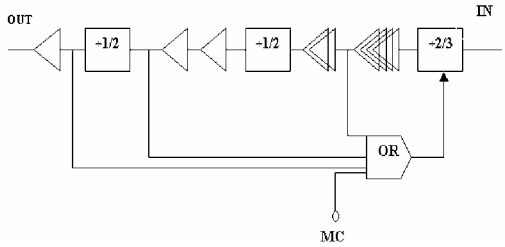

Fig. 5. Block diagram of ÷8/9 prescaler after improvement

To design a E_TSPC logic ÷2 divider for ÷8/9 prescaler block, at first, we design ÷2 divider using first part of [1] and size of transistors used in ÷2/3 divider introduced there. It is observable that power of ÷8/9 prescaler increases by 1.8 mw. Then to decrease of power loss, width of transistors in ÷2 and ÷2/3 dividers is is possible decreased to necessary dimensions. In the third step, we insert some reversers in the circuit. Now, power consumption is decreased by 0.9 mw. In the improved circuit, ÷2 divider which previously could not perform dividing for input frequencies lower than 2.2 *GH*, can execute that task suitably. Of course, this advantage is achieved despite of increasing power consumption to 1 *mw*.

The VCO's output frequency firstly is divided by 2 and secondly is divided by 2 or 3. Then it enters a ÷2 divider which is less than 2.2 *GH* according to aforesaid frequency reductions. So, we designed second and third ÷2 dividers by E_TSPC logic to ÷8/9-prescaler can do frequency dividing correctly for its input 2.5-3 *GHz* frequencies (*5-6* GHz input frequency to first stage of ÷2 divider after VCO). Fig. 3 illustrates width of transistors in both improved and unimproved ÷2 divider at E_TSPC logic and Fig. 4, shoes width of transistor in improved ÷2/3 divider in micrometers. Finally, in Fig. 5 block diagram of improved ÷8/9 prescaler is shown.

4 Simulation Results

To verify the results of this paper, firstly we simulated the primary plan of circuit using *Hspice* software. In that primary plan the *MC* input voltage is separated to two 1/8 and 1/9 dividers. In this case, according to the dimensions of unimproved ÷2

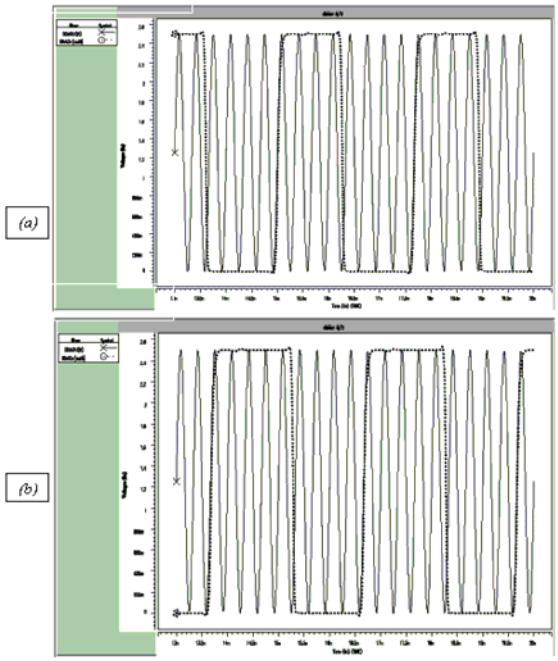

Fig. 6. The output of improved ÷8/9 prescaler for a *3 GHz* input
(a) MC=2.5 v "1/8", (b) MC=0 v "1/9"

divider that are mentioned before, the power consumption of ÷8/9 prescaler is equal to 3.8 mw.

For improvement of power, we should omit the input capacitor loads of input transistors, then we should reduce loading effect of transistors between the stages; finally we should to exchange or decrease the high-consumption elements of circuit.

Adding some reversers to circuit and decrement of key transistor's dimensions could be handle abovementioned problems. Therefore, we reduced width of some transistors so that the relation of *1/8* for *MC=2.5 v* and the relation of *1/9* for *MC= 0 v* is preserved at the frequency range of *2.5_3 GHz*. Width of transistors in reversers has been considered about *0.5 um*)

Power consumption is reduced to 2.9 mw by reduction of transistor's dimensions. The diagram of circuit analysis with improved dimensions is illustrated in Fig. 6. To draw the layout of improved circuit, after drawing and performing *DRC* (analysis of design roles and correcting problem) we extract a *SPICE* file as circuit Layout. The layout of circuit is shown in Fig. 7.

It is necessary to explain that the minimum amount of transistor's width is considered as *w= 0.25 um* and the *0.25* micrometer technology has been used. Then we simulated the spice file extracted from layout that

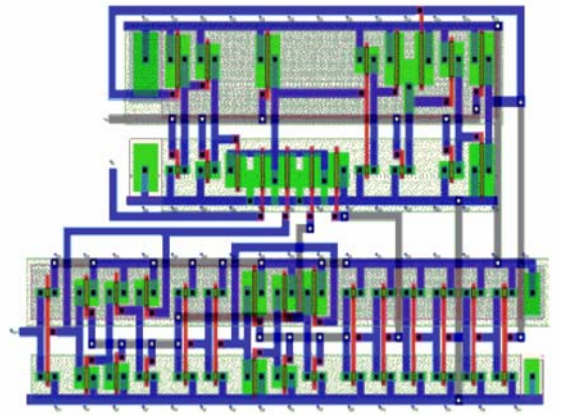

Fig. 7. layout of improved circuit

the results of simulation was exactly equal to that in improved spice file.

5 Conclusions

A ÷8/9-prescaler can not perform the dividing tast at low input frequencies. Using dynamic E_TSPC logic ÷2 divider in structure of ÷8/9- prescaler, in, we could perform dividing thas. Employing E_TSPC logic causes increase in speed of switching while not appearing effects of body at circuit transistors. Finally, at this logic there is not any problems concerning to glitch that is a major problem in ordinary TSPC.

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