Control of Three-Phase Pulse Width Modulation Voltage Rectifier

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Abstract: - In this paper, we develop an algorithm to control the input currents of three-phase voltage PWM rectifier in ABC frame. We start by elaborating knowledge and control models of this converter using Petri nets. Then, an algebraic modulation strategy using the triangular-sinusoidal with two carriers is presented. The digital simulation results show the performances of the network currents control with a unit power-factor.

Key-Words: - Petri nets, PWM, Buck rectifier, Algebraic modulation, voltage control, Unity power factor, Network.

1 Introduction

The power quality problem has interested many studies. Harmonics in transmission systems have attracted engineers attention even before the advent of thyristors [1]. In the modern power electronics era, the concern on harmonic problems is increasing. This is mainly spurred by the incessant proliferation of power electronic equipments as nonlinear loads, such as diode rectifiers.

One of effective methodologies to handle harmonic problems is to use another electronic system. Among representative approaches are the active power filter and the PWM rectifiers. The latter is the approach of interest in this paper.

A great amount of work has already been done concerning the three phases PWM boost rectifier and the buck rectifier [2-3].

The three-phase PWM buck converter, with six-step, provides adjustable DC output voltage and sinusoidal input currents with no low-frequency harmonics [4-5-6]. However, the switching frequency harmonics contained in the input currents must be eliminated by the input filter, which produces a phase shift between the line frequency components of the input currents and input voltages [4].

This paper presents a new control algorithm which provides output voltage regulation with line input currents and input voltages in phase.

A control loop, designed by considering only output filter dynamics, is employed for output voltage regulation. The line input currents are controlled through control loop of input filter. This algorithm assures a unity power factor at the network side. In the following sections, a power stage topology of the converter, operating principle and control model are described. Then, a new algebraic PWM strategy for the three-phase source voltage rectifier is developed. A steady dynamic modelling and representative results of circuit simulations are presented.

2 Converter Modelling

2.1 Knowledge model

A circuit diagram of the three-phase buck converter is shown in Fig. 1. The rectifier consists of six switches (diode - transistor) TDki commendable with the opening and closing, where the indices k=1, 2, 3 are the order of the phase and i = 1, 0 are respectively the upper and lower switches of the bridge.

The two current sources are connected via a parallel capacitor. Practically, however, the available ac source is a voltage source; accordingly, the ac current must be a series combination of an ac voltage source and inductor (Fig.1). The LC network between the ac voltage source and the ac current source has a function

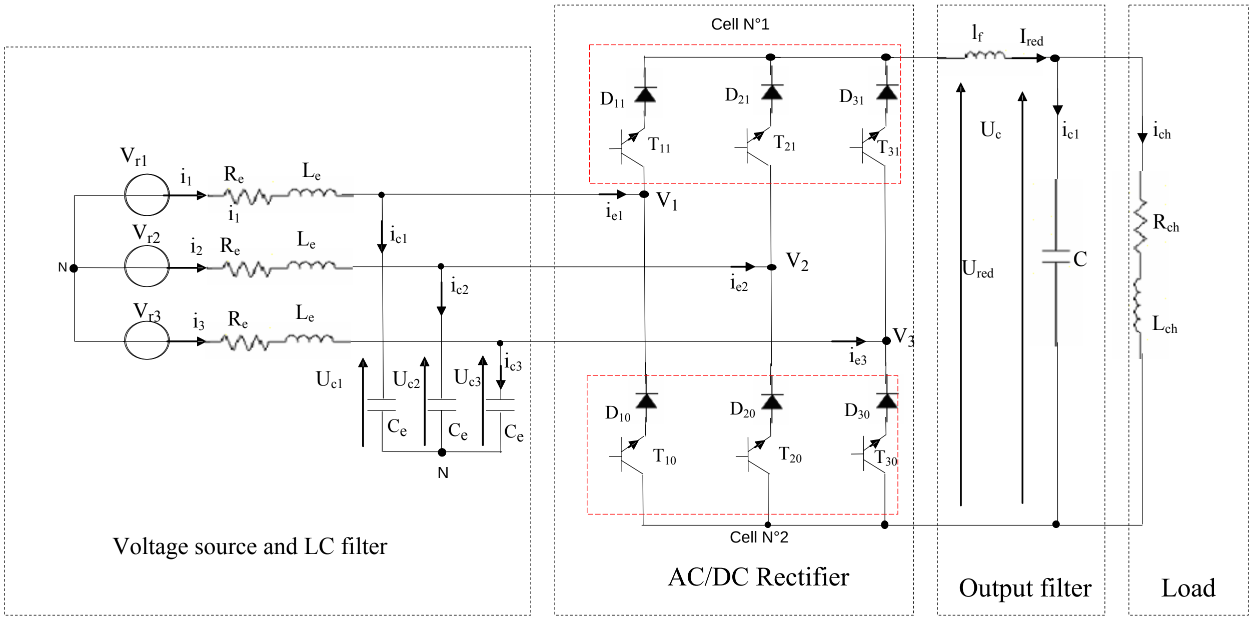

Fig. 1. Three-phase Buck rectifier structure

to filter output switching frequency components due to current chopping on the rectifier side [1-6-7].

A topology analysis of this structure shows two commutation cells (Fig.1) [5-6]. At any given instant, only one switch of the upper cell and one switch of the lower one of the bridge conducts, so that the input voltage source are never shorted, and a freewheeling path for the inductor current is always provided.

The symmetry of the three-phase rectifier allows its modelling by half bridge (cell N°1 or cell N°2)[5-7-8]. The transition receptivities Rij between the different configurations of the Petri nets associated to the working model of half Converter Bridge (Fig.2) are logic function between [5-6-9]:

1- External control B_{ki} of the switches

2- Internal control defined by the sign of the ac input voltages and rectified current.

The following equation: give the receptivity R_{ij}:

$$
\begin{aligned}
R_{01} &= (B_{1i} = 1 \,\&\, V_{1i} > 0);\\
R_{10} &= (B_{1i} = 0 \text{ or } I_{rect} = 0);\\
R_{02} &= (B_{2i} = 1 \,\&\, V_{2i} > 0);\\
R_{20} &= (B_{2i} = 0 \text{ or } I_{rect} = 0);\\
R_{03} &= (B_{3i} = 1 \,\&\, V_{3i} > 0);\\
R_{30} &= (B_{3i} = 0 \text{ or } I_{rect} = 0);
\end{aligned} \tag{1}
$$

$$
R_{12} = \begin{pmatrix} (B_{1i} = 0 \,\&\, B_{2i} = 1 \,\&\, I_{red} \neq 0) \\ \text{or} \\ (B_{2i} = 1 \,\&\, (V_2 - V_1) > 0 \,\&\, I_{red} \neq 0) \end{pmatrix}; \quad
R_{21} = \begin{pmatrix} (B_{2i} = 0 \,\&\, B_{1i} = 1 \,\&\, I_{red} \neq 0) \\ \text{or} \\ (B_{1i} = 1 \,\&\, (V_2 - V_1) < 0 \,\&\, I_{red} \neq 0) \end{pmatrix}; \tag{2}
$$

$$
R_{13} = \begin{pmatrix} (B_{1i} = 0 \,\&\, B_{3i} = 1 \,\&\, I_{red} \neq 0) \\ \text{or} \\ (B_{3i} = 1 \,\&\, (V_3 - V_1) > 0 \,\&\, I_{red} \neq 0) \end{pmatrix}; \quad
R_{31} = \begin{pmatrix} (B_{3i} = 0 \,\&\, B_{1i} = 1 \,\&\, I_{red} \neq 0) \\ \text{or} \\ (B_{1i} = 1 \,\&\, (V_3 - V_1) < 0 \,\&\, I_{red} \neq 0) \end{pmatrix}; \tag{3}
$$

$$
R_{23} = \begin{pmatrix} (B_{2i} = 0 \,\&\, B_{3i} = 1 \,\&\, I_{red} \neq 0) \\ \text{or} \\ (B_{3i} = 1 \,\&\, (V_3 - V_2) > 0 \,\&\, I_{red} \neq 0) \end{pmatrix}; \quad
R_{32} = \begin{pmatrix} (B_{3i} = 0 \,\&\, B_{2i} = 1 \,\&\, I_{red} \neq 0) \\ \text{or} \\ (B_{2i} = 1 \,\&\, (V_3 - V_2) < 0 \,\&\, I_{red} \neq 0) \end{pmatrix} \tag{4}
$$

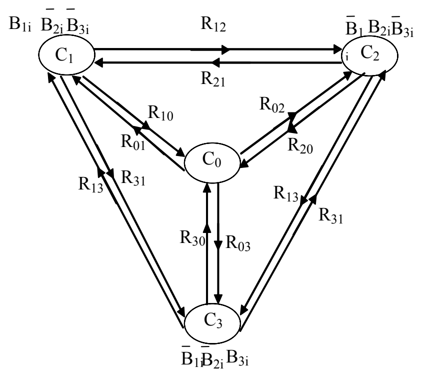

Fig.2. A Petri network of cell N° (1) of three-phase rectifier

2.1 Control model

In order to develop the model of rectifier without presumption on its control, we represent each pair Transistor-diode (T_{ki},D_{ki}) by a bi-directional switch TD_{ki}

In controlling mode, the optimal complementary law used for this converter is presented below:

$$B_{1i} + B_{2i} + B_{3i} = 1 \tag{4}$$

B_{ki}: control signal of the semiconductor T_{ki}

The switching functions of a switch T_{ki} in Fig.1 is defined as:

$$f_{ki}(t) = \begin{cases} 1, & TD_{ki} \text{ closed} \\ 0, & TD_{ki} \text{ open} \end{cases} \tag{5}$$

$$k \in \{1,2,3\}, \quad i \in \{1,0\}$$

Equation (4) can be expresses as

$$f_{1i} + f_{2i} + f_{3i} = 1 \tag{6}$$

Then, from Fig.1, the input currents are given by:

$$\begin{bmatrix} i_{e1} \\ i_{e2} \\ i_{e3} \end{bmatrix} = \begin{bmatrix} f_{11} - f_{10} \\ f_{21} - f_{20} \\ f_{31} - f_{30} \end{bmatrix} . I_{red} \tag{7}$$

While the output voltage Ured is:

$$U_{red} = \begin{bmatrix} (f_{11} - f_{10})\, U_{c1} + (f_{21} - f_{20})\, U_{c2} \\ + (f_{31} - f_{30})\, U_{c3} \end{bmatrix} \tag{8}$$

Where U_{c1}, U_{c2} and U_{c3} are capacitors input voltages.

At frequencies significantly below the switching frequency, operation of the circuit can be modelled by an average model. Thus, we define the generating function " X_g " of the discontinuous one "X", as the mean of "X" on a modulation period T_h supposed very small as follow[4-5-6]:

$$X_g = \left[\frac{1}{T_h} \int_0^{T_h} X \, dt \right] \tag{9}$$

The average model of three-phase rectifier, where all quantities are continuous, is given by the following equations with $\langle i_{e1} \rangle$, $\langle i_{e2} \rangle$ and $\langle i_{e3} \rangle$ representing the mean value of the instantaneous ones, and $(f_{ki})_g$ are generating connection function of each switches T_{ki}.

$$\begin{bmatrix} \langle i_{e1} \rangle \\ \langle i_{e2} \rangle \\ \langle i_{e3} \rangle \end{bmatrix} = \begin{bmatrix} (f_{11})_g - (f_{10})_g \\ (f_{21})_g - (f_{20})_g \\ (f_{31})_g - (f_{30})_g \end{bmatrix} I_{red} \tag{10}$$

And

$$\langle U_{red} \rangle = \begin{bmatrix} (f_{11})_g - (f_{10})_g \\ (f_{21})_g - (f_{20})_g \\ (f_{31})_g - (f_{30})_g \end{bmatrix}^T \begin{bmatrix} U_{c1} \\ U_{c2} \\ U_{c3} \end{bmatrix} \tag{11}$$

3 Algebraic PWM Strategy

Different Triangular-sinusoidal strategies could be achieved with digital mean by sampling reference signal i_{refk} such as:

$$i_{ref}[k] = I_{ref} \sqrt{2} \sin(\omega t - \frac{2\pi}{3}(k-1)) \tag{12}$$

With $\omega = 2.\pi f$ is the network pulsation and f is the network frequency.

In this paper, we develop a new digital PWM algorithm of three-phase buck rectifier dedicated for a digital realisation and obtained by using the control model developed previously[6-7]. The general flow chart of an algebraic PWM using this control model is presented in Fig.3. This strategy is characterised by modulation index m defined as a ratio between the frequency f_c of the carrier and the frequency of the reference signal ($m = f_c / f$), and amplitude modulation index (r) is the ratio of the reference signal magnitude and that of the carrier ($r = A_m / A_c$).

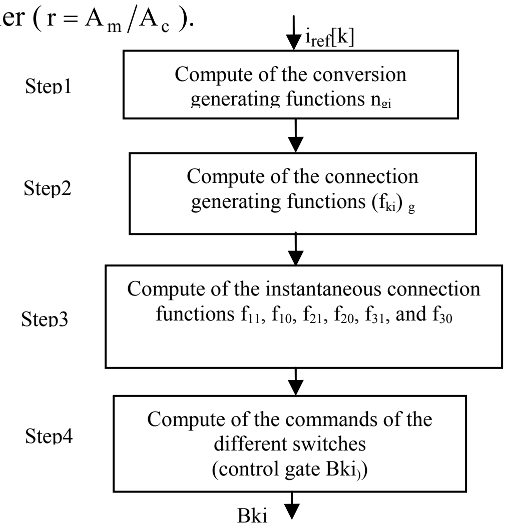

Fig. 3 The general of flow chart of an algebraic modulation using average model of the three-phase

This algorithm is based on the triangular-sinusoidal strategy with two carriers [10].The generating conversion functions ng_k are:

$$ng_k = \frac{i_{ref}[k]}{I_{red}}; \quad k = 1,2,3 \tag{13}$$

With I_{red} is the rectified current.

Fig. 4 represents the line input current of three-phase buck voltage rectifier controlled by the proposed algebraic modulation for m=30 and r=0.8.

The current harmonics gather by families centred around frequencies multiple of mf. The most important harmonics are (m±1) and (2.m±1) in view their magnitude (Fig. 4)

The adjusting characteristic is linear from r=0 to r_{max}= 1, and the total harmonics distortion (THD) decreases when r increases as is shown in Fig. 5

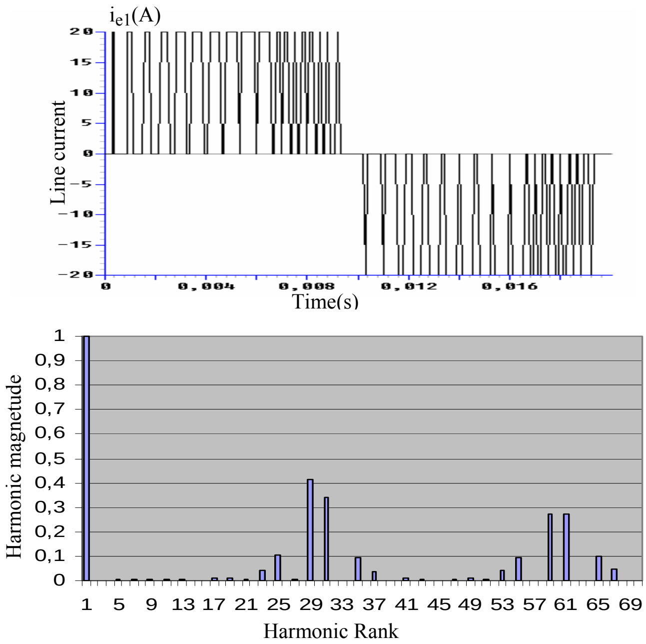

Fig. 4 The input line current of three-phase and its spectrum for Algebraic strategy control with m=30, r=0,8

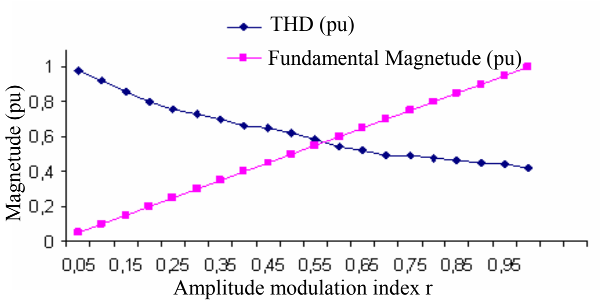

Fig.5 Adjusting characteristic of the input line current for Algebraic strategy with m=30

4 Converter Modelling

4.1 Input filter model

Due to discontinuous currents, the converter must be preceded by an input filter shown in Fig.1.

The input filter model is given by the following equations:

$$\begin{bmatrix} di_1/dt \\ di_2/dt \\ di_3/dt \end{bmatrix} = \frac{1}{L_e}\left(\begin{bmatrix} V_{r1} \\ V_{r2} \\ V_{r3} \end{bmatrix} - \begin{bmatrix} U_{c1} \\ U_{c2} \\ U_{c3} \end{bmatrix} - \begin{bmatrix} R_e & 0 & 0 \\ 0 & R_e & 0 \\ 0 & 0 & R_e \end{bmatrix} * \begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} \right) \quad (14)$$

$$\begin{bmatrix} dU_{c1}/dt \\ dU_{c2}/dt \\ dU_{c3}/dt \end{bmatrix} = \frac{1}{C_e}\left(\begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} * \begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} - \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} * \begin{bmatrix} i_{e1} \\ i_{e2} \\ i_{e3} \end{bmatrix} \right) \quad (15)$$

Where:

V_{rk}, i_k : source voltage and current (k=1, 2, 3),

U_{ck}, i_{ck} : capacitor voltage and current,

i_{ek} : Converter input current,

L_e, C_e : filter inductance and capacitance,

R_e : Line resistance,

The relationship between the rectifier input and output is given by (7).

4.2 Output filter model

The following equations describe the mathematical model of the output filter (Fig 1.)

$$\frac{dU_C}{dt} = \frac{i_c}{C} \quad (16)$$

$$i_{red} = i_c + i_{ch}$$

Where: U_c , i_c : capacitor voltage and current

I_{red} , i_{ch} : rectified and load current respectively.

C : output filter capacitance

We assume that losses in the converter and in the input filter are negligible. The relationship of the rectifier output and input is obtained by:

$$3\, V_{eff} I_{eff} \cos\varphi = I_{red} U_{red} = U_c I_{red} \quad (17)$$

With V_{eff}, I_{eff} : efficient source voltage and current of network,

φ: Phase shift between the line source current and corresponding phase voltage.

For a unit power-factor operation ($\cos\varphi \approx 1$), the equation (17) can be represented by the block diagram depicted in Fig 6

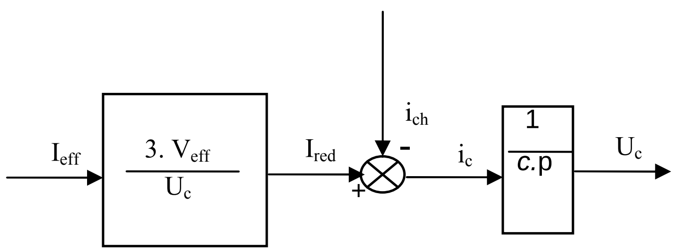

Fig. 6 Block diagram of the output filter model.

4.3 Circuit Simulation
For the PWM three-phase voltage rectifier, the magnitude of dc output voltage can be regulated either constant or variable. In this paper, we propose a new algorithm to control the output filter voltage (U_c) for constant reference value.
Fig 7 shows a control block diagram used in the simulation. Three-phase currents and dc voltage are sensed for the feedback control purposes.
Moreover, the load current i_{ch} is also measured and added to capacitance current to improve the dynamic response in the dc voltage control. Thus we obtain the input current magnitude reference of the rectifier.

- L_{ch}=0.1mH .
- switching frequency of the converter : fc=1500hz

Fig. 9 shows the dc output voltage of the rectifier following its reference. The rectified current oscillates around mean value because of the switching commutations. The Fig. 10 shows the input capacitor voltage filter which is sinusoidal and equal to its reference. However the effect of the rectifier switches commutations on the wave. In Fig. 11, it is compared the real input line current i_1 with its reference i^*_1. The network current follows the reference wave with good accuracy. It is closely sinusoidal.
shape is not eliminated.

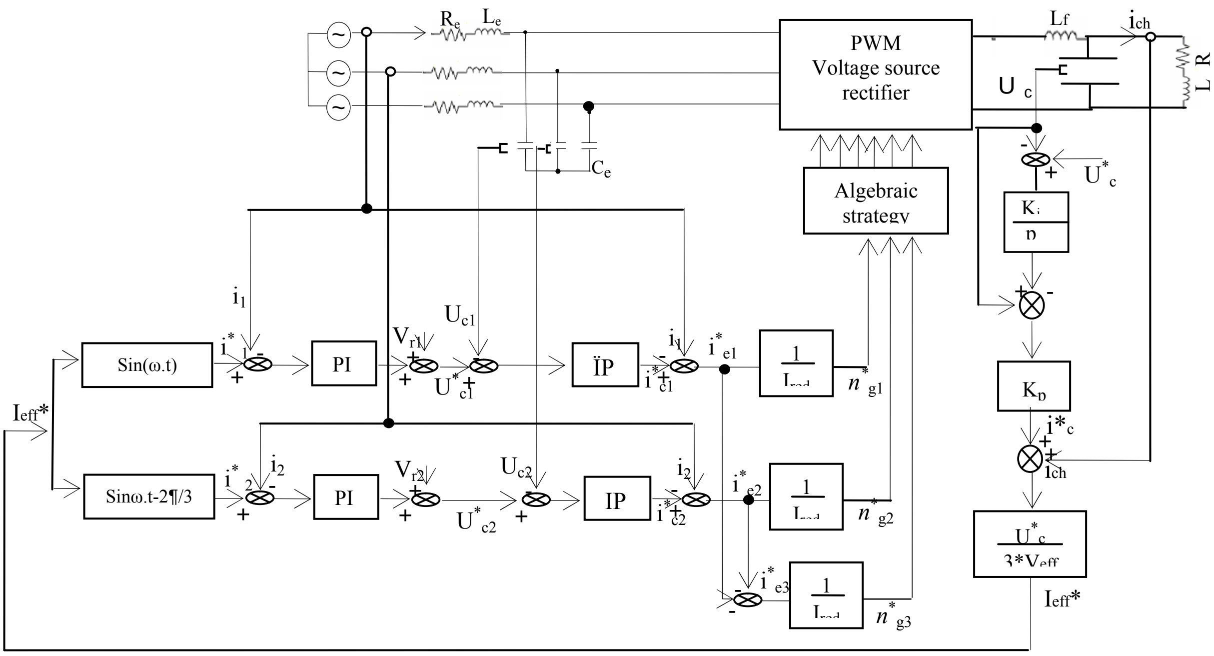

Fig. 8 Control block diagram of the rectifier

The later gives us the instantaneous input currents for the desired dc voltage. PI regulator is used for controlling the input current, and IP regulator to regulating the input capacitance voltage.

5 Simulation Results
To verify the validity of the proposed control scheme, simulations are carried out, with the parameters used as follows:

- line filter capacitor: c_e = 50µF ,
- line filter inductor : L_e = 1mH ,
- dc link inductor : l_f= 10 mH ,
- output filter capacitor: C =1mF ,
- load parameters: R_{ch} =20Ω ,

The input phase current and the corresponding input phase voltage are given by the Fig. 12. With this algorithm, the obtained power factor is nearly equal to 0.999.

6 Conclusion
An input filter is necessary for the three-phase PWM source voltage rectifiers to suppress the switching harmonics contained in the inputs currents. The inputs filter produce a phase shift between the line input currents and input voltages. The phase shift is caused by the input filter parallel capacitors. It varies with the load and with the magnitude of the input phase voltage. It can result in some operating conditions unacceptably low power factor.

In this paper, a new simple control algorithm for three-phase PWM source voltage rectifier with an input filter is proposed, which applies a multivariable state feedback control and feed forward control.
With the PWM converter, the source current can be sinusoidal and the unity power factor control is obtained. In addition, the input filter capacitor voltage is regulated so that the resonance between the LC filter can be avoided.
By using IP regulator, the control scheme of the PWM converter is directly applied to regulate the output dc voltage. The IP regulator is used for anti-saturation.
The simulation results confirm that the proposed overall control algorithm is effective.

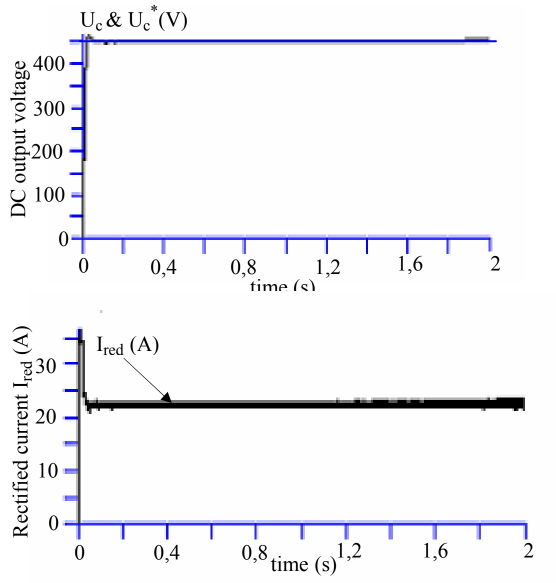

Fig. 9 The DC out put voltage and the rectified current for dc voltage reference U_c^*=450 V.

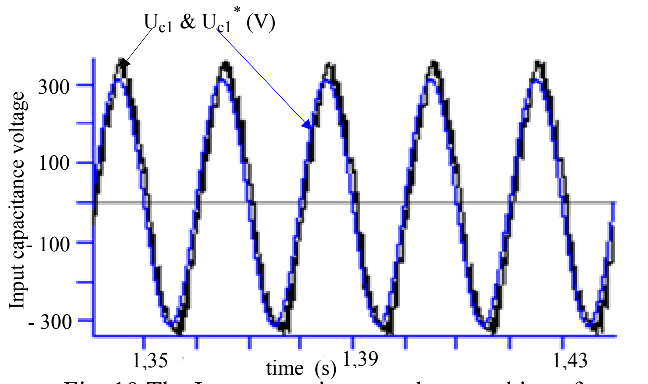

Fig. 10 The Input capacitance voltage and its reference

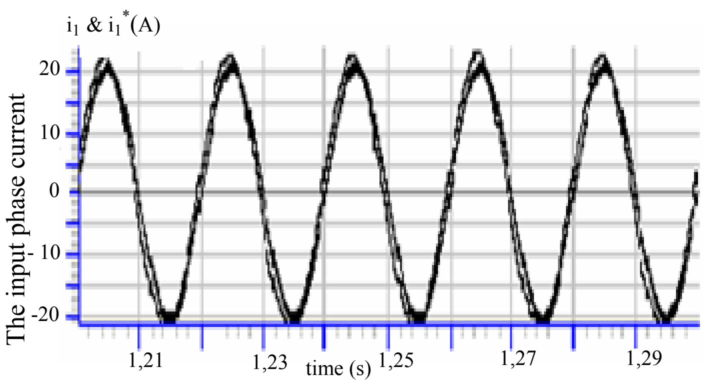

Fig. 11 The input phase current i_1 and its reference i^*_1

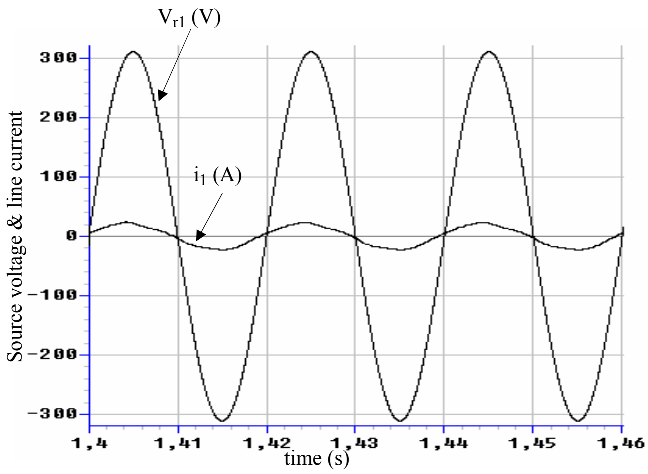

Fig. 12 Source voltage *and corresponding input* current

References:

[1] J. Kikuchi, T.A. Lipo, Three-phase PWM Boost – Buck rectifiers with power Regenerating Capability; *IEEE Tans, on Power Electronics,*,2001, pp: 308-315.

[2] V. Blasko and V. Kaura, A new mathematical model and control of three phase ac-dc voltage source converter, *IEEE Trans, on Power Electronics*, 1997, Vol. 12, No. 1, pp.116-123.

[3] A. Busse and J. Holtz, Multiloop control of a unity power factor switching ac to dc converter, *Conference proceedings of IEEE PESC* 82, 1982, pp. 171-179.

[4] S. Hiti, V. VlatkoviC, D. BorojeviC and C. Y. Lee, A New Control Algorithm for Three-Phase PWM Buck Rectifier with Input Displacement Factor Compensation, *IEEE Trans. on Power Electronics*, 1994, Vol. 9, No. 2,pp.173-178.

[5] T. G. Habetier, A space vector-based rectifier regulator for ac/dc/ac converters, *IEEE Trans. on Power Electronics*, 1993, Vol.8, No. 1, pp. 30-36.

[6] D.C.L.EE, D.S.LIM, AC Voltage and Current Senseless control of three-phase PWM Rectifiers, *IEEE Trans. on Power Electronics,* November 2002 , VOL.17, N°.6.

[7] R. Guedouani, E Berkouk, M. Boucherit ,Modélisation et commande d'un redresseur de tension triphasé à MLI, C2*MNI6 6ème Colloque Maghrébin sur les Modèles Numériques de l'Ingénieur*, 1998,Tunisie.

[8] J.P Hautier, X.Guillaud, Le formalisme et les modèles Hybrides appliqués à des convertisseurs statiques électroniques, *Revue Générale d'Électricité*, N°1/95.

[9] J.P. HAUTIER, G. MANESSE, Utilisation des réseaux de Petri pour l'analyse des systèmes électrotechnique,Technique de l'ingénieur (D 3 740).

[10] G Seguier, F. Labrique, *Les convertisseurs de l'électronique de puissance*, Edition Lavoisier. Tec & Doc, 1989, Tome1 et Tome 4.