Matrix Converter Active and Passive Protection Strategy Considerations

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Abstract: This paper focusses on Matrix Converter (*MC*) protection strategies. In order to improve its ride-through capability, *MC* faults are classified and some software and hardware strategies are proposed. The influence of the clamp circuit in *MC* switches is analyzed, while a special emphasis is given to the blocking voltage of different *MC* topologies. Besides, the *MC* and doubly fed asynchronous induction machine (*DFIM*) interaction is theoretically studied in terms of the protection circuit and, finally, all the design parameters relating to a practical clamp circuit are defined in order to ensure its commercial use in full-scale applications.

Key–Words: Matrix converter, clamp design, doubly fed asynchronous induction machine, *DFIM*, overvoltage protection, overcurrent protection, bidirectional switches, B6 Bridge

1 Introduction

The clear trend of the power electronics market is to attain the following objectives: improve interaction with the grid, the flow of bidirectional power, high-efficiency, operation at high commutation frequency, small size and the integration of complex solutions within a single power module. In principle, the Matrix Converter (*MC*) meets all of these targets.

The *MC* is an *AC/AC* converter, where it is possible to implement a *n x m* polyphase converter. Because of its inherent bidirectional topology, the *MC* can operate in all four quadrants, taking or delivering instantaneously power from the grid. Using appropriate modulation strategies, it is possible to achieve sinusoidal currents at the grid and sinusoidal voltages at the load [1]- [2], with a unity power factor with any type of load, having a low harmonic distortion in these waveforms.

However, the *MC* presents some disadvantages: voltage transfer ratio is limited to $\frac{\sqrt{3}}{2}$; high number of power switches (this means a higher connection complexity, control and thermal management); protection of the converter is a complex task, because there is no way to store energy; and, finally, the *MC* is very sensitive to voltage dips and distortions in the grid, because the power conversion has no intermediate steps.

Nowadays, most wind turbine manufacturers are working with new concepts based on Variable Speed Wind Turbine (*VSWT*) with pitch control driven with doubly fed induction machines (*DFIM*) [3]. *VSWT-DFIM* platforms require a power converter connected between the rotor and the grid. *MC-DFIM* applications are unknown in the industry, but recently *Vestas* has patented a variable speed wind turbine having a matrix converter [4]. Taking the overall characteristics of the *MC*, it could provide solutions for a wide range of applications. In order to consolidate its use on the real scale applications market and, being aware of the fact that the effort of the community revolves around control algorithms, this paper tackles the protection problems of *MC*.

In this paper, *MC* faults are classified and some protection strategies are proposed; the influence of the clamp circuit in *MC* switches is analyzed; then, the *MC* and *DFIM* interaction is theoretically studied (in terms of the protection circuit); and, finally, all the design parameters relating to the clamp circuit are defined.

2 MC Fault Conditions

MC performs a direct *AC/AC* conversion, without any storage element, so it is a low ride-through capability converter and it is very difficult to control and protect the *MC* during fault conditions. In general, the fault conditions can be classified as overcurrent and overvoltage. The reasons of overcurrent could be:

a) *MC* supply faults: due to grid distortion, voltage sag, voltage drop out, blackout, etc.

b) *MC* commutation faults: due to *MC* switch faults, *EMC* fault, control strategy fault, inadequate *MC* switch combination, error on current sign detection, two basic *MC* rules are not fulfilled, etc.

c) Abnormal operation of the motor: due to overload, short circuit in its coils, grounding faults, etc.

d) High inrush currents: due to inappropiate start up of the converter or absence of a resistor in the protection circuit.

e) Circulating current along *MC* switches: due to *MC* commutation faults or two basic *MC* rules are not fulfilled.

On the other hand, overvoltage faults can be classified as input and output overvoltages. The reasons could be:

a) Input overvoltage: due to distortion or perturbation on the grid. Usually, they are short in time and they can be damped by the input filter capacitor [5].

b) Output overvoltage: due to sudden *MC* shut down. It is one of the main *MC* problems (greater than the input overvoltage) and this is usually originated by overcurrent problems. The worst case should be when load current reaches overcurrent limit and *MC* switches are turned off; this way, the overvoltage appears when there is no path for the inductive currents of the load and there is a magnetic energy stored on it.

c) Stray inductance along *MC* switches can generate overvoltages in both sides of the converter because of high $\frac{di}{dt}$ at switching instants. In order to reduce this effect C_f (fig. 1) should be placed as near as possible from the *MC* switches.

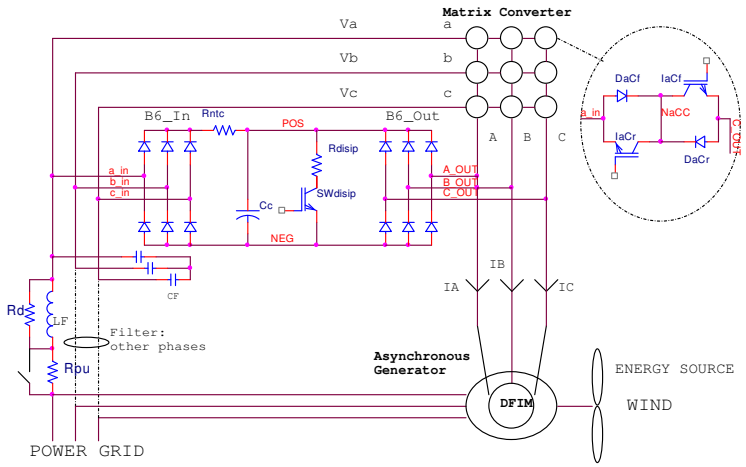

Figure 1: Matrix Converter, filter and clamp circuits.

3 Protection Strategy Considerations

In order to reduce the effect of fault conditions, *MC* controller can activate some vectors; this form of protection should be classified as software or active strategies:

1) Overcurrent protection strategy [6]: when high currents are unleashed in the load they can be reduced applying a properly selected *MC* vector. For example, if I_A is positive and I_B and I_C are negatives (fig. 1), then the control should active the corresponding vector that makes *MC* input voltages in the next way: V_a as negative as possible and V_b and V_c as positive as possible. Here, *MC* selected vector will change as a function of the variations of changes in V_{in}.

2) Circulating current protection strategy [6]: the switches of the output phases in which there is no overcurrent can be controlled until load current in these phases are crossing zero. The switches involved in the circulating current are switched off while one of the remaining switches of the phase is turned on to give a path to the motor current. The current only rises during the delay time of switching off the *IGBTs*. Besides, the input filter inductance [5] makes smoother the slope of the current.

It is advisable to place in the correct position current and voltage sensors to detect the possible faults that should appear in *MC*. The *MC* current fault threshold level must be established taking into account the maximum current of the load (higher than the nominal current), the nominal current of *MC* switches and the power losses in *MC*. The current level on *MC* output, among others, depends on the power delivered to the load, the power factor and *MC* voltage transfer ratio. This current level and *MC* switching frequency will determine the *MC* power losses and so the temperature reached by the semiconductors.

3) Overvoltage protection when one switch does not respond: the load phase without any current path should be connected to another input phase (always fulfilling two basic rules of *MC* and selecting a switch that operates appropriately). When load current is zero, *MC* should be turned off [6]. In this case, a little clamp circuit should be necessary giving a path to the opened phase load and limiting the overvoltage caused by it.

4) Control the magnetic energy stored in the load

(W_L) and its current during fault conditions [7]: on the one hand, applying a zero vector the kinetic energy of the motor is converted into W_L; and due to the short-circuit of the load phase its currents should increase. On the other hand, turning off all the *MC* switches, W_L will be transferred to clamp circuit, and because of clamp voltage is higher than the back *EMF* of the motor, its currents should be forced to decrease. So, the control must alternate between zero vector and switching off the *MC*.

5) Control the magnetic energy stored in the load (W_L) during normal operation of *MC* [8]: the W_L can be reduced applying dynamically free-wheeling paths (current sense must be known). These paths should be formed by the bidirectional *MC* switches. The control must maintain the load currents while applying reverse biased voltages with respect to the load currents. These currents decrease to zero and there are not high current spikes due to zero vector is applied. Another way to minimize W_L [7] during normal operation is to control the motor by means of increasing the number of current harmonics, this increases the load losses and decreases the W_L.

6) Minimize inrush current at start up: whem the *MC* is turned on it is possible that one of the input phases has its peak value. The worst case for the *MC* should be when the capacitor of the clamp is discharged, appearing an inrush current. Besides, due to the presence of input filter [5] in *MC*, an overvoltage of two times the peak of input voltage can be in the clamp capacitor because of *MC* has been connected to the grid instantaneously. A solution for that problem should be the controlled connection of the C_c (1) to the source, i.e. selecting the input voltage that is nearest of zero or applying a ramp voltage.

7) Minimize output overvoltages during normal operation of *MC*: due to the presence of W_L in the load, the *MC* must control the turning off of its switches [9]. The magnetic energy is falling slowly and when it reaches zero level the *MC* is turned off.

Software protection is not enough to get correct ride-through capability in *MC*. Hardware or passive solutions, as the input filter [5] and the clamp circuit, are needed to operate safely:

8) The single stage *MC LC* low-pass filter [5] consists of (fig. 1) an inductance, a *X* class capacitor and a phase damping resistor to increase the attenuation of the resonance spike which occurs around the cut-off frequency. The aim of the filter is to minimize the impact of the converter in the network, to limit the emission of input current harmonics, thus reducing the ripple that occurs in the input current. In this way, the distortion of V_{in} and *EMI* emissions are minimized and the filter together with the *MC* are made to behave like a sinusoidal current from the input viewpoint. If R_{pu} is used (fig. 1) then overvoltages during power up process are minimized.

9) When the clamp circuit (patented by [10]) is used in *MC* the load parameters must be known and all-silicon property is reduced. But, on the other hand, it mitigates overvoltage problems: when *MC* is turned off, the voltage spike originated in the load is limited because W_L is transferred from the load to the clamp through the output bridge; besides, inrush currents and input side overvoltages are clamped by the C_c; during normal operation of *MC*, $L_{leakage}\frac{di}{dt}$ are minimized by this protection circuit. Besides, the clamp can be used to perform regenerative braking of a motor or the energy stored in the capacitor can be used to supply the components of *MC* during fault conditions [11], improving the ride-through capability. There are some alternatives to the clamp circuit:

- In [12] the clamp circuit is simplified using only 6 diodes. This can be performed when *MC* switches are in common emitter (*EC*) configuration. More isolated supplies are necessary (9 instead of 6 as in common collector, *CC*, topology). An intermediate architecture can be used [12] with some switches (*aA*, *bB* and *cC*) in *EC* and the others in *CC*.

- In [1], [8] the input filter capacitor is used to clamp the inductive load currents. Here, knowledge of direction of the load currents and polarity of line-to-line input voltages is required.

- In [9] varistors, suppressors and an additional circuit are used to protect *MC* against overvoltages; but, here, the problem of unbalanced blocking voltages must be solved. Besides, a problem appears if *MC* switches are turned off asynchronously. These can only be used in low power *MC* applications because the silicon devices dissipate the W_L [13].

The clamp circuit is the more robust architecture. For this reason the next sections will study it in detail.

4 MC Clamp Design Considerations

The next points must be taken into account during the design process of the clamp circuit:

a) The energy stored in the inductive load (W_L), must be estimated. If no resistor R_{disip} (fig. 1) is used in the clamp circuit, W_L should be calculated according to the load when the current limit protection has been reached and the *MC* has been turned off.

b) The energy that can be absorbed by the capacitor must be determinated (1). When the *MC* is turned on, the C_c will be charged until it reaches the peak values of the input line voltage. This voltage is increased in the presence of input harmonics to $V_{C_{ini}} \approx 600V$ (when $V_{in_{phase_{max}}} = 230V$) and the capability to absorb W_L is reduced.

$$W_C = \frac{1}{2} C_c \cdot (V_{C_{final}}^2 - V_{C_{ini}}^2) = W_{L_{clamp}} \quad (1)$$

where $V_{C_{final}}$ is the threshold in which SW_{disip} is turned on (*800V* taking into account C_c rating, see table 1).

c) The capacitor type (electrolytic capacitors allow a great amount of stored energy, while polypropylene capacitors show a better behaviour during transients), capacitor value and its maximum voltage must be determined. Many references, i.e. [14], say that this voltage depends on: W_L and the maximum blocking voltage of the *MC* switches. Nevertheless, it is also influenced by the amplitude of the *MC* input voltages. These parameters will influence during the time in which W_L is transferred to the clamp (fig. 2) as it is explained in section 6.

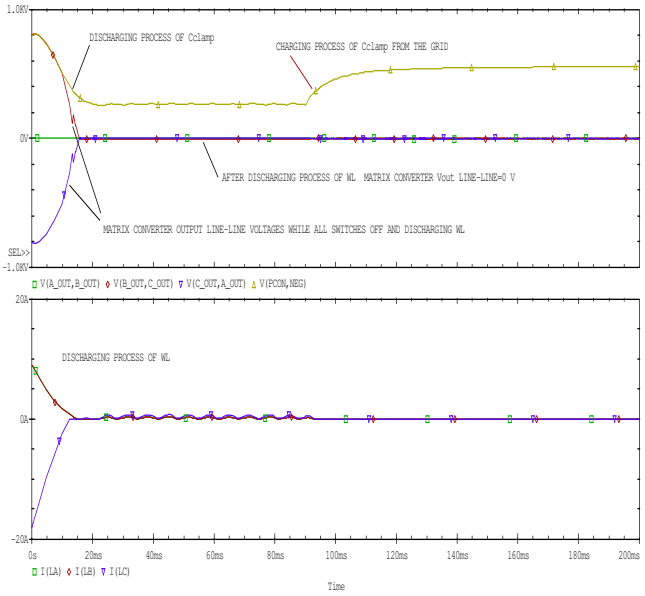

Figure 2: Discharging process of W_L when *MC* is turned off.

d) When the capacitor reaches high voltage levels and it must absorb W_L, depending on these values, it is necessary to use two capacitors in series to increase the voltage capability. In this case, some small resistors placed in parallel with C_c are necessary to balance the voltage between these reactive elements.

e) In order to increase the modularity, the clamp capacitor can be considerably reduced by using a resistor R_{disip} (fig. 1). Its function is to dissipate the excess of energy (2) that is not transferred to the capacitor and to discharge C_c when it reaches its maximum voltage. This way, the *MC* is cheaper and compact (10 to 100 times [7]). Besides, when R_{disip} is used no additional heatsink must be employed because it works only during fault conditions.

$$W_{L_{R_{disip}}} = W_L - W_{L_{clamp}} \quad (2)$$

If *MC* is used in high power applications, C_c should be too big, thus reducing the initial advantage of the *MC* based on all-silicon converter; so, it is possible to remove the C_c by sizing the resistor and its switch to handle the overcurrent level and taking into account the blocking capability of *MC* switches.

f) A correct ohmic value of R_{disip} must be selected. When C_c must be discharged, SW_{disip} is turned, and if there is a remaining part of W_L in the load, depending on the value of R_{disip}, the magnetic current can flow through R_{disip} and C_c, contributing in this way to increase the C_c voltage (fig. 3 and 4). So, this capacitor can be damaged and $V_{ce_{max}}$ can be exceeded. On the other hand, many manufacturers usually select a R_{disip} which power is a third of the load power (3).

$$P_{R_{disip}} \approx \frac{1}{3} \cdot P_{Load} \quad (3)$$

g) If an output filter is included in *MC*, the energy stored in this filter should be considered when sizing C_c and R_{disip}.

h) If C_c is connected directly to the input bridge, high inrush current $I_{C_{irh}}$ (4) may appear (fig. 5). In order to minimize it, a *NTC* (R_{ntc} in fig. 1) is proposed to be included between the input bridge and the capacitor clamp C_c.

i) The blocking voltage in the diodes of the input (fig. 6) and output bridges must be considered (fig. 7) in the worst cases.

$$I_{C_{irh}} = C_c \cdot \frac{dV_{in_{line}}}{dt} = 2\sqrt{2}\pi \cdot f_{in} \cdot C_c \cdot V_{in_{line}} \quad (4)$$

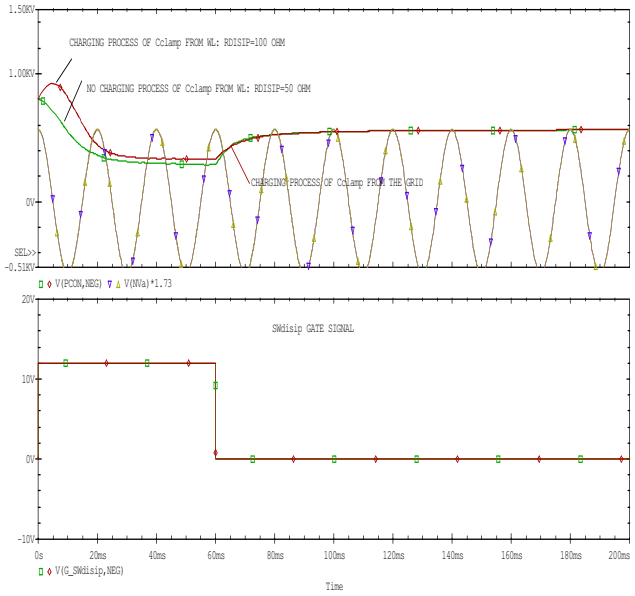

Figure 3: Discharging process of C_c with suitable turning on of SW_{disip}.

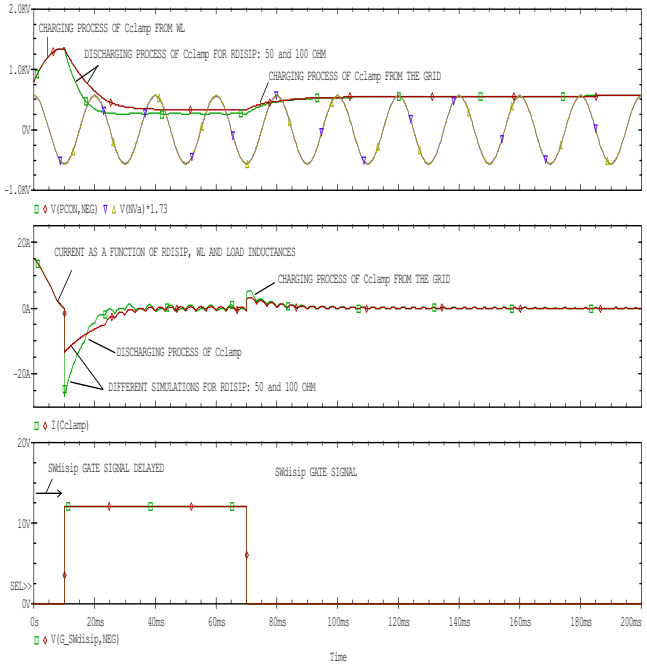

Figure 4: Discharging process of C_c with delayed turning on of SW_{disip}.

5 W_L study with DFIM load

5.1 Nomenclature

- p: derivative operator.
- $\overrightarrow{Z}_x^e$: Z (voltage, flux or current) vector linked to the stator flux frame (e); where x: stator (s) or rotor (r). These vectors can be decomposed in d and q components.
- R_x: stator or rotor coils resistance (x: s or r).
- ω_r: rotor electrical speed.

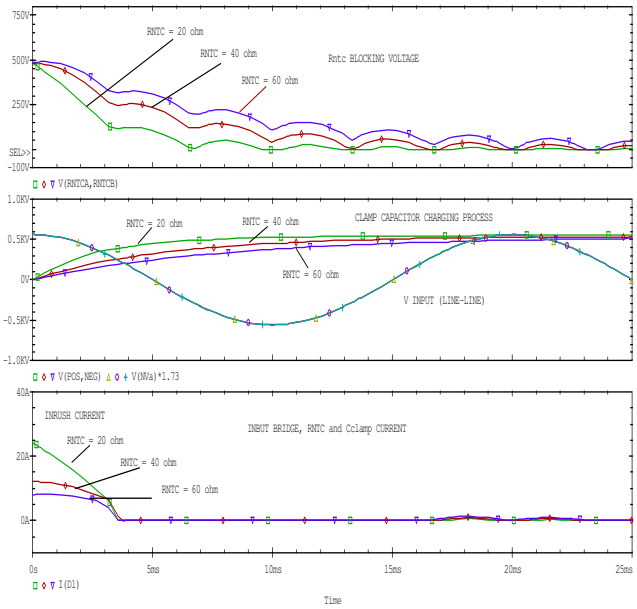

Figure 5: Initial charging process, inrush current and blocking voltage in R_{NTC}.

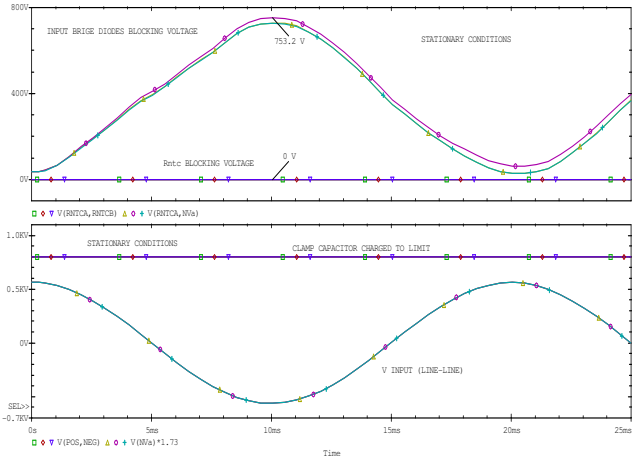

Figure 6: Input bridge diodes and R_{NTC} blocking voltage with $V_{C_c} = 800V$.

Table 1: Practical clamp circuit components values.

Component	Main values	Manufacturer
C_c (2 in series)	270μF, 450V, 35x35mm	Nichicon
R_{ntc}	20Ω, 10A, 500J, 680V, 35x74mm	Ametherm
R_{disip}	50Ω, 600W (2.7Kw)	Cressall
SW_{disip}	1200V, 33A (114A)	IR
Bridges	1200V, 60A (750A)	Semikron

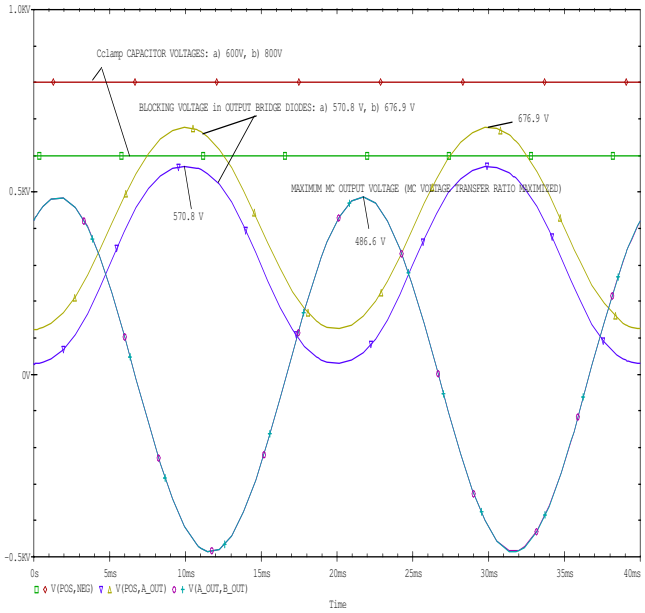

Figure 7: Output bridge diodes blocking voltage with maximum *MC* voltage transfer ratio and V_{C_c}=600V and 800V.

- ω_e: synchronism speed (reference system speed).
- L_{xl}: stator or rotor (*x*: *s* or *r*) leakage inductance.
- L_m: magnetic inductance.
- N_x: number of equivalents turns (*x*: *s* stator or *r*) rotor.
- W_L: magnetic energy stored in the machine.
- P_x: stator or rotor (*x*: *s* or *r*) power.
- $P_{R_{s,r}}$: stator and rotor (*s* or *r*) power losses.
- $P_{magn_{s,r}}$, $P_{em_{s,r}}$: magnetic and electromagnetic power.
- V_{sx}, V_{sy}, I_{sx}, I_{sy}: stator and rotor instantaneous phase voltages and currents (stator *x: a, b, c*; rotor *y: A, B, C*).

5.2 DFIM Magnetic Energy Evaluation

In order to design properly the *MC* clamp circuit the stored magnetic energy (W_L) must be calculated. This section shows how to calculate it when the load is a *DFIM*.
The *DFIM* equations, in the reference frame linked to the stator flux (fig. 8) are defined in (5)-(8).

$$\overrightarrow{V}_s^e = R_s\vec{I}_s^e + p\vec{\psi}_s^e + j\omega_e\vec{\psi}_s^e \quad (5)$$

$$\overrightarrow{V}_r^e = R_r\vec{I}_r^e + p\vec{\psi}_r^e + j(\omega_e - \omega_r)\cdot\vec{\psi}_r^e \quad (6)$$

$$\vec{\psi}_s^e = L_s\vec{I}_s^e + L_m\vec{I}_r^e \quad (7)$$

$$\vec{\psi}_r^e = L_r\vec{I}_r^e + L_m\vec{I}_s^e \quad (8)$$

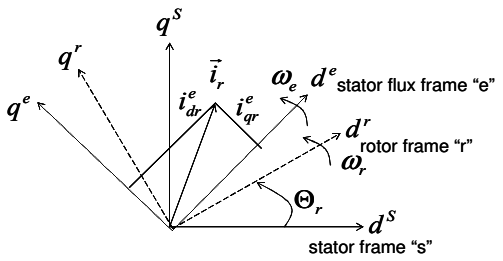

Figure 8: Reference frames and angles for the *DFIM*.

where L_s and L_r inductances are defined as

$$L_s = L_{sl} + \sqrt{\frac{3}{2}}\frac{N_s}{N_r}L_m \qquad L_r = L_{rl} + \sqrt{\frac{3}{2}}\frac{N_r}{N_s}L_m \quad (9)$$

The machine can be represented by two equivalent circuits (fig. 9), each one corresponding to *d* and *q* frame components.

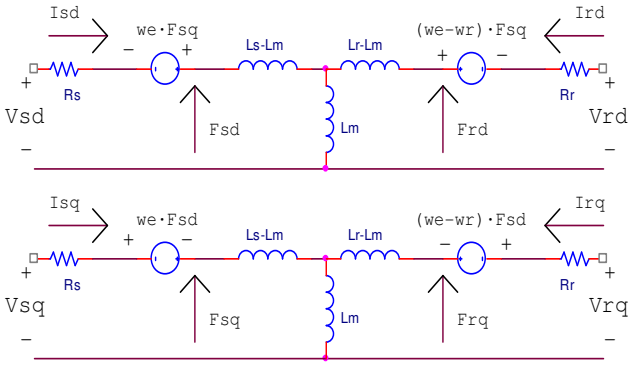

Figure 9: *DFIM* equivalent circuit (*d* and *q* frame components) in transitory conditions.

The *DFIM* interchanges power with the grid through the stator and rotor. Considering a balanced system, these powers are defined as:

$$P_s(t) = \sum_{x,y=a,b,c} V_{sx}\cdot I_{sy} = V^e_{sd}\cdot I^e_{sd} + V^e_{sq}\cdot I^e_{sq} \quad (10)$$

$$P_r(t) = \sum_{x,y=A,B,C} V_{rx}\cdot I_{ry} = V^e_{rd}\cdot I^e_{rd} + V^e_{rq}\cdot I^e_{rq} \quad (11)$$

Using (5)-(8) in (10) and (11) the next expressions, which represents the power generated in the stator and rotor, are obtained.

$$P_{s,r}(t) = P_{R_{s,r}}(t) + P_{em_{s,r}}(t) + P_{magn_{s,r}}(t) \quad (12)$$

That is, the machine power is distributed in: the resistive losses (13); the converted power in mechanical or electromagnetic power (14)-(15), it will be output or input power depending on the machine works as generator or motor; the necessary power to magnetize the machine (16)-(17).

$$P_{R_{s,r}} = R_s \cdot (I_{sd}^{e^2} + I_{sq}^{e^2}) + R_r \cdot (I_{rd}^{e^2} + I_{rq}^{e^2}) \quad (13)$$

$$P_{em_s} = \omega_e \cdot (I_{sq}^e \psi_{sd}^e - I_{sd}^e \psi_{sq}^e) \quad (14)$$

$$P_{em_r} = (\omega_e - \omega_r) \cdot (I_{rq}^e \psi_{rd}^e - I_{rd}^e \psi_{rq}^e) \quad (15)$$

$$P_{magn_s} = (p\psi_{sd}^e) \cdot I_{sd}^e + (p\psi_{sq}^e) \cdot I_{sq}^e \quad (16)$$

$$P_{magn_r} = (p\psi_{rd}^e) \cdot I_{rd}^e + (p\psi_{rq}^e) \cdot I_{rq}^e \quad (17)$$

The magnetic energy (18) stored in the machine is

$$W_L = \int P_{magn_{s,r}}(t) \cdot dt \quad (18)$$

Using (16)-(17) and (7)-(8), W_L can be decomposed in *d* (19) and *q* (calculated in a similar way) components.

$$W_{Ld} = \int \left\{ (L_s - L_m) \cdot I_{sd}^e \right\} \cdot dI_{sd}^e + \int \left\{ (L_r - L_m) \cdot I_{rd}^e \right\} \cdot dI_{rd}^e + \int \left\{ L_m (I_{sd}^e + I_{rd}^e) \right\} \cdot d(I_{sd}^e + I_{rd}^e) \quad (19)$$

Adding W_{L_d} and W_{L_q}, the total amount of magnetic energy is obtained (20).

$$W_L = 0.5 \cdot \left[\left\{ (L_s - L_m) \cdot (I_{sd}^{e^2} + I_{sq}^{e^2}) \right\} + \left\{ (L_r - L_m) \cdot (I_{rd}^{e^2} + I_{rq}^{e^2}) \right\} + \left\{ L_m \cdot \left((I_{sd}^e + I_{sq}^e) + (I_{rd}^e + I_{rq}^e) \right)^2 \right\} \right] \quad (20)$$

When obtaining W_L from simulation, (20) should be used instead of (18) to avoid excessive noise errors from derivatives.

In fig. 10 simulated value of W_L during different operating intervals of *DFIM* are shown:

a) The *DFIM* accelerates with the stator open circuited.

b) Stator voltage synchronization with the grid.

c) Normal operation with zero active power generated.

d) Normal operation with non zero active power generated.

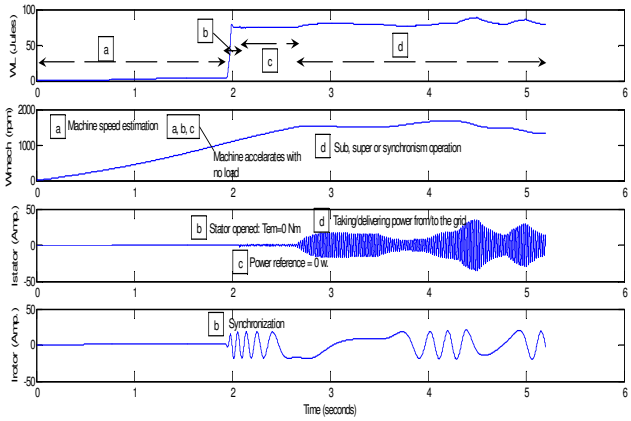

Figure 10: Magnetic energy stored in the DFIM, machine speed and stator and rotor currents.

6 Blocking Voltage in MC Switches

The blocking voltage of the semiconductors of the *MC* is one of the parameters to take into account when protecting the *MC*. On the one hand, the antiparallel diode of the *IGBT* is necessary to obtain V_{ce} blocking capability. On the other hand, $V_{ce_{max}}$ must not be exceeded in order to remain in the *IGBT SOA*. This way, the blocking voltage will appear in the left or right side of the bidirectional switch, only in one of them, while in the other side the difference of voltage will be around zero because the antiparallel diode is positively polarized. The next considerations must be taken into account:

1. Depending on the amount of input and output phases of the *MC*, states and vectors applied on it, the blocking voltage is different. Under normal conditions the voltage in the *IGBTs* of the bidirectional switches that are switched off depends on the *MC* switch configuration. For instance, if *CC* is used, the common node (*NaCC* in fig. 1) will be at the lowest voltage between the output voltage and the corresponding input voltage of each switch; and, if *EC* is used the node will be at the highest voltage. This blocking voltage will alternate between the left and right side depending on the values of the input voltages and the vector applied in the *MC*.

This way, a new protection strategy can be introduced. For example, when the system strategy or state does not allow to turn off the *MC*, and an input overvoltage is detected (due to resonance effects in the input filter, glitch on the grid or any of the before mentioned reasons), a *MC* vector which imposes in the *MC* outputs the input voltage which is not the highest and the smallest of them should be selected. This way, the blocking voltage in the semiconductors is minimized and damaging is avoided. This strategy acquires more importance if the clamp circuit is not used.

2. When a fault occurs there are two different situations:
a) The magnetic energy is being transferred to the clamp, and so the clamp diodes are conducting. In this case, the *MC* outputs will be connected to C_c for a short period of time (depending on the value of the stored W_L and the value of each phase inductance). Here, the blocking voltage (21) in the switches will be different and it will depend on the number of output phases, (i.e. *3x1*, *3x2* or *3x3 MC*), V_{clamp} and *MC* input voltage.

$$V_{block_{xY}} = V_{in_x} \pm k_{V_{clamp_z}} \quad (21)$$

where *x* can be one of the *MC* (1) input phases (*a*, *b* or *c*), and *Y* one of the output phases (*A*, *B* and *C*) and *z* represents the polyphase structure of the *MC*. The sign + or - depends on the polarity of V_{clamp}. When *MC* is *3x2* the offset $k_{V_{clamp_z}}$ will be (22):

$$k_{V_{clamp_{3x2}}} = \frac{V_{clamp}}{2} = \frac{V_{A_{out}} - V_{B_{out}}}{2} \quad (22)$$

In a *3x3 MC* architecture the blocking voltage varies with a different offset (23) (fig. 11):

$$k_{V_{clamp_{3x3}}} \approx \frac{V_{clamp}}{3} \quad (23)$$

So, if the maximum input voltage is *230V* and *IGBT* $V_{ce_{max}}$ is *1200V*, $k_{V_{clamp}}$ must be less than *875V* to fulfil (24). This way, turning on the R_{disip} switch when V_{clamp} reaches *800V*, $k_{V_{clamp}}$ rounds about *550V* and so a safety margin is assured.

$$|V_{block_{xY}}| = |V_{in_x}| + |k_{V_{clamp}}| < V_{ce_{max}} \quad (24)$$

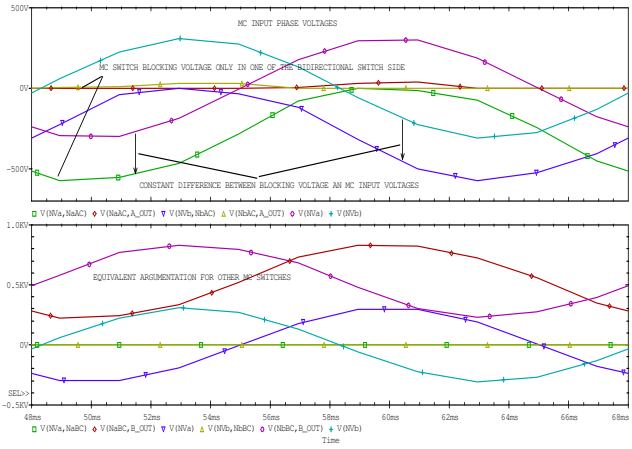

Figure 11: Blocking voltage with *3x3 MC* turned off.

b) W_L has been transferred, no current through the diodes is present. Then, the clamp circuit is isolated from the *MC* and V_{clamp} has not any influence in the blocking voltage. In this situation, this voltage will depend on only the input voltages (fig. 11).

3. The worst case for the blocking voltage of the clamp diodes takes place when the clamp is at its maximum voltage, the *MC* is not turned off and its output reaches the maximum voltage transfer ratio. Taking into account that *MC* output is floating, if $V_{C_{final}} = 800V$ and $V_{in_{phase}} = 230V$, the maximum blocking voltage will be *677V* (fig. 7).

7 Conclusions

Taking into account that *MC* has a low ride through capability, this paper deals with the *MC* protection. An exhaustive analysis of different fault conditions is presented and different active (which can be easily embedded in a *DSP* or *FPGA*) and passive solutions are summarized. A practical design of a clamp circuit is presented and the correspondence of this protection circuit with the *MC* and the load (*DFIM*) is determined.
Finally, the influence of the clamp on *MC* switches blocking voltage is quantified for different topologies; likewise, an active method to minimize it is introduced.
This way, it can be said that this paper contributes to the mitigation of certain *MC* protection deficiencies.

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