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About the FPGA Implementation in the Electronic Equipment for the Movement Properties Telemetry

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Abstract: - The paper presents the implementation of a programmable circuit (FPGA) in a Doppler radio telemetry system dedicated for the determination of the features of low speed motions with reduced cost of execution of movement in air environment. It is presented the choice of the structure based on the simulation in VHDL and is verified the proper operation of selected structure for the achievement of technical features required by the telemetric system.

Key-Words: - FPGA, VHDL, VCO, Doppler, Telemetry, PLL

1 Introduction

For the determination of the features of the motion in air with the low speed and reduced cost of execution, the authors proposed in [1] a system of radio telemetry Doppler with fixed active referential. The structure of the system is indicated in figure 1.

The correct operation of the structure indicated in figure 1 is based on the following requirements [1]:

a) - The selection of the studied movement from the multitude of movements with close features by changing the frequency f_1 to f_2 on the fixed referential (the activation of the fixed referential).

b) - The assurance of the initial phase shift of the frequency signal f_2 identically with the one of frequency f1, both generated in the electronic equipment on the mobile referential RM. The assurance of the initial phase shift and frequencies (f2) identity for the signal generated by the equipment on the fixed active referential RFA with the one generated by mobile referential RM.

c) - The introduction of the diplexer filter DF as an element which provides separate ways for the signals of frequencies f_1 and f_2; DF1 for the signal emitted on the frequency f_1 and received on the frequency f_2, and DF2 for the signal emitted on the frequency f_2 and received on frequency f_1.

d) - The assurance of centering of the Doppler deviation of frequency by modulating the f_2 frequency signal with a low frequency signal fj; compared with f_j the Doppler deviation of frequency $\pm\Delta f_2$ is not negligible and it permits the achievement of the centering signal s_{axi} and s_D at the exit of the extractor of Doppler signal, DSE.

e) - The use of a unique aerials on each referential, for the emission on f1 and the reception on f2 frequency – aerials A1, for the emission on f2 and the reception on f1 frequency – aerial A2.

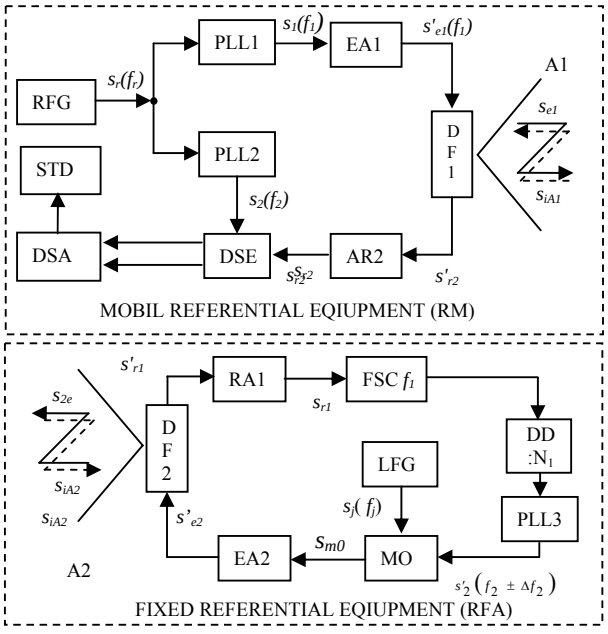

Fig.1. The general structure for the Doppler radio-telemetry system: RFG – reference frequency signal generator; LFG – low frequency signal generator; PLL1, 2, 3 – frequency synthesizers; EA1, EA2 – emission amplifiers; DF1, DF2 – diplex filters; RA1, RA2 – reception amplifiers; FSCf_1 – f_1 frequency selection circuit; DD – digital frequency divider; MO – DSB-SC modulator; DSE – Doppler signal extractor; DSA – Doppler signal analyzer; STD – display and transmit data block.

The conditions a, b and d are resulted from the conception of the structure and the other two are conditions required from the simplification of the electronic equipment on both referential.

The first two conditions are obtained with indirect frequency synthesizers, based on the PLL loop: RFG with PLL1 and PLL2 in the electronic equipment on RM and $FSCf_1$ with DD3 and PLL3, on RFA.

The b condition is realized only if the reference frequency f_r is the same on RFA with the one generated of RFG on RM and the PLL3 loop is the same with the PLL2. It is obtained the s'_r signal shown by the relation (1):

$$s'_r = A'_r \sin\left[2\pi\left(\frac{f_1}{N_1} \pm \frac{\Delta f_1}{N_1}\right)t + \varphi_1\right] = A'_r \sin\left[2\pi\left(f_r \pm \Delta f_r\right)t + \varphi_1\right] \quad (1)$$

For the maximum movement speed of RM, v_{max} = 70m/s and the propagation speed of electromagnetic wave $v_f = 2{,}98 \cdot 10^{10}$ m/s and a reference frequency $f_r = 10 \cdot 10^6$ Hz results $\Delta f_r / f_r = 2{,}3 \cdot 10^{-8}$, that means that the equality error of the reference frequency on RFA with the one on RM is $2{,}3 \cdot 10^{-6}$%.

The frequency synthesizers, two on RM and one on RFA, are essential electronic blocks in the structure of radio Doppler telemetry equipment shown in figure 1. The realization of them with dedicated integrated circuits leads to the improvement of the performances of movement evaluation, at the miniaturization of the electronic equipment and also to the decrease of price [4].

For the realization of frequency synthesizers, first, a FPGA is implemented in the RM equipment and another one in the RFA equipment. In the RM equipment the programmable circuit also is used for partial implementing DSE and DSA, and on RFA for the realization of the low frequency generator f_j. The structure of an indirect frequency synthesizer, based on PLL is indicated in Figure 2.

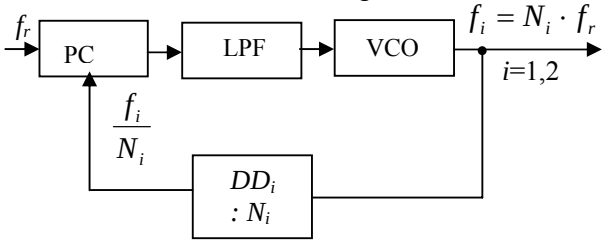

Fig. 2 Indirect frequency synthesizer: PC-phase comparator; LPF – Low pass filter; VCO –voltage controlled oscillator, DD_i - frequency divider

For high frequency 140 MHz, 160 MHz, partially or totally numeric synthesizers are used. The complete numeric synthesizer gives at the exit a rectangular wave and must be clocked with a frequency three times bigger than the biggest generated frequency. If that kind of programmable circuit is not available, there can be realized a partial numeric synthesizer which use a voltage controlled oscillator as a separated analogical unit.

2 The FPGA implementation

The FPGA-FLEX10K circuit was obtained by our research community from ALTERA Corporation together with the support for applications development. Concomitantly, there were received the developing software QUARTUS II and MAX-PLUS II [7,8]. This software package offers facilities in introducing projects in graphic format, text format (including VHDL and VERILOG) or in wave form, with compilation and synthesis, full simulation, time analysis for the worst cases and device configuration. Every device contains, mainly, an incorporated matrix and a logic matrix. The incorporated matrix is used for implementing a variety of memory functions or a series of complex logic functions (digital signal processing, microcontrollers, and use of large data lines and data conversion functions).The logic matrix is used for the implementation of general logic functions – counters, adders, state automats and multipliers.

The combination of the two matrixes leads to high performances and gives the user the chance to implement a complete logic system in one device

2.1 The phase comparator.

In the realization of the PLL loop, see figure 2, the contribution of the FPGA circuit is the programmable dividers and the phase comparator. The most important part is the phase comparator, and it will be forward treated. Trough the same signal entries *comp_in* (f_r in figure 2) and *sig_in* (f_{0i} / N_i in figure 2) can be created three types of phase comparators with the exits PC1, PC2 and PC3 – figure 3.

The phase comparator 1, PC1, is formed from a network of XOR gates. The input signals *comp_in* and *sign_in* must have a 50% duty cycle in order to obtain the optim catch of phase. The mean output voltage of PC1-out, which arrives at the entry of the voltage-controlled oscillator VCO through a low pass filter, LPF, is obtained at the output of the demodulator and it is the difference of phase of the two input signals. When there is no difference of phase, the mean output voltage is $V_{CC} / 2$, and the VCO oscillates on the central frequency f_0.

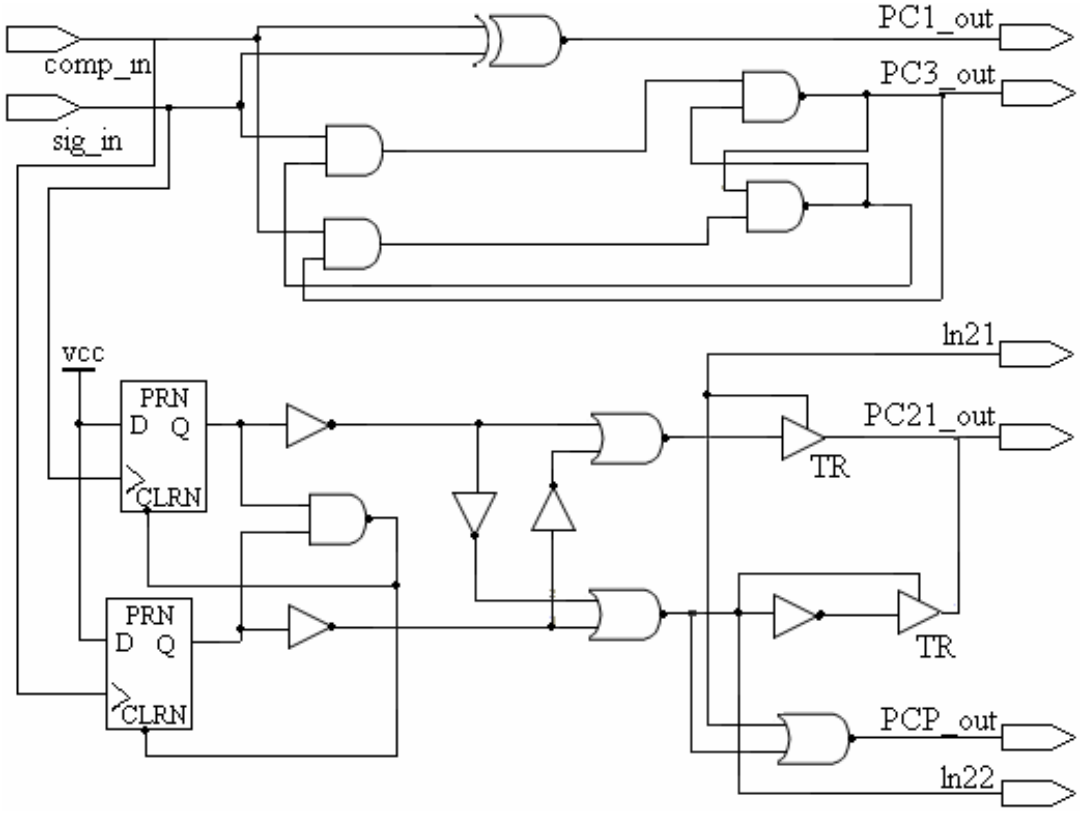

Fig.3.The structure of the phase comparator

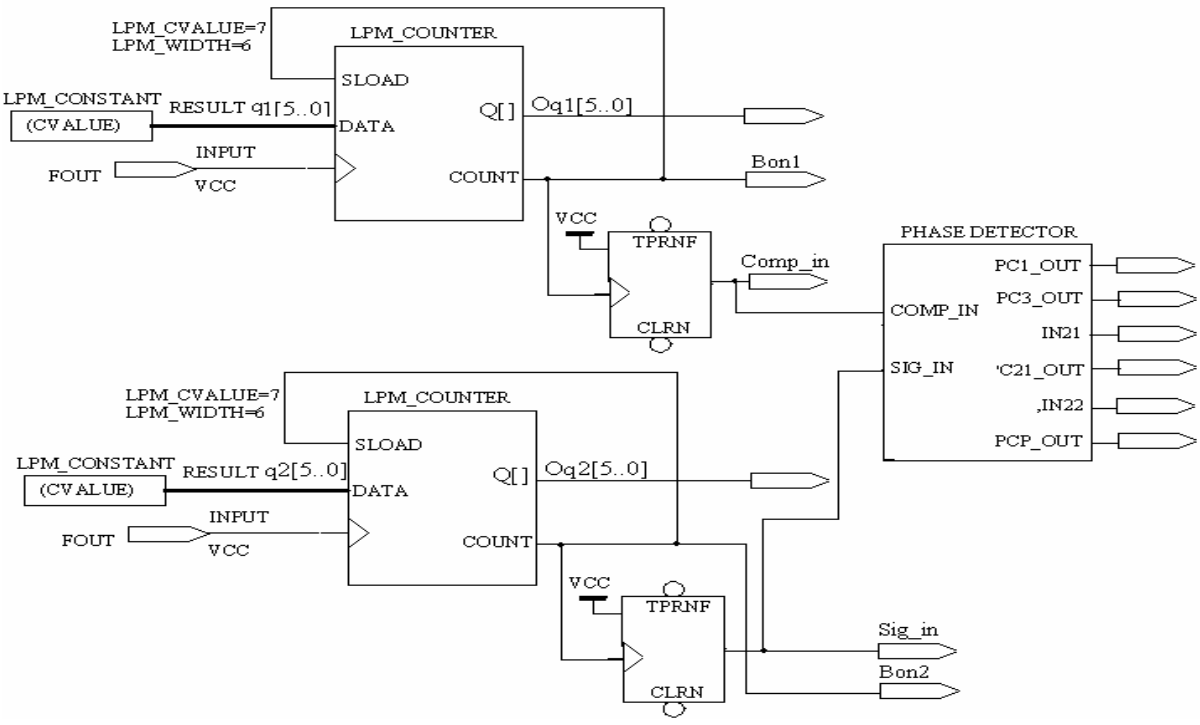

Fig.4 .The structure of the digital section for the FPGA implemented PLL.

The range of capture frequencies is lower or equal to the range of the follow-up frequencies and depends on the characteristics of the LPF filter. This structure of the comparator preserves the loop locked even for noise affected input signals. The phase comparator 2, PC2, is a phase and frequency detector activated on the raising edge of the clock. When the PLL uses this comparator, the loop is controlled by the positive transition of the input signals and the duty cycle is no longer important. PC2 contains two D-flip-flops, two control gates and an output stage with three states When the input signals *sign_in* si *comp_in* are the same, but *comp_in* goes behind *sign_in*, then the "p" driver, from the output PC 2 is kept "ON" for a time which corresponds with the difference of phase φ.When the input signal *sign_in* goes behind com_in, then, the "n" driver is kept "ON". When the frequency of the signal *sign_in* is higher than frequency of *comp_in* ,the output driver "p" is kept "ON" for a long time of the input signal period, and for the rest of the period both drivers – "p" and "n"-are "OFF"- three state , the high impedance state. If the frequency of the signal *sign_in* is lower, then the "p" drivers is kept "ON" for a long time of the period .The voltage on the low pass filter's capacitor connected at the output $PC2_{OUT}$ varies until the two input signals have the same frequency and phase; at this time, the output PC2 is in high impedance. For such a phase comparators, the follow band and the catcher band are the same, and both bands are independents of the low pass filter. The phase comparator 3, PC3, is a sequential phase detector, which uses a RS flip-flop. When the PLL loop uses this comparator, it is controlled by the positive input signal transitions and the duty cycle of the input signals aren't important. The mean voltage at the output PC3 is the difference of phase of the two input signals. The catcher and the follow bands depend on the low pass filter.

The frequency divisors used in the PLL structure are basically, presetable counters with self loading. Basically each loop have two dividers A first divisor feeds the reference input of the phase comparator and the second one divides the VCO output signal, and the output of this divisor is fed to the second input of the phase comparator. The scaling reports are chosen so that they comply with the necessary frequencies and the desired resolution is assured.

Following this considerations result a compact implementation of a PLL loop in FLEX10K which is shown in fig.4. In order to implement the frequency dividers were used counter modules from the parametric modules library provided by the MAXPLUS II environment [7].

3 Experimental Results

In the electronic equipment on the mobile reference RM, there are two PLL loops: PLL1 and PLL2 - see fig. 1. For this two loops, the circuit FPGA-FLEX10K can implement two structures such as the one showed in figure 5, using like VCO two , professionals circuits, MAX2606 for f_{01} = 140 MHz and MAX2607 for f_{02} = 160 MHz.

The inductances are standard and was delivered with the integrated circuits MAX2606 MAX2607.The values L_{Fi}, i=1,2 are determined from the characteristics diagram of the chip [9], for $f_{0i.}$ The voltage-controlled oscillator (VCO) was made on a printed circuit board special designed for high frequencies in technique SMD which was connected with the FPGA/FLEX10K development board. The board was fully-equipped with the adequate connectors for the connection to the PC.

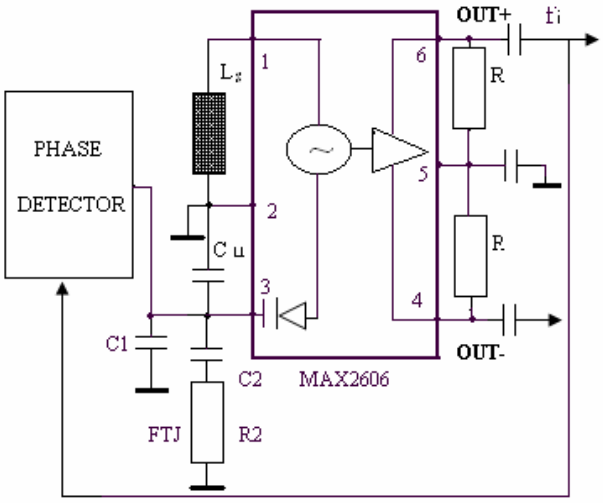

Fig.5. The connection of VCO-MAX2606, MAX2607 in a PLL loop with FPGA FLEX10K

Figure 6 show the proper operation of the PLL digital section implemented in Flex10k. The results were obtained by simulation with MAXPLUS II environment.

4 Conclusion

The paper presents the implementation of a programmable circuit (FPGA) in a Doppler radio telemetry system. It is presented the choice of the structure based on VHDL simulation and is verified

the proper operation of selected structure for the achievement of technical features required by the telemetric system

The FLEX 10K structure contains three phase comparators, meaning that the device allows the construction of three digital or the half digital frequency synthesizers in PLL loop. The choosing of the structure for the divisors and for the phase comparator in order to obtain from VCO the carrier frequency f_1 and f_2, was achieved through modern designing in VHDL [6, 7]. The accuracy check of the chosen solution is achieved trough simulation, considering different situation for reference and output frequency as well as the case of PLL being locked. In all the three considered cases, the diagrams show a correct operation of the chosen structure.

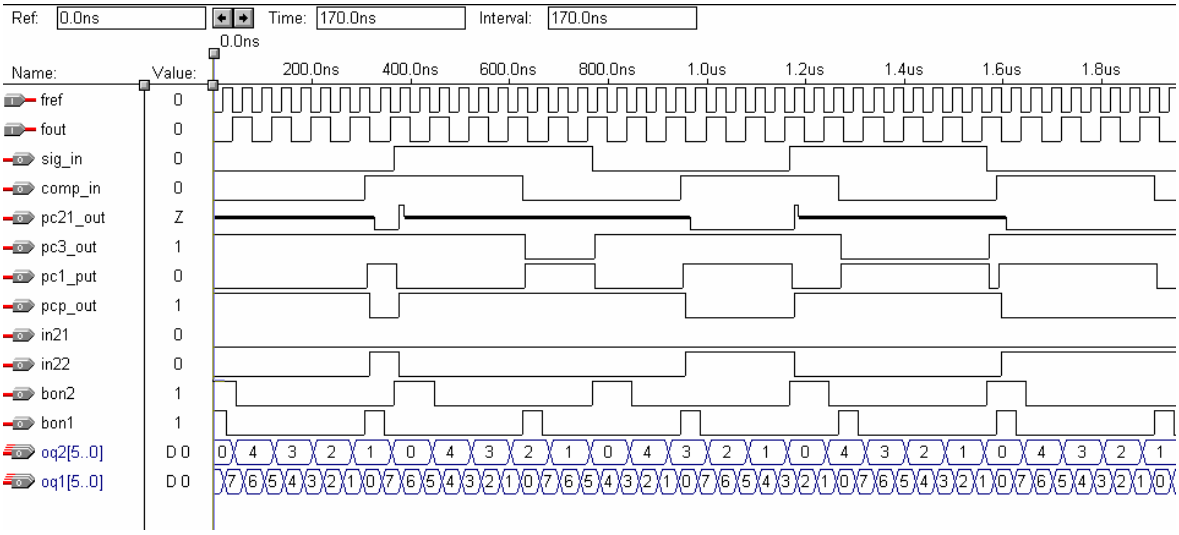

Fig.6 .Timing diagram for the digital section of a FPGA implemented PLL – case when the loop is locked.

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