

State-Space Analytical Modelling for On-Chip Coupling Effects

HJ KADIM

School of Engineering
Liverpool JM University
Liverpool L3 3AF
UK

Abstract – Increasing interconnect-densities and high clock rates give rise to cross-coupling effects between on-chip interconnect wires – thus leading to significant delay and crosstalk noise problems that may affect signal integrity. In this paper, state-space-based analytical modelling expressions to examine the effect of crosstalk noise on circuit parameters are presented.

Key-Words: - State-space, Interconnect, Crosstalk, Noise, VLSI

1 Introduction

Crosstalk noise resulting from capacitive and inductive effects [1][2] between adjacent interconnect lines is becoming a major concern for circuit performance and reliability. Crosstalk noise is defined as the noise voltage on signal lines caused by a change of state in neighbouring lines. The line affecting its neighbour by its switching state is often referred to as the aggressor line, while the affected one as the victim line. Crosstalk noise can lead to performance degradation and functional failure depending on the state of the conduction wire and its adjacent neighbours and equally importantly, depending on the width, peak amplitude and frequency of the generated parasitic noise [3]. Development toward Deep Sub-Micron (DSM) technology requires that such consideration being taken into account to accurately and efficiently estimate interconnects crosstalk-induced noise and delay.

On-chip interconnect wires were modelled as lumped capacitance, then as lumped and distributed RC lines [4][5], with Elmore delay model [6], which only considers the first moment, was employed for estimation of delays and related crosstalk effects. At the DSM level, the average length of an interconnect line being often resistive compared to its driver resistance, and therefore requiring that the inductive and distributed nature of on-chip interconnect are properly modelled [7] Pillage [8] extended the concept of two poles one zero transfer function approximation by Horowitz and introduced

Asymptotic Waveform Evaluation (AWE) for RLC networks. This technique is based on explicitly matching the ‘ $2q-1$ ’ moments of the transfer function using Padé approximation. However, AWE technique, which has been mainly used for lumped RLC interconnect networks, suffers from numerical instability [9]. Recently, analytical and compact expressions for crosstalk analysis of distributed RLC line were presented in [10][11][12]. The compact expression of a single and coupled distributed RLC line presented in [10] is derived into time-domain using the incidence wave of the transmitted signal without explicitly solving the s-domain expression of the line transfer function. However, the analysis in [10] is based on a distributed RLC line with arbitrary series impedance, therefore misrepresentative of the practical VLSI interconnect model. The above works mainly focus on accurate modelling of noise effects and may result in an excellent match between models and Spice, but they lack insight into the effect of coupling effects on circuit and signal parameters (e.g. phase shift, operating frequency). In this paper, a state-space based analytical model to examine the effect of worst-case crosstalk noise on circuit parameters is presented.

This paper is organised as follows: Section 2 introduces the single-line analytical expressions, and the distributed-coupled RLC transmission line model, including the worst-case crosstalk noise expression. Simulation results are presented in Section 3. Conclusions are given in Section 4.

2 Mathematical Modelling

A distributed RLC interconnect of length d , with driver resistance and load capacitance is depicted in Fig.1.

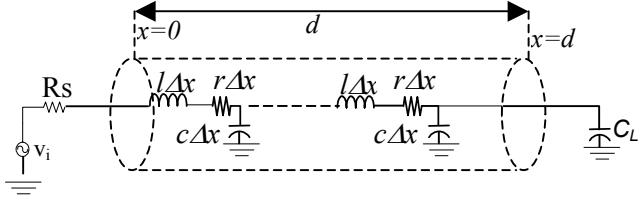


Fig.1. Distributed RLC transmission Line

From Fig.1:

$$v(x,t) = r\Delta x I(x,t) + l\Delta x \frac{\partial i(x,t)}{\partial t} + v(x+\Delta x, t) \quad (1)$$

Re-writing (1):

$$\frac{\partial v(x,t)}{\partial x} = ri(x,t) + l \frac{\partial i(x,t)}{\partial t} \Big|_{\Delta x \rightarrow 0} \quad (2)$$

Applying Kirchhoff's current law:

$$i(x,t) = i(x+\Delta x, t) + \Delta i \quad (3)$$

$$i(x,t) = i(x+\Delta x, t) + c\Delta x \cdot \frac{\partial v(x+\Delta x, t)}{\partial t} \quad (4)$$

with

$$\frac{\partial i(x,t)}{\partial x} = c \frac{\partial v(x,t)}{\partial t} \Big|_{\Delta x \rightarrow 0} \quad (5)$$

Manipulating (2) and (5), and taking Laplace Transform:

$$\frac{\partial^2 v(x,s)}{\partial x^2} = s^2 lc(1 + r/l_s) v(x,s) \quad (6)$$

$$\frac{\partial^2 i(x,s)}{\partial x^2} = s^2 lc(1 + r/l_s) i(x,s) \quad (7)$$

The solution of (6) and (7) are given by:

$$v(x,s) = v_1 e^{-\lambda x} + v_2 e^{\lambda x} \quad (8)$$

and

$$i(x,s) = i_1 e^{-\lambda x} + i_2 e^{\lambda x} \quad (9)$$

$$\text{Where } \lambda = s\sqrt{lc} \sqrt{1 + \frac{r}{sl}}$$

By manipulating and applying the boundary conditions to (8) and (9), the fourth-order transfer function is given as follows:

$$\frac{v(x=d,s)}{v_i(s)} = H(s) = \frac{1}{b_4 s^4 + b_3 s^3 + b_2 s^2 + b_1 s + 1} \quad (10)$$

where the b_i 's coefficients are as in [3].

From (10),

$$\frac{V_o(x,s)}{V_i(x,s)} = \frac{s^{-4}}{b_4 + b_3 s^{-1} + b_2 s^{-2} + b_1 s^{-3} + s^{-4}} \quad (11)$$

$$E(x,s) = V_i(x,s) - \frac{I}{b_4} \left(1 + \frac{b_3}{b_4} s^{-1} + \frac{b_2}{b_4} s^{-2} + \frac{b_1}{b_4} s^{-3} + \frac{1}{b_4} s^{-4} \right) E(x,s) \quad (12)$$

$$Y(x,s) = \frac{I}{b_4} E(x,s) \Big|_{Y(x,s)=V_o(x,s)} \quad (13)$$

where E is a convenient variable to link the two equations.

Equations (6) and (7) lead to four state variables $x_1(t)$, $x_2(t)$, $x_3(t)$ and $x_4(t)$ as follows:

$$x'_1(t) = x_2(t) \quad (14a)$$

$$x'_2(t) = x_3(t) \quad (14b)$$

$$x'_3(t) = x_4(t) \quad (14c)$$

$$x'_4(t) = - \left[\left(\frac{1}{b_4} \right) x_1 + \left(\frac{b_1}{b_4} \right) x_2 + \left(\frac{b_2}{b_4} \right) x_3 + \left(\frac{b_3}{b_4} \right) x_4 \right] + V_i(t) \quad (14d)$$

$$Y(t) = \frac{1}{b_4} x_1(t) \quad (15)$$

From (14) and (15), the state-space (SS) representation of the distributed RLC line is as follows:

$$x'(t) = Ax + Bx \quad (16)$$

$$Y(t) = Cx + Dx \quad (17)$$

Such that:

$$x'(t) = \begin{bmatrix} 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \\ -\frac{1}{b_4} & -\frac{b_1}{b_4} & -\frac{b_2}{b_4} & -\frac{b_3}{b_4} \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ x_3 \\ x_4 \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ 0 \\ 1 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ x_3 \\ x_4 \end{bmatrix} \quad (18a)$$

$$y(t) = \begin{bmatrix} I/b_4 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ x_3 \\ x_4 \end{bmatrix} \quad (18b)$$

For a typical interconnect of length 2um, with the following parameters: per-length mutual inductance, resistance and capacitance are 0.246pf, 0.0015Ω and 0.000176pf; the source resistance and load capacitance are 100 Ω and 0.01 pf, respectively:

$$A = \begin{bmatrix} 0 & \dots & \dots & -3.5 \times 10^{-44} \\ 0 & \dots & \dots & 0 \\ 0 & \dots & \dots & 0 \\ 0 & 0 & \dots & 0 \end{bmatrix}$$

$$B = \begin{bmatrix} I \\ 0 \\ 0 \\ 0 \end{bmatrix}; \quad C = \begin{bmatrix} 0 & 0 & 3.4 \times 10^{-44} \end{bmatrix}$$

With

$$A_{diag} = 10^{11} \times \begin{bmatrix} -9.7 & 0 & 0 & 0 \\ 0 & -0.064 + j1.24 & 0 & 0 \\ 0 & 0 & -0.064 - j1.24 & 0 \\ 0 & 0 & 0 & -0.22 \end{bmatrix}$$

In LT representation:

$$Y(s) = H(s)v_i \Big|_{H(s)=C(SI-A)^{-1}B+D} \quad (19)$$

For a ramp input:

$$Y(s) = K \prod_{i=1}^m (s - z_i) \Big/ s^2 \prod_{i=1}^n (s - p_i) \quad (20)$$

with

$$y(t) = L^{-1}\{y(s)\} \quad (21)$$

where z and p represent the zeros and poles of the output function; $m, n > 0$.

The response to a finite ramp input:

$$y_{fin}(t) = \frac{V_{DD}}{T_R} [y(t) - y(t - T_R)] u(t) \quad (22)$$

where T_R is the ramp rise time.

2.1 Coupled RLC Line

A coupled RLC line is shown in Fig.2.

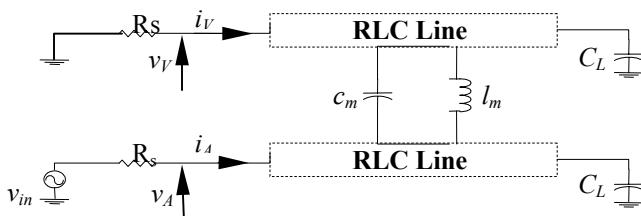


Fig.2 Coupled RLC lines.

The voltage equations for the aggressor and victim lines can be achieved by amending (6) to include the capacitive and inductive effect components, as follows:

$$\frac{\partial^2 v_a(x,s)}{\partial x^2} = s^2 lc(1 + r/l_s) v_a(x,s) - l_m s^2 i_a(x,s) \quad (23)$$

$$\frac{\partial^2 v_v(x,s)}{\partial x^2} = s^2 lc(1 + r/l_s) v_v(x,s) - l_m s^2 i_v(x,s) \quad (24)$$

where the subscripts ‘ a ’ and ‘ v ’ indicate the aggressor and victim lines, respectively.

With

$$s^2 i_a(x,s) = cs^2 V_a(x,s) - c_m s^2 (V_a(x,s) - V_v(x,s)) \quad (25)$$

and

$$s^2 i_v(x,s) = cs^2 V_v(x,s) - c_m s^2 (V_v(x,s) - V_a(x,s)) \quad (26)$$

By manipulating (23), (24), (25) and (26), the expression for voltage at which the worst-case crosstalk occurs is given as follows:

$$\frac{\partial^2 v^-(x,t)}{\partial x^2} = (\alpha(l - l_m) - \beta c_m) s^2 - r(c + 2c_m)s \Big|_{\alpha=c+c_m; \beta=l-l_m} v^-(x,s) \quad (27)$$

$$\frac{\partial^2 v^+(x,t)}{\partial x^2} = (\gamma cs^2 + rcs) v^+(x,s) \Big|_{\gamma=l+l_m} \quad (28)$$

where $v^-(x,s)$ is the voltage when both lines are switching in opposite directions. l , c , and r are the self-inductance, self-capacitance, self-resistance per unit length of the line, respectively. l_m and c_m are the mutual inductance and capacitance per unit length, respectively, between the victim line and the aggressor line.

As (27) and (28) are analogous to (6), their respective SS representation are as follows:

$$SS^+(d,s) = SS(d = f(l_{eff}, c_{eff}), s) \Big|_{l_{eff}=l+l_m; c_{eff}=c} \quad (29)$$

$$SS^-(d,s) = SS(d = f(l_{eff}, c_{eff}), s) \Big|_{l_{eff}=l-l_m; c_{eff}=c+2c_m} \quad (30)$$

For the typical interconnect in Section 2:

$$A^+ = \begin{bmatrix} 0 & \dots & \dots & -2.4 \times 10^{-44} \\ 0 & \dots & \dots & 0 \\ 0 & \dots & \dots & 0 \\ 0 & 0 & \dots & 0 \end{bmatrix}$$

$$B^+ = \begin{bmatrix} I \\ 0 \\ 0 \\ 0 \end{bmatrix}; \quad C^+ = \begin{bmatrix} 0 & 0 & 0 & 2.4 \times 10^{-44} \end{bmatrix}$$

With

$$A_{diag}^+ = 10^{11} \times \begin{bmatrix} -8.142 & 0 & 0 & 0 \\ 0 & -0.062 + j1.14 & 0 & 0 \\ 0 & 0 & -0.062 - j1.14 & 0 \\ 0 & 0 & 0 & -0.23 \end{bmatrix}$$

$$A^- = \begin{bmatrix} 0 & \dots & \dots & -3.9 \times 10^{-44} \\ 0 & \dots & \dots & 0 \\ 0 & \dots & \dots & 0 \\ 0 & 0 & \dots & 0 \end{bmatrix}$$

$$B^- = \begin{bmatrix} I \\ 0 \\ 0 \\ 0 \end{bmatrix}; \quad C^- = \begin{bmatrix} 0 & 0 & 0 & 3.9 \times 10^{-44} \end{bmatrix}$$

With

$$A_{diag}^- = 10^{11} \times \begin{bmatrix} -1.2 & 0 & 0 & 0 \\ 0 & -0.0054 + j1.28 & 0 & 0 \\ 0 & 0 & -0.0054 - j1.28 & 0 \\ 0 & 0 & 0 & -0.02 \end{bmatrix}$$

The postscripts ‘-’ and ‘+’ indicate common and differential modes, respectively.

Using (29) and (30),

$$SS^+(d,s) \xrightarrow{L^{-1}\{y(d,s)\}} y^+(d,t) \quad (31)$$

and

$$SS^-(d,s) \xrightarrow{L^{-1}\{y(d,s)\}} y^-(d,t) \quad (32)$$

3 Simulation Results

The state-space model was verified by simulating a single and coupled distributed RLC interconnect lines with source and load impedances, and the results of the model was then compared with those obtained from [13].

Fig.3 shows the phase shift in the nominal function for the differential mode –thus corresponding to the worst-case crosstalk. Almost a negligible phase shift occurs at low frequencies, but a gradual increase in the phase shift can be observed at relatively higher frequencies. The phase shift varies between 20% and 33% as the frequency fluctuates between 90 and 100 Hz. To counterbalance the above fluctuations in the phase – i.e. maintaining a constant phase shift – the frequency has to drop by approximately 11% and 17.5%, respectively.

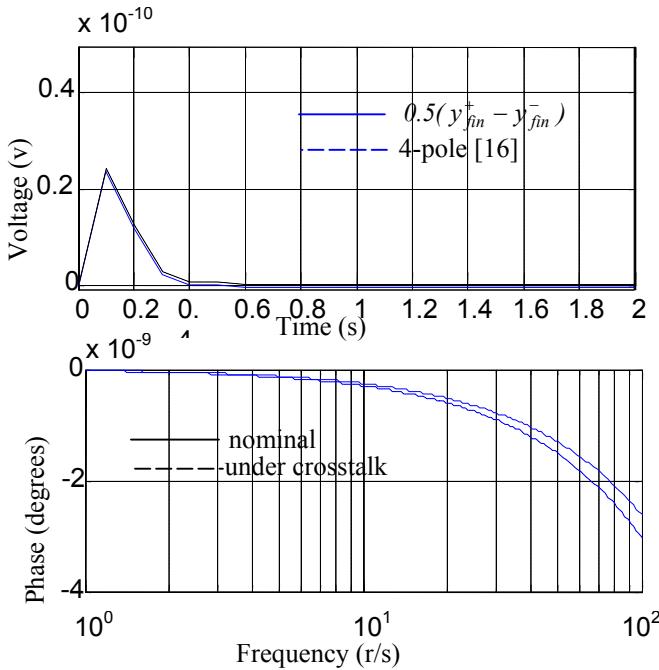


Fig.3 (a) crosstalk noise, (b) phase shift.

4 Conclusion

A state-space based model, which considers the distributed nature of an RLC interconnect, for investigation of crosstalk effects on circuit parameters was presented. The model can also provide useful information to estimate time-delay, and can easily be adapted to various applications such as interconnect optimisation for noise minimization.

References:

- [1] X. Qi, B. Kleveland, Z. Yu, S. S. Wong, R. W. Dutton, and T. Young, “On-chip inductance modelling of VLSI interconnects,” in 2000 IEEE Int. Solid-State Circuits Conf. Dig. Techn. Papers, 2000, pp. 172–173.
- [2] H.J. Kadim, L.M. Coulibaly, “EM-based Analytical Model for Estimation of Worst-Case Crosstalk Noise”, Proc. of IEEE Int. Symposium on Circuits and Systems, Kos, Greece, 21-24 May 2006.
- [3] L. Coulibaly and H.J. Kadim, “Analytical Ramp Delay Model for Distributed On-Chip RLC Interconnects,” 47th IEEE International Midwest Symp. on Circuits and Systems, Japan, July 2004, pp. I 457-I 460.
- [4] T. Sakurai, “Closed form expression for interconnect delay, coupling and crosstalk in VLSI,” IEEE Trans. Electronic Devices, Vol. 40, pp. 118-124, Jan, 1993.
- [5] Q. Yu, E.S. Kah, “exact moment matching model of transmission lines and applications to interconnect delay estimation,” IEEE Trans. VLSI Syst., Vol.3, No.2, pp. 311-322, June 1995.
- [6] R. Gupta, B. Tutuianu, L. Pileggi, “The Elmore delay as a bound for rc trees with generalised input signals”, IEEE Transactions on Computer-Aided Design, Vol. 16, No. 1, pp. 95 - 104, 1997.
- [7] H.J. Kadim, L.M. Coulibaly, “Wave-Propagation based Analytical Model for Distributed On-Chip RLC Interconnects”, Proc. of IEEE Int. Symposium on Circuits and Systems, Kos, Greece, 21-24 May 2006, in press.
- [8] L. T. Pillage and R. A. Rohrer, “Asymptotic waveform evaluation for timing analysis,” IEEE Transactions on Computer-Aided

- Design, Vol. CAD-9, No. 4, pp. 352 - 366, April 1990.
- [9] Odabasioglu A., et al, "PRIMA: Passive reduced-order interconnect macromodeling algorithm," ICCAD 1997, pp 58-65.
- [10] J. A. Davis and J. D. Meindl, "Compact distributed RLC interconnects Part I: Single line transient, time delay, and overshoot expressions" in *IEEE Transactions on Electron Devices*, vol.47, No.11, Nov2000.
- [11] L.M. Coulibaly and H.J. Kadim, "A Comparative Analysis of a Distributed On-Chip RLC Interconnect Model under Ramp Excitation", Proc. of IEEE EUROCON, International Conference on "Computer as a Tool" Belgrade, 2005, pp 519-522
- [12] H.J. Kadim and L.M. Coulibaly, "Time-delay Estimation: Two Comparative Models for Distributed On-Chip RLC Interconnects under Ramp Excitation," Proc. of the 23rd Norchip Conference, Oulu, Finland, November 2005, pp245-248.
- [13] L.M. Coulibaly, H.J. Kadim, "Analytical crosstalk noise and its induced-delay estimation for distributed RLC interconnects under ramp excitation," IEEE Inter. Symp. on Circ. and Sys., Japan, 2005, pp 1254-1257.