Proceedings of the 10th WSEAS International Conference on CIRCUITS, Vouliagmeni, Athens, Greece, July 10-12, 2006 (pp201-206)

A Multi-Cell Switch-Mode Power-Supply Concept Featuring Inherent Input Voltage Balancing

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Abstract: – A novel switch-mode power supply (SMPS) concept is presented which is especially suited to high input voltages. The topology is based on a multi-cell arrangement where individual DC-DC converter cells are connected in series regarding their input side whereas the isolated output stages of the cells are connected in parallel. The identical cells are realized as self-oscillating series-resonant converters operated at near unity duty cycle. Consequently, the cell only performs an isolation function, the voltage regulation is realized by a subsequent non-isolated DC-DC converter at low voltage level. The isolation stage is based on the well known half-bridge topology utilizing efficient standard medium-voltage MOSFETs. A very interesting feature of the proposed system is that it is characterized by an inherent equalizing of the input voltage of the individual cells without any control requirements. The paper gives a short introduction to the basic problems of SMPS for high input voltages, describes the basic operation of the presented topology and gives a dimensioning as well as simulation results and presents measurement results taken from a laboratory prototype.

Key-Words: – switch-mode power supply, SMPS, multi-cell topology, voltage balancing

1. Introduction

In comparison to office and residential applications, switch-mode power supplies (SMPS) for industrial systems often are characterized by increased input voltage levels. A good example is the auxiliary (housekeeping) power supply of a three-phase AC inverter for drive applications. To facilitate a defined braking behavior of the drive in case of power loss (mains failure), the housekeeping power has to be taken out of the main DC voltage link (cf. **Fig.1**). For inverters operated at the common 400...480V mains DC link voltages of 500...650V appear which may even rise to typically 800...900V in case of braking operation. Consequently, the housekeeping SMPS has to be designed for this high input voltage level.

Unfortunately, the well known basic SMPS topologies like fly-back or forward converters are not optimally suited for higher input voltages. The topologies mentioned are characterized by the fact that the blocking voltage capability of the applied power transistors has to be typically 1.5...2.5 times the maximum input voltage, i.e., semiconductor switches with blocking voltages in the range 1.2...2.2kV would be required. This, however, makes impossible the efficient application of power MOSFETs being the standard switching device for computer and household appliance SMPS. Due to the fact that MOSFETs are majority carrier devices their on-state resistance dramatically worsens for higher blocking voltage levels. MOSFETs are commercially available only up to 1200V blocking voltage and also in the 800... 1000V region the devices are comparatively expensive due to their in principle poor utilization of the silicon. An alternative would be the application of minority-carrier based devices, e.g., IGBTs. These devices, however, show much higher switching losses (especially for the voltage region under consideration) and, therefore, do not allow high switching frequencies which are essential to keep the size of the SMPS isolation transformer small.

As given by semiconductor fundamentals (e.g., [1], p.589) the on-state resistance $R_{DS,on}$ of power MOSFETs follows the maximum blocking voltage BV according the relation $R_{DS,on} \propto (BV)^{2.5...2.7}$ which is confirmed by a comparison of real transistors of approximately equal die size in the voltage region of 400...1000V (see **Fig.2**). This relationship suggests

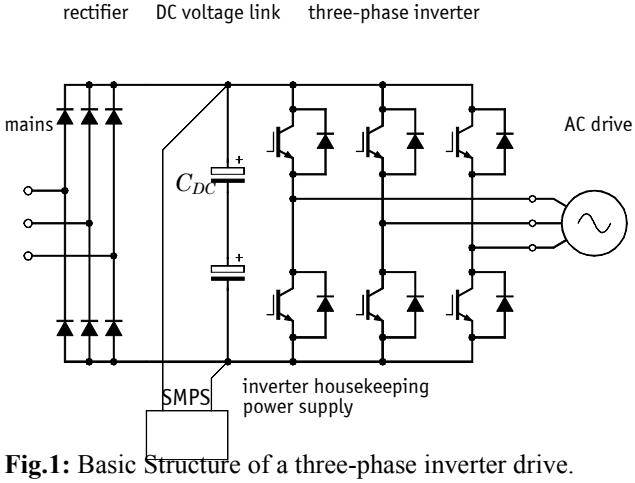

Fig.1: Basic Structure of a three-phase inverter drive.

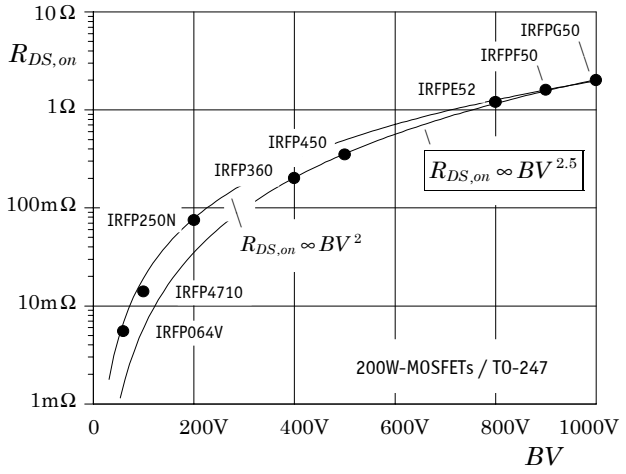

Fig.2: Comparison of on-state resistance of power MOS-FETs (≈equal die size) for different blocking voltages.

the split-up of the SMPS into several (say N) parts ("cells") connected in series in a similar way as this has been proposed for class-D power amplifiers [2]. With this split-up transistors of lower rated voltage can be used and the total on-state resistance of all transistors $\Sigma R_{DS,on} \propto N \cdot (BV/N)^{2.5...2.7}$ which determines the on-state losses is lowered for increased N by a factor of $1/N^{1.5...1.7}$.

The topology and the operating principle of a SMPS based on a series arrangement of individual switching cells will be presented in the following section. Afterwards, in section 3 the stationary operating behavior is analyzed and dimensioning guidelines are derived. Section 4 presents simulation results and measurements of a specific laboratory model. Finally, an interesting extension of the concept where the SMPS is also used for balancing the DC link electrolytic capacitors of the main drive converter is proposed in section 5.

2. Multi-Cell SMPS

As shown in **Fig.3** the proposed SMPS topology is formed by a group of identical half-bridge stages which are connected in series at the input side but in a parallel manner at the output. The switching cells are completely self-sustaining, each cell is gated by its own driver oscillator, however, using equal switching frequency nominal values. The duty cycle is adjusted to be slightly lower than 100% to prevent cross conduction and achieve zero voltage switching. As will be shown in section 4 the gate drive can be implemented very easily using integrated circuits originally designed for lamp ballast control.

Due to the operation using maximum duty cycle and due to zero voltage switching such stages achieve a very good efficiency [3]. However, they do not permit any voltage regulation. In fact the cell acts as a pure isolation stage which only opens the possibility of the mentioned series/parallel concept. The nominal output voltage of the cell is directly linked to its input voltage, the transmission ratio is defined by

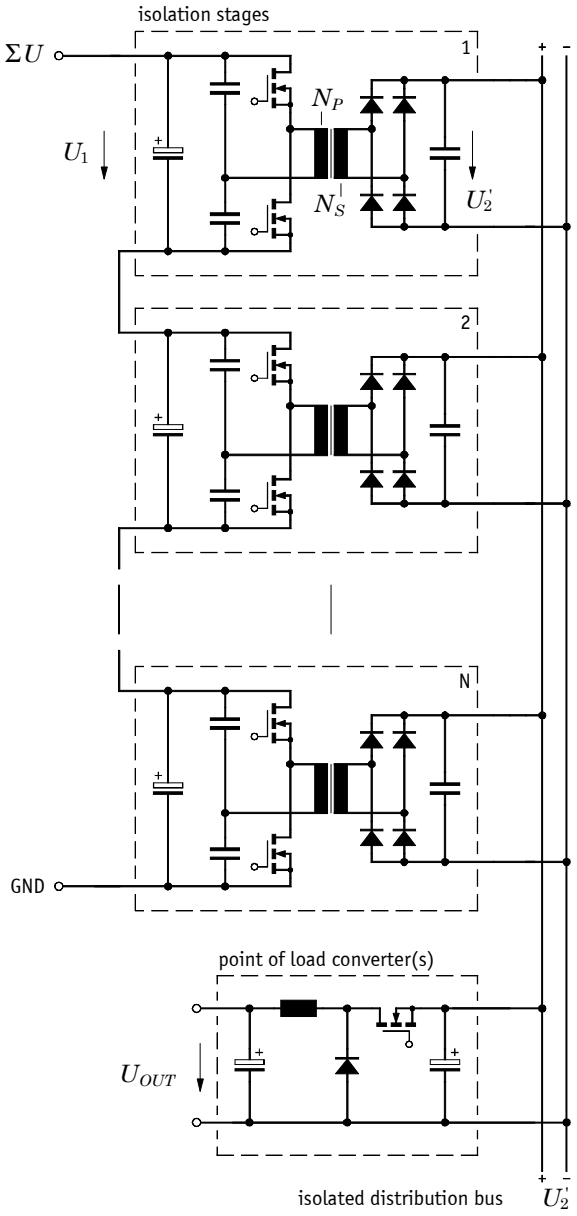

Fig.3: Basic circuit diagram of the proposed SMPS based on a series arrangement of self-oscillating half-bridges.

the transformer windings: $U_2' = 1/2 \cdot U_1 \cdot N_S/N_P$ (the factor 1/2 originates from the fact that the transformer primary results to $\pm U_1/2$ for half-bridge circuits). If, e.g., the total input voltage is specified to be $\Sigma U = 900$V and $N = 3$ has been chosen the nominal cell output voltage results to $U_2' = 30$V if a transformer winding ratio of 5:1 is assumed. This low voltage level ideally is suited to be distributed to one or several non-isolated point-of-load converters to achieve load voltage regulation to, e.g., $U_{OUT} = 12$V as well as current limitation. Such converters usually are based on buck topology and can be realized easily by the application of integrated power regulators ICs which are offered at low-cost by several semiconductor manufacturers (e.g., the series LM500x by National Semiconductors Inc.). The analysis of the non-isolated point-of-load converter will not be treated in detail in this paper, however.

3. Stationary Operating Characteristic

The isolation stages are operated in series-resonant mode with capacitive output filtering. This mode has been chosen due to the expected good efficiency based on the near unity duty cycle and the zero-voltage turn-on of the power transistors. Furthermore, the blocking voltage stress on all semiconductors is well defined and the transformer leakage L can be utilized as resonance inductance. Therefore, as opposed to, e.g., transformers for flyback converters a certain amount of leakage is of advantage here.

In the following, the characteristics of the stationary operation shall be calculated. To simplify the considerations the total cell input voltage here shall be denoted as $2U_1$ (**Fig.4**). The system is characterized by different conduction states (A→B→C→D) defined by the polarities of the input voltage u_1 and of the reflected secondary voltage u_2. Whereas the polarity of u_1 is defined by the control circuit, the polarity of u_2 is determined by the direction of the resonant current i_L. For state A, u_1 and u_2 show equal direction and the (small) difference $\Delta U = U_1 - U_2$ is applied to the LC series resonant circuit. This results in a circular shaped system trajectory around the center point $[+\Delta U,0]$ (cf. $u_C Z_0 i_L$-diagram of **Fig.5** (a), $Z_0 = \sqrt{L/C}$ defines the characteristic impedance of the resonant network). Because the system operates with a switching frequency f_S above the natural frequency $f_0 = 1/(2\pi\sqrt{LC})$, the input voltage u_1 changes its polarity at instant 1 due to the turn-off of the high-side transistor before i_L becomes zero. Consequently, the system transits to state B where the sum $U_1 + U_2$ causes a steep current reduction (cf. Fig.5 (b)) according to the circular trajectory with the center point $[-(U_1+U_2),0]$. At instant 2, the current i_L becomes negative, the current in the rectifier diodes commutates and u_2 again shows equal (i.e., negative) polarity as u_1 (state C); now $[-\Delta U,0]$ is the new center of the trajectory valid until the lower power transistor turns off at instant 3 and the system passes over to state D (center $[U_1+U_2,0]$) which completes a full cycle in instant 4.

For the practical realization of the converter it is of importance that, in general, $U_1 + U_2 >> \Delta U$ is valid. With this assumption the system trajectory in good approximation shows the shape of Fig.5 (c), i.e., the current contribution of states B and D to i_2 can be neglected ($t_{1,2} \to 0$, Fig.5 (c)). With this and using the conduction angle $\alpha = \pi / (f_S/f_0)$ the equations

$$(\hat{u}_C + \Delta U)\cos(\pi - \alpha) = \hat{u}_C - \Delta U \qquad (1)$$

and

$$Z_0 I_2 = (\hat{u}_C + \Delta U)\frac{1}{\alpha}\int_0^{\alpha} \sin(\omega t)\, d\omega t \qquad (2)$$

can be derived according to the geometrical relations given by Fig.5 (c) and according to the fact that the average value of i_2 (i.e., the rectified inductor current i_L) in the stationary case is defined by the load current I_2. Evaluation of Eq.(2) and rearranging using Eq.(1) finally leads to

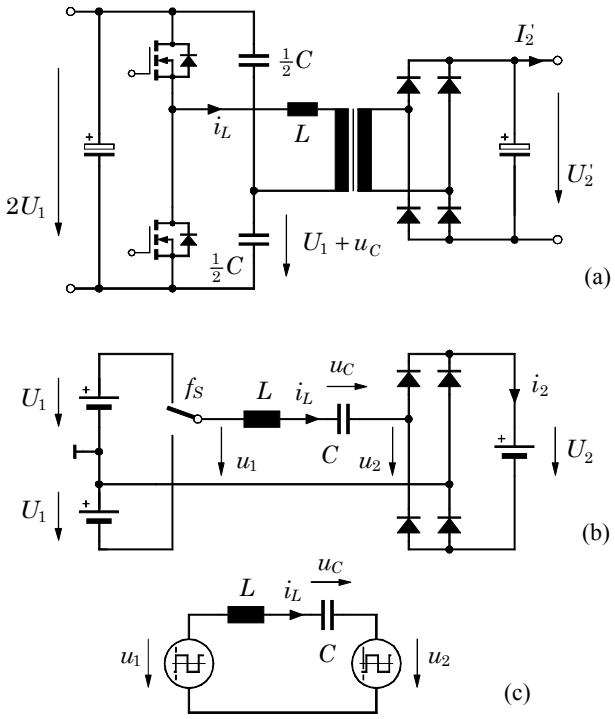

Fig.4: Schematic diagram of the series-resonant converter (a) and corresponding equivalent circuits (b), (c).

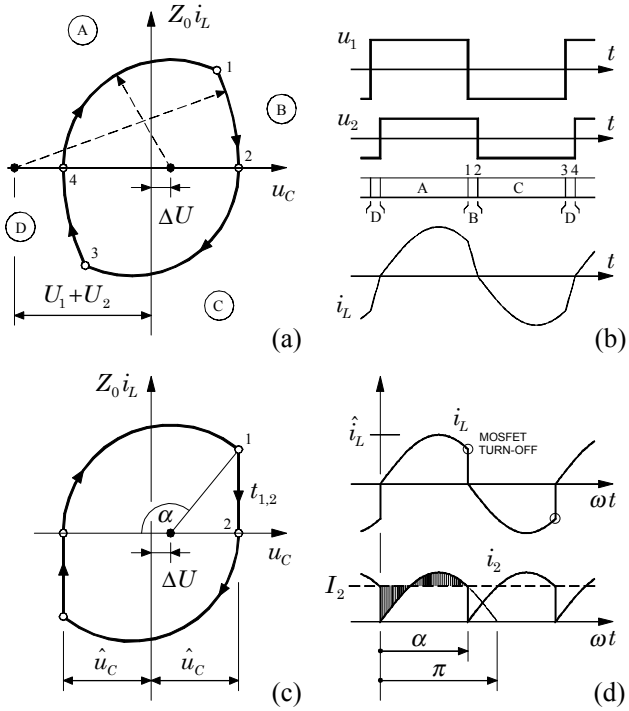

Fig.5: System trajectory (a) and time behavior (b) of the series resonant converter; (c), (d): simplification valid for $U_1 + U_2 >> \Delta U$; i_2: output current of the rectifier (Fig.4 (b)).

$$\Delta U = I_2 \cdot R_{OUT} \quad \text{with} \quad R_{OUT} = Z_0 \frac{\alpha}{2}\frac{1+\cos\alpha}{1-\cos\alpha} \qquad (3)$$

and

$$\hat{u}_C = I_2 \cdot Z_0 \cdot \frac{\alpha}{2} = \frac{I_2}{4 f_S C} \quad . \qquad (4)$$

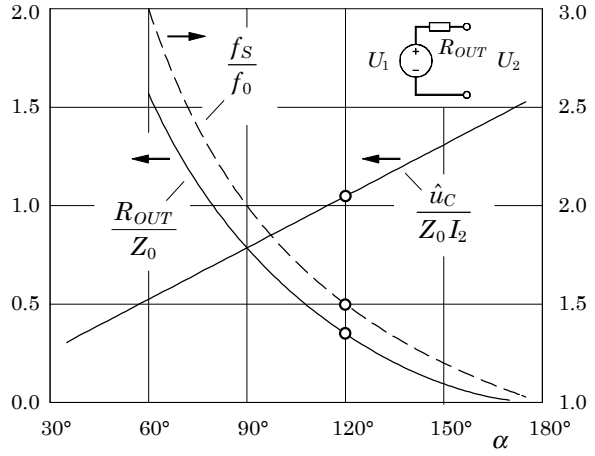

Fig.6: Dependency of the characteristic dimensioning parameters on the conduction interval α.

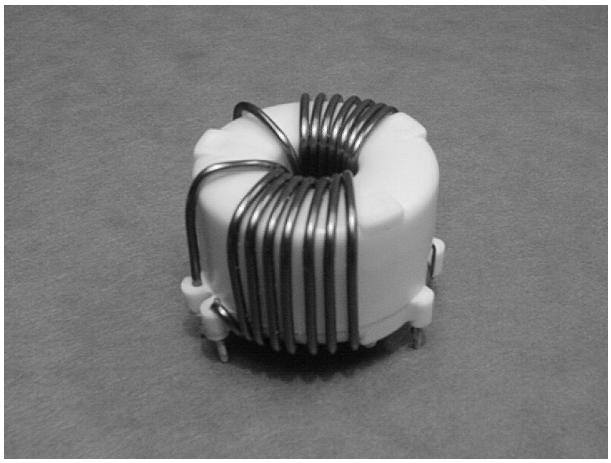

Fig.7: Toroid transformer as used in halogen lamp ballasts. Primary winding fully encapsulated.

These equations state that for a given switching frequency (i.e., a fixed conduction interval α) the output voltage U_2 decreases proportional to the load current I_2, the converter shows a quasi-ohmic (non-dissipative!) output impedance (current-independent output resistance R_{OUT}, cf. equivalent circuit given in **Fig.6**, where Eqs. (3) and (4) are evaluated graphically). Due to the fact that R_{OUT} mainly is determined via Z_0 by L (the transformer leakage inductance), its value usually is comparatively low related to the nominal load resistance U_2/I_2. The appearing load voltage drop $\Delta U = R_{OUT} \cdot I_2$ easily can be corrected by the point-of-load converter. On the other hand, the non-zero value of R_{OUT} is essential for the applicability of this concept, because it guarantees the current sharing of all cells and with this, in an indirect manner, the balancing of the individual input voltages of the series connected cells.

4. Dimensioning Example

As is indicated by Fig.5 (d), a dimensioning using a high value of α would be of advantage since the current which the MOSFETs have to switch-off is reduced as a fact of the resonance principle ($i_L \rightarrow 0$). A value of $\alpha = 150°...170°$, however, gives a very low R_{OUT} (cf. Fig.6) which worsens the current sharing. Furthermore, R_{OUT} also acts as a (non-dissipative!) damper for the resonant circuit. For a practical realization, therefore, a dimensioning of $\alpha = 120°$ (i.e., $f_S = 1.5 f_0$) is a good trade-off leading to $R_{OUT} = \pi/9 \cdot Z_0 \approx 0.35 \cdot Z_0$.

Due to the high input voltage level the converter has to have a very good isolation barrier. Therefore, a transformer is applied which features a strict separation of the windings. Electronic ballasts for low-voltage halogen lamps very often are equipped with a toroid transformer where the primary and secondary windings are separated very strictly by different coil former elements. The primary winding shows a full encapsulation, the isolated secondary winding is located at the transformer surface (**Fig.7**). Despite the

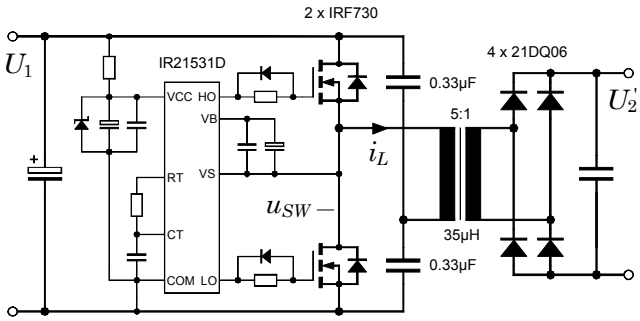

Fig.8: Schematic diagram of the power circuit.

fact that this component is a low-cost device, the transformer shows very good electrical parameters. Its sole "drawback", the somewhat increased stray inductance is rather of advantage for this application. The applied transformer, based on a ∅25x14mm toroid core is characterized by the parameters:

primary:	80 turns	$L_1 = 30$mH
secondary:	2x8 turns	$L_2 = 1.2$mH
leakage (primary side):		$L = 35$µH.

Both secondary windings are connected in series to get a 5:1 transformation ratio in order to receive the aimed 10:1 input-to-output voltage ratio. If a switching frequency of $f_S = 50$kHz and $\alpha = 120°$ are chosen, one gets for the residual parameters:

natural frequency:	$f_0 = 50\text{kHz} / 1.5 \approx 33\text{kHz}$
resonance capacitors:	$C = 2 \times 0.33\mu\text{F}$
characteristic impedance:	$Z_0 = 7.3\Omega$
output imp. (primary side):	$R_{OUT} = 2.5\Omega$.

As depicted in **Fig.8** the control of the converter shows a very low effort if an integrated gate drive IC (IR21531D, originally designed for energy saving lamps) is applied. The operating frequency is set by R_T and C_T; the IC provides an internal fixed dead

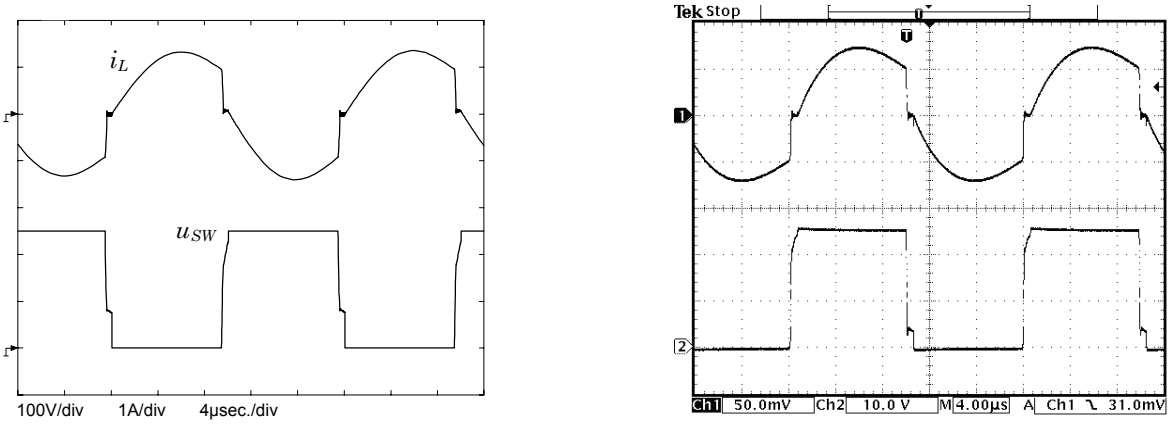

Fig.9: Simulation results (left hand side) and measurements (right hand side) taken from a 60W laboratory prototype. Parameters: $U_1 = 250\text{V}$, $U_2 \approx 25\text{V}$, $R_{LOAD} = 10\Omega$, $I_2 \approx 2.5\text{A}$.

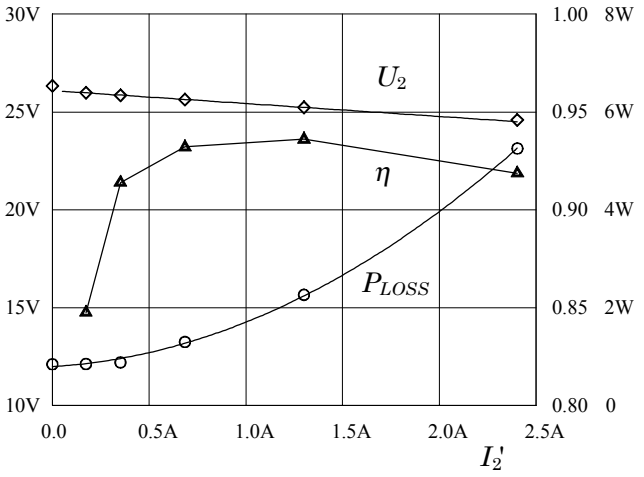

Fig.10: Laboratory prototype measurement results.

time of 0.6µs to prevent cross-conduction and enable low-loss ("zero-voltage") turn-on at higher load currents. The secondary-side rectification is realized by a full-bridge topology. The measurements taken from the laboratory model very closely match the results gained by PSpice-simulation (**Fig.9**). As indicated by the lower traces of Fig.9, no real zero-voltage switching is achieved. Despite this, the converter shows a good efficiency of up to ≈94% (**Fig.10**). It has to be kept in mind that although Schottky-diodes are used, the passive rectifier significantly contributes to the total losses. For converters with active rectifier stages employing modern low-voltage power MOSFETs or for converters dimensioned for higher output voltages efficiency values of above 97% seem to be achievable [3], [4].

The output voltage shows the expected ohmic behavior $U_2 = U_{2,0} - R_{OUT} \cdot I_2'$ as discussed in section 3. However, the actual value of R_{OUT} is increased significantly as predicted by Eq.(3) due to the ohmic losses of the MOSFETs ($R_{DS,ON} \approx 1\Omega$), of the transformer (copper losses) and of the rectifier. In the case at hand a value of $R_{OUT} = \Delta U_2 / \Delta U_2 \approx 0.6\Omega$ is valid.

5. Input Voltage Balancing

A very interesting characteristic of the proposed SMPS concept is that the topology according to Fig.1 inherently balances the input voltages $U_{1,i}$ of the individual switching cells so that the total input voltage ΣU is partitioned equally to all N cells. This feature is immediately clear if the equivalent circuit of the whole system is observed (**Fig.11**). Due to the fact that all cells are connected in parallel at their secondary side and in series on the input side, they show equal values for U_2 and I_1. Assuming equal output impedances R_{OUT} evaluating Fig.11 (a) after a short calculation gives

$$U_{1,i} = \frac{\Sigma U}{N} \quad \text{and} \quad U_2 = \frac{\Sigma U}{N} - I_{2,tot} \frac{R_{OUT}}{N} \ , \quad (5)$$

i.e., that ΣU in the idealized case is partitioned equally independent of the load current and concerning the output voltage all R_{OUT} act in parallel.

To demonstrate the balancing behavior of the system two cells have been arranged according to Fig.11 (b). An additional resistor R_A has been inserted for emulating a distortion I_A of the current distribution (e.g., as a result of different leakage currents of the input capacitors). As indicated by Fig.11 (c), the center point voltage U_{CP} shows a very stiff behavior, $U_{1,1} = U_{1,2} = \Sigma U/2$ is satisfied with good accuracy.

The excellent balancing behavior suggests a further specific application of the concept. With the exception of low power systems, drive converters usually are operated from a three-phase mains. As described in section 1, the DC link voltages may rise up to 800...900V in case of motor braking or if active rectifiers are used. However, due to technology limitations electrolytic capacitors mainly are available only in the voltage range < 500V. Consequently, the DC voltage link of such converters in general is equipped with a series connection of two or more capacitors. To achieve a homogenous voltage distribution the capacitor manufacturers usually demand balancing resistors R_B connected in parallel to each

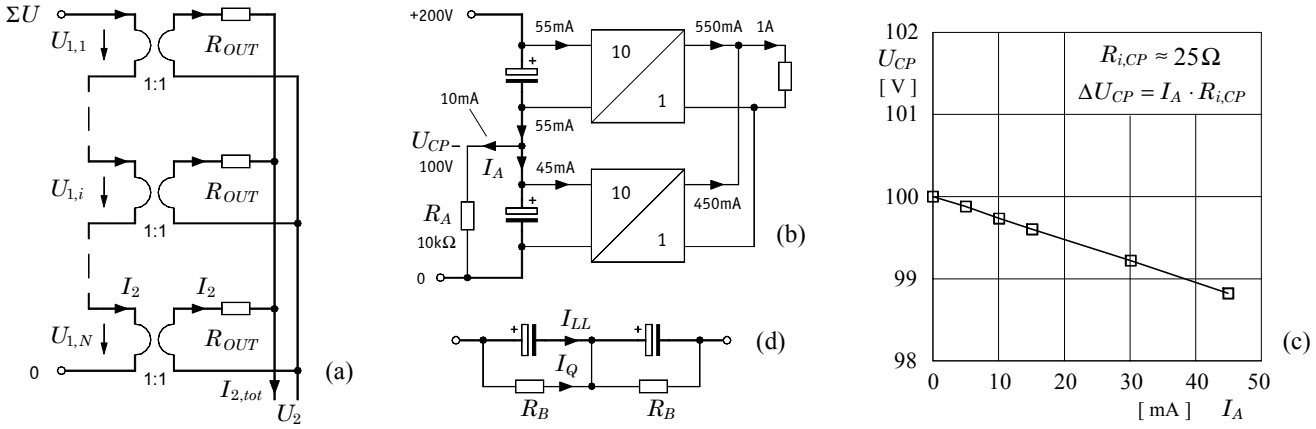

Fig.11: Inherent balancing of converter input voltages. (a) Equivalent circuit diagram, (b) testing circuit for evaluating the voltage balancing, (c) center point voltage U_{CP} in dependency on the current distortion I_A, (d) passive capacitor balancing using dissipative voltage divider resulting in high permanent balancing losses caused by the quiescent current $I_Q >> I_{LL}$.

capacitor to form a resistor voltage divider (cf. Fig.11 (d)). These resistors have to be dimensioned such that the appearing quiescent current I_Q is substantially higher than the leakage currents I_{LL} of the capacitors. Unfortunately, however, the leakage current of electrolytic capacitors may vary in a wide region, dependent on aging status and temperature. As a rule of thumb, it is usually recommended to choose R_B such that $R_B \cdot C_{DC} \approx 50$ sec. is valid [5]. For a 5000µF capacitor this, e.g., gives a balancing resistor of $R_B = 10\text{k}\Omega$ leading to a quiescent current of I_Q =25mA (@250V capacitor voltage) and resulting in additional losses of 2 x 250V x 25mA=12.5W for the total converter. If the converter is permanently operated or at least powered by the mains, this losses sum up to a substantially energy consumption of more than 100kWh/year! The problem of this balancing method is that R_B has to be selected regarding a worst-case condition of the capacitors but high additional losses also exist even if the capacitors show much smaller actual leakage currents.

If the SMPS of the drive converter, however, is realized using the proposed concept (Fig.2), the balancing resistors R_B can be omitted if the SMPS cells are fed by the individual electrolytic capacitors C_{DC} of the DC voltage link of the drive. It has to be noted, however, that the balancing operation as described before requires a specific minimum load of the SMPS and is not given in the case of no-load operation. This, however, is not a serious problem for practical systems where the SMPS usually shows a considerable basic load.

6. Conclusions

A SMPS concept has been proposed especially suited for higher input voltages as needed, e.g., for three-phase drive converters. The topology consists of an arrangement of identical isolation stages connected in series at the input side but in parallel regarding the output side. The isolation stages operate at near unity duty cycle and do not provide voltage regulation. This, and also the current limitation in case of short-circuit is provided by the subsequent point-of-load converter which can be realized in a simple way by application of buck converter ICs. The proposed concept shows good efficiency and can be realized with low effort using control circuits and transformers known from lighting ballast applications. The system performs inherent input voltage balancing behavior. This feature can be utilized beyond the basic SMPS operation to avoid the widely used DC link balancing resistors of drive converters which opens a considerable potential for energy saving.

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