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Simulation of Electro-Thermal Effects in Device and Circuit

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Abstract: This papers describes a computer environment that supports the simultaneous electrical and thermal interactions at device and chip level. A circuit simulator and a finite element thermal simulator are coupled through an application program interface that synchronizes the transfer of information between two simulators. Temperature dependent thermal conductivity of silicon is taken into account by solving the nonlinear heat diffusion equation. This method is applied to perform electro-thermal analysis of bipolar junction transistor (BJT) to predict the temperature distribution and the device performance in a circuit. The performance of the device was evaluated by coupling both electrical and thermal analysis. In addition, power dissipation was computed for each part of the device including collector, emitter and base.

Key-Words: Microelectronics, Electro-thermal Analysis, Thermal Modeling, Numerical Simulation, Si BJT and Thermal Effects.

1 Introduction

Shrinking device sizes and higher integration densities are giving rise to a number of new challenges in designing the next generation of integrated electronic circuits. Many roadmaps now recognize advanced electro-thermal analysis as one of the major challenges in electronic product innovation [1]. The reasons are due to ongoing push of technology towards higher speed and device density and/or higher power and increased complexity. The compounding effects of size reduction and increased power lead invariably to higher heat generation per unit area. Without accurate prediction of the temperature at device and chip level, it is impossible to determine properly the devices' electrical characteristics and therefore devices may be at risk of overheating thus causing early device failure [2,3].

Many efforts have been performed to obtain temperature gradients in time and space at device level and to attain a consistent electro-thermal simulator to be able to evaluate the circuit performance at different temperatures prior to the manufacturing [4-8].

There are two principal methods to model thermal issues in electronic design on system, board, package, chip, and device level, the relaxation method and the direct method.

Relaxation technique: In this technique an interface program couples two powerful electrical and thermal simulators. Hence, almost any thermal model can be applied and any nonlinearity of the system can be easily considered. The advantage of this technique is the relative simplicity of its implementation.

Direct technique: In this technique [5] a number of electrical and thermal equations are solving simultaneously. This method requires some assumptions and changes in the actual model so it can be evaluated with a standard model [9]. The drawback is that it requires a more complex implementation than the relaxation method and specialization of electrical or thermal problem solving methods cannot be implemented.

Typical devices such as, bipolar junction transistors (BJT) have a specific current density characteristic that makes them suitable to be implemented in short-pulse, high power applications [10]. Since BJTs commonly utilize in high power applications, temperature effects on device performance need to be carefully considered.

The rest of the paper is organized as follows. In section 2, the methodology and implementation of an electro-thermal simulator using the relaxation method is described. In section 3, the capabilities of the the simulator is demonstrated on a benchmark problem and the obtained results are evaluated. Conclusion and further work are presented in section 4.

2 Methodology

An algorithm was developed in MATLAB [11] to create an interface between SPICE [12], as the electrical simulator, and COMSOL [13], as the

thermal simulator. By implementing this algorithm, an electro-thermal simulator to analyze different electronic circuits and devices has been obtained. The implementation of the electro-thermal simulator requires: a) communication between two simulators to receive and to send calculated parameters to another simulator b) time step c) convergence test. The developed algorithm in MATLAB controls these requirements. The flow chart of electro-thermal simulator is shown in Fig. 1.

The procedure begins by computing power dissipation in SPICE at a given time step and temperature. This power dissipation is imported to COMSOL as the heat source of the thermal model through MATLAB. The three-dimensional finite element model generated by COMSOL is used to obtain temperature distribution in the thermal model according to the defined heat source. Time dependent thermal equation is solved in COMSOL at a given time step to extract the junction temperature, and temperature profile. The circuit simulator waits while temperatures are calculated by thermal simulator. Thus, for each iteration of the circuit simulator, several thermal iterations might be required since temperature becomes a new parameter for the circuit simulator. Therefore a more accurate thermal behaviour of the system is available. The new junction temperature is imported to SPICE and the power dissipation is up-dated, by taking the new temperature profile into account. Every time that SPICE computes new power dissipation according to the new temperature profile, this dissipated power is compared to the previously calculated power dissipation. The loop should be continued until the difference is smaller than the specified error, ε. If the convergence achieved, the next time step will begin.

The convergence behavior of simulator may be affected by the choice of proper initial conditions for the first time interval. Each time interval applies the results of the previous time step as its initial condition.

The advantage of the proposed method is the availability of two powerful circuits and thermal simulator. Therefore, complex electrical and thermal issues can be properly addressed. For instance, temperature dependent thermal conductivity of semiconductor material can be considered in the thermal modeling process. In addition, detail three-dimensional thermal analysis of the internal structure of the semiconductor device and the inclusion of circuit metal interconnects of devices can be performed.

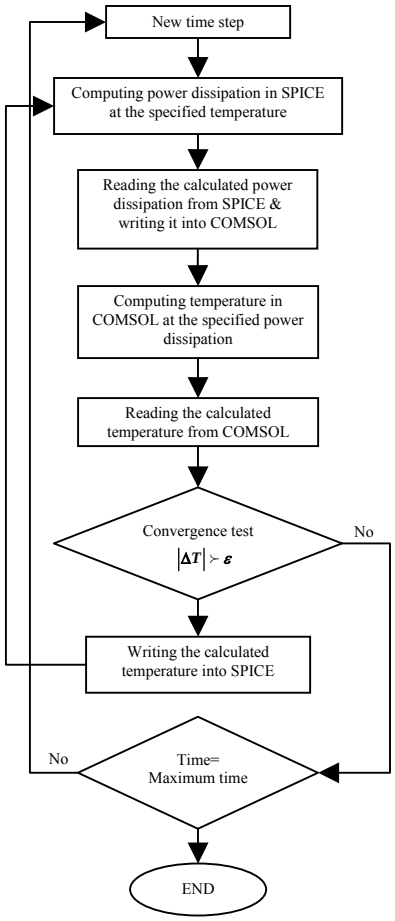

Fig. 1: Flow chart of electro-thermal simulator.

3 Application Example

Three-dimensional thermal simulation was performed for the active device (BJT) located on a 1cm×1cm×0.035 cm chips. The size of the active device was 400 μm ×300 μm ×10 μm [14]. To verify the simulator at this stage, only one device has been considered. The device was modeled in SPICE, whereas the chip structure was modeled in COMSOL.

In SPICE, Q2N3904 silicon bipolar transistor was biased in a moderate operating point. The collector-emitter voltage, Vce, was 10V and the collector current, Ic, was 182.37mA. At ambient temperature (27ºC), when input voltage of base-emitter, Vbe, was 0.85 V DC, the power dissipation was computed 1.83 Watts.

The three-dimensional finite element model shown in Fig. 2 was developed to simulate the thermal behavior using COMSOL code. The chip and the active device were modeled using approximately 11000 solid elements as shown in Fig. 2.

The governing heat transfer equation is given in the following form:

$$\nabla\left(k(T)\nabla T\right)+Q=\rho c_p\frac{\partial T}{\partial t}$$

subjected to thermal boundary condition:

$$k\frac{\partial T}{\partial n}+hT=f$$

and the initial temperature condition:

$$T_{t=0}=F$$

Where T denotes the temperature (°C), t denotes time (s), ρ (kg/m³) is the density, Cp (J/kgºK) is the specific heat capacity, k (W/mºK) is the thermal conductivity and ko is the thermal conductivity at 300ºK. They were specified according to silicon characteristics in this model. Q (W/m³) is the heat source density which was defined according to the power dissipation. h is the heat transfer coefficient (W/(m²°C)), f is an arbitrary function, F is the initial temperature and n is the outward direction normal to the surface. The heat diffusion equation is non-linear by virtue of the thermal conductivity being temperature dependent.

The following boundary conditions were applied: There is a thermal resistance at the backside of the substrate. Therefore, the backside heat flux, q W/m², was defined as:

$$q=\left(\frac{1}{r_{th,b}}\right)\times\left(T_{amb}-T\right)$$

Where $r_{th,b}=R_{th,b}\times A_b$. A_b is the backside area. $R_{th,b}$ was obtained by measurement in [7] equal to 16 K/W. Thermal isolation was considered at the side walls and the top.

Silicon thermal conductivity was considered nonlinear [10]. The thermal characteristics used for silicon are listed in Table 1 [12]. An initial temperature of 27°C was applied to computational domain.

Table 1: Silicon thermal characteristics.

ρ (kg/m³)	2330
Cp (J/kgºK)	703
ko (W/mºK)	163
k (W/mºK)	$ko\times 163\times\left(\frac{T}{300}\right)^{\left(\frac{-4}{3}\right)}$

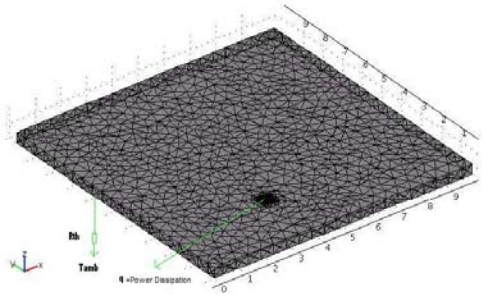

Fig. 2: Finite element model and boundary conditions.

The temperature contour obtained from the finite elements simulation, with a device power dissipation of 1.83W, is shown in Fig. 3.

As shown in Fig. 3, the maximum temperature was 88.4ºC. It can be observed that the maximum temperature occurred at the device junction (Tj).

During coupled simulation SPICE sends the power dissipation P of the transistor and receives the temperature Tj of the device from COMSOL.

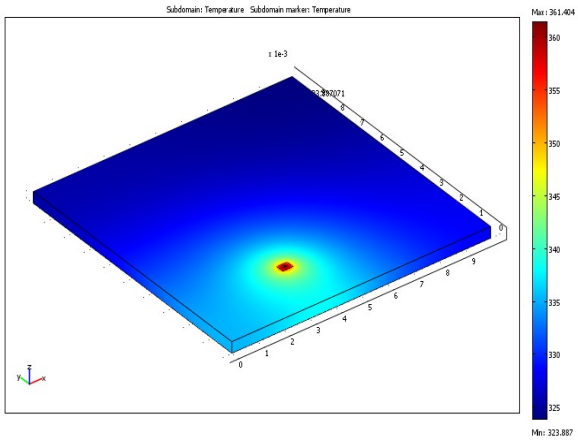

Fig. 3: 3D temperature distribution at a power dissipation of 1.83W.

The power dissipation-temperature curve is also shown in Fig. 4. It indicates that the converged temperature is 107.2°C. Power dissipation increased from 1.83W to 4.5W at Tj. This indicates the importance of an electro-thermal simulation.

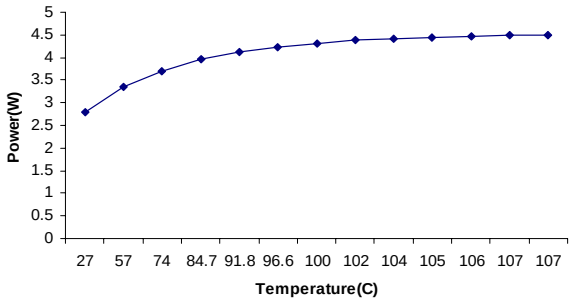

Fig. 4: Device power variations versus its temperature.

Fig. 5 shows the variations of collector current versus collector-emitter voltage when temperature rises to Tj. Ic varied from 183mA to 448 mA. Hence, the operating point changes.

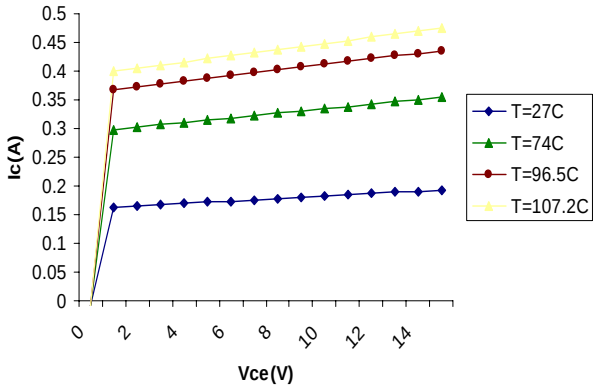

Fig. 5: Ic versus Vce while device was reaching its junction temperature.

As noted earlier, during the thermal simulation efforts the device has been modeled as a flat plate. This model has been improved to take into account more detailed structure of semiconductor device which include substrate, collector, base and emitter.

Thermal simulation was performed on the device itself to investigate temperature distribution in base, emitter and collector structure, when the device reached its junction temperature.

The following device dimensions were considered: collector volume = 400×300×10μm³, base volume = 150×150×0.8 μm³ and emitter volume = 5×5×0.5μm³. Heat source in each subdomain is the power dissipation density of the subdomain. Considering the operating point at collector-emitter voltage of 10V and collector current of 182.37mA, collector power dissipation was 1.83W, emitter power dissipation was 1.8W and base power dissipation was 0.0018W. As the result of the previous simulation shown in Fig. 3, the maximum temperature in the chip increased, however, the substrate temperature remained reasonably constant. Therefore, to set the boundary conditions of the device, the backside was considered as the ambient temperature which was 27ºC in this example. The side walls and the top were thermal insulation.

Fig. 6 indicates temperature distribution in different parts of the device. The temperature distribution inside device reveals substantial temperature difference between major heat source located in collector area and thermally sensitive area of emitter-base junction. The junction temperature was computed 87ºC. Fig. 6 indicates that the emitter is the hottest part of the device.

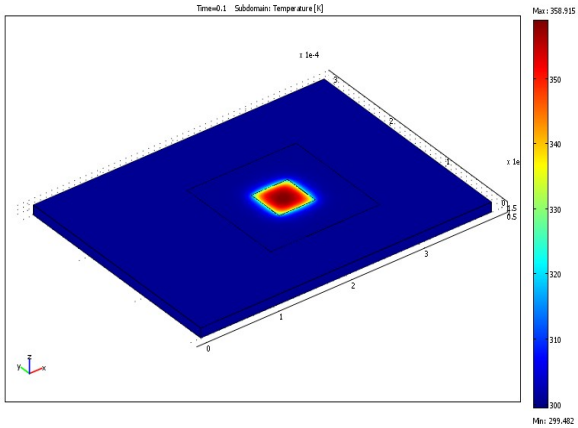

Fig. 6: Temperature distribution in the BJT.

4 Conclusion

Based on the relaxation approach, a methodology and an algorithm to analyze the electro-thermal behavior of device and integrated circuits has been presented. A circuit simulator and a finite element thermal simulator were coupled through an application program interface that synchronizes the transfer of information between two simulators. Thermal simulator is able to cope with the material non-linearity of semiconductor material and complex geometry. This is based on the application of non-linear heat flow differential equation in semiconductor material. It has been shown that thermal issues are critical and must be considered during their early design phase. The simulation results indicate that the electro-thermal simulator can quickly find the temperature profile of the chip. In addition, detail analysis of internal structure of the semiconductor device indicates substantial temperature difference between major heat source located in collector area

and thermally sensitive area of emitter-base junction. Future work will be directed to the extraction of compact electro-thermal model of electronic systems.

Acknowledgments:
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