4th WSEAS International Conference on ELECTRONICS, CONTROL and SIGNAL PROCESSING, Miami, Florida, USA, 17-19 November, 2005 (pp.167-168)

A Novel CCII Based Differential SC Resonator

Hooman Kaabi, Ahmad Ayatollahi
Electrical Engineering Department
Iran University of Science and Technology
Narmak, Tehran 16844
IRAN
http://www.sei.ir

Abstract: - A Novel Switched capacitor Resonator circuit based on CCII is proposed. The new Circuit is the CCII based version of I2P Resonator.

Key-Words: - RESONATOR, CCII, SC Filter, SC Circuit

1 Introduction

Direct digitization of signals in wireless communications needs band-pass ΣΔ modulators. They are used to digitize the received analog signal at an intermediate center frequency. These modulators are usually implemented by high speed switched capacitor resonators, which are tuned to a particular frequency. A resonator must be designed such that it has a sharp resonant peak at a specific center frequency. There exist many resonator circuits to implement SC band pass ΔΣ modulators and filters for high-frequency applications, such as : the 'lossless-discrete integrator' (LDI) [1], 'two-delay loop' (TDL) [2] and 'pseudo-two-path' (P2P) type [3] and finally 'Integrating two path' I2P. The most recent one is I2P which is claimed to have superior performance due to center frequency insensitivity to circuit imperfections [4].
However, because of bandwidth limitation and physical circuit imperfections, the resonance peak gain and/or the center frequency are degraded in existing architectures.
Due to inherent high frequency capability of CCII building block [5], it is an attractive candidate for replacing OpAmps in traditional resonator circuits. The new structure is a CCII version of I2P resonator. Thus inherits all of I2P advantages plus higher frequency operation due to utilizing CCII building blocks.

2 Proposed Resonator

Resonator Equation: the input-output relationship of a discrete-time resonator is :

$$v_{out}(n) = v_{in}(n-1) - v_{out}(n-2) \quad (1)$$

This corresponds to a z-domain transfer function of:

$$H(z) = \frac{z^{-1}}{1+z^{2}} \quad (2)$$

2.1 Resonator Circuit

The circuit is shown in fig. 1.

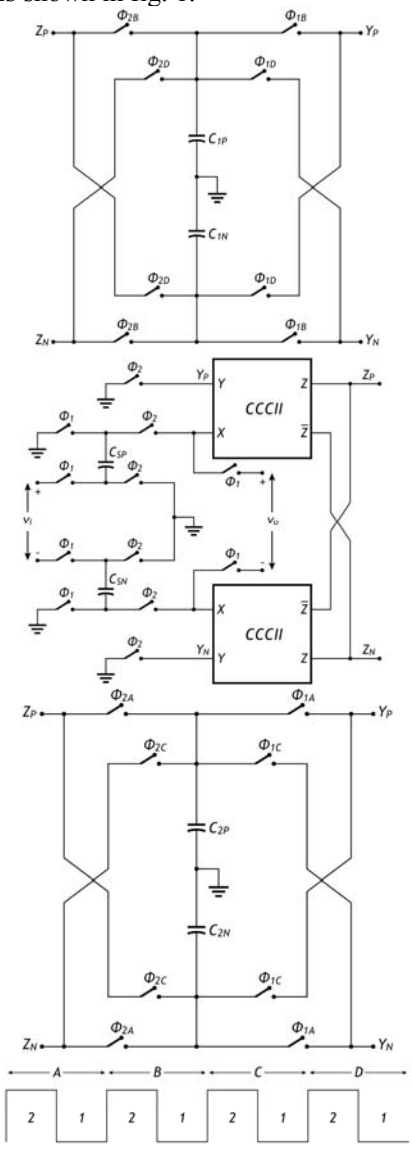

Fig.1 Proposed Resonator

It is based on CCII integrators proposed in an earlier work [7]. To be fully differential input-output operation, the compound CCII is incorporated. The circuit operation is similar to the traditional I2P circuit. Two pairs of integrating capacitors are sequentially connected to the integrating circuit in an interlaced manner. The differential voltage occurring two clock pulses earlier is stored in the *C1* Capacitors during odd clock phases. The pair is interchanged in the next clock phase to implement the resonator input-output equation (1).This operation is provided for the *C2* capacitor pair in even clock phases similarly. With a first order approximation there is no odd-order terms in the *H(z)* denominator.

Taking into account gain and leakage errors the actual transfer function becomes:

$$H(z) = \frac{a \cdot z^{-1}}{1 + (1-c) \cdot z^{2}}$$

Where error term 'a' depends on both current gain of current copier and voltage gain of the voltage buffer, while the term c is a function of parasitic circuit elements which disturb the stored charges on the integrating capacitors.

2.2 Simulation results

A CCCII macromodel [8] is used for simulation of the proposed circuit. The resonator output for a 12.5 MHz input with a 50Mhz Clock is shown in fig. 2.

Conclusion: a Novel switched-capacitor resonator is proposed. For the first time it is used a CCII as basic building block. Due to inherent high-speed nature of CCII, it must have better capability to be used for higher frequency IF signals.

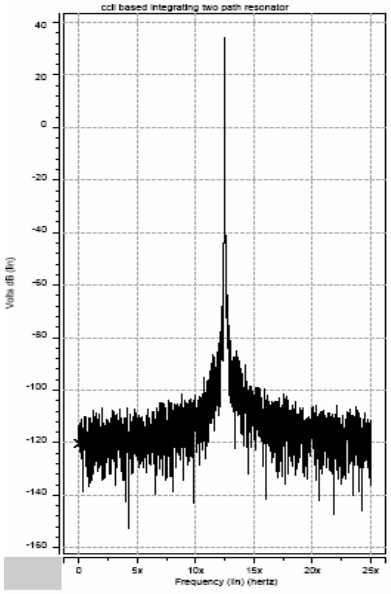

Fig. 2: Simulation Results

3 Conclusion

A Novel switched-capacitor resonator is proposed. For the first time it is used a CCII as basic building block. Due to inherent high-speed nature of CCII, it must have better capability to be used for higher frequency IF signals.

References:

[1]. F. W. Singor and W. M. Snelgrove, "A switched-capacitor bandpass ΔΣ A/D modulation at 10.7MHz", *IEEE J. of Solid State Circuits*, vol. 30, pp. 184–192, Mar. 1995.

[2]. S. Bazarjani and W. M. Snelgrove, "A 160-MHz fourth-order double- sampled SC bandpass ΔΣ modulator", *IEEE Trans. on CAS-II*, vol. 45, pp. 547–555, May 1998.[

[3]. S.-I. Liu, C.-H. Kuo, and R.-Y. Tsai, "A double-sampled pseudo-two-path bandpass ΔΣ modulator", *IEEE J. of Solid State Circuits*, vol. 35, pp.276–280, Feb. 2000.

[4]. M. Keskin, U. Moon, and G. C. Temes, "A novel switched-capacitor resonator structure with improved performance", *Electronic Letters*, vol. 37, no. 4, Feb. 2001.

[5]. A. Sedra, K. C. Smith, "A Second Generation Current Conveyor and its Applications" IEEE Trans. Circuits and Systems, CT-17, pp.132-134, 1970.

[6]. O. Oliaei, J. Porte, "Compound current conveyor ($CCII^{+}$ and $CCII^{-}$)" Electron. Lett., Vol. 33, Issue 4, pp.253-254, Feb 1997.

[7]. H. Kaabi, M. R. Jahed Motlagh, and A. Ayatollahi, "A Novel Current-Conveyor-based Switched-Capacitor Integrator', Proc. ISCAS, Vol. , pp. ,2005.

[8]. B. Wilson, 'Performance Analysis of Current Conveyors", Electronics Letters, Vol. 25, No. 9, pp. 1597-1598, Nov. 1989.