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Differential Quartet, A Novel Circuit Building Block for High Slew Rate Differential Amplification

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Abstract: - A new Differential Circuit is presented. It has the best properties of both conventional diff. pairs and Class AB cross coupled diff. pairs. The proposed circuit has high g_m of Diff. pair while High current capacity of class AB cross coupled diff. pairs. The large signal and small signal analysis are done and are compared to other circuits. The circuit is used to design a new OTA for SC. Circuits. The simulation results are also included

Key-Words: - **Diff. Pair, Diff. Circuit, Class AB Stage, Diff. Quad, OpAmp, OTA, CCII**

1 Introduction

The rapid increase in chip complexity has forced the need to implement complete analog-digital subsystems on a single substrate, using the same technology. The push toward integrating entire systems for operation with a single supply induces various problems for the analog portions. The lack of a solid analog ground and the reduced voltage range without a corresponding reduction in the threshold voltages eliminates the use of many proven circuit configurations.

For these reasons, implementation of analog functions in digital CMOS technology has become increasingly important, and great strides have been made in recent years in implementing functions such as high-speed ADC's, DAC's, SC. Filters and modulators, voltage references, instrumentation amplifiers, and so forth in CMOS and BiCMOS technologies. Another key technical development has been a maturing of the state of the art in the implementation of Discrete-Time Sigma-Delta modulators in CMOS technologies. These developments have been well documented in the literature. These modulators are key elements of most analog subsystems, particularly in high performance ADC systems that their performance is strongly affected by modulator's quality.

The key element of Sigma-Delta Modulators are their high performance OTA's. Thus the design of high performance Operational Transconductance Amplifiers has a great importance. Frequency response, power dissipation and Slew-rate limitation are high priority problems in the design of high performance OTA's.

An important factor that places a lower limit on the achievable power dissipation in switched capacitor integrators is that a certain amount of charge must be drawn from a power supply in order to charge and discharge the integrating and load capacitors on which the signal is stored. The OTA must be designed so that when the largest amplitude signal is present, enough current can be supplied to charge the capacitors to be required new value in one clock cycle. In class A amplifiers the maximum available output current is limited to the quiescent bias current, placing a low limit on the required bias current. Although conventional diff. pair is well suited to be used but its class A biasing results in a compromise between slew-rate limitation and power dissipation specially in SC. Circuits. Large power savings can be affected if only that current is drawn that is needed to charge the capacitance on that particular cycle. The use of class AB differential amplifier configurations which can deliver peak charging currents to the load that are much larger than quiescent current flowing in the circuit can result in large reductions in power dissipation in these types of applications.

Class AB circuitry is widely used in both bipolar and CMOS circuit design to minimize power dissipation. The term class AB is taken to mean a circuit that can deliver to and pull from a load a current that is larger than the dc quiescent current flowing in the circuit. If an important objective is the minimization of total power dissipation then the use of class AB operation can be extended to the internal stages of the amplifiers.

The intent of this paper is to introduce a new differential scheme that has superior performance in compare to conventional diff. pairs [1-2] and cross

coupled diff. amplifier [3].

This paper is organized as follows. In section II a historical review is presented. In section III the new circuit is proposed and described in detail. Section IV compares large signal and small signal properties of the proposed circuit with conventional designs. Section V discussed the structure of a typical OTA incorporated the new Diff. Quartet as input stage.

2 Historical review

2.1Differential pair

Differential pairs are perhaps the most widely used subcircuit in analog integrated circuits. The usefulness of this circuit stems from the fact that cascades of these pairs can be directly coupled to one another without interstage coupling capacitors and that the differential input characteristics provided by the circuit are required in many types of analog circuits[4] . As a class A amplifier, the maximum available output current is limited to the quiescent bias current, placing a low limit on the required bias current.

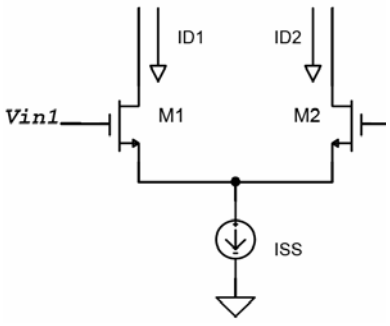

Fig. 1: Conventional Diff. Pair

Assuming that the devices are identical and neglecting output resistance and body effect we can express the differential current of the two devises as [5]:

$$\Delta I_D = I_{D1} - I_{D2} = \frac{1}{2}\cdot\beta_n\cdot\left[\left(V_{gs1}-V_{thn}\right)^2-\left(V_{gs2}-V_{thn}\right)^2\right] = \frac{1}{2}\cdot\beta_n\cdot\left(V_{in1}-V_{in2}\right)\cdot\sqrt{\frac{4I_{SS}}{\beta_n}-\left(V_{in1}-V_{in2}\right)^2} \quad (1)$$

Where $\beta_n = \mu_n\cdot C_{ox}\cdot\left(\frac{W}{L}\right)$.

The expression is valid when both transistors are in saturation that is true if:

$$\left|V_{in1}-V_{in2}\right| \le \sqrt{\frac{2I_{SS}}{\beta_n}} \quad (2)$$

This condition shows a limiting behavior when the differential input voltage exceeds a certain value.

For analog applications we are particularly interested in the Transconductance of the diff. pair i.e., the equivalent G_m of M1 and M2, defined as:

$$G_m = \frac{\partial\Delta I_D}{\partial\left(V_{in1}-V_{in2}\right)} \quad (3)$$

Taking the derivative of (3), results in:

$$G_m = \frac{1}{2}\cdot\beta_n\cdot\frac{\frac{4I_{SS}}{\beta_n}-2\left(V_{in1}-V_{in2}\right)^2}{\sqrt{\frac{4I_{SS}}{\beta_n}-\left(V_{in1}-V_{in2}\right)^2}} \quad (4)$$

Particularly in equilibrium condition $V_{in1}-V_{in2}=0$, the expression will be simplified and reduces to differential small-signal Transconductance of the circuit:

$$G_m\big|_{equilibrium} = \sqrt{\beta_n\cdot I_{SS}} = g_{m1} = g_{m2} \quad (5)$$

Thus the Transconductance of the diff. pair is the same as the Transconductance of each individual device. As seen this Transconductance depends on bias current and device size (W/L).

Fig.2 intuitively shows the graphical representation of Transistor currents and equivalent Transconductance for a typical diff. pair.

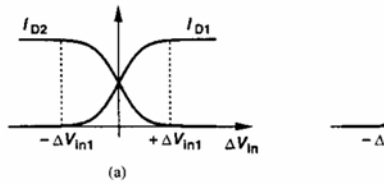

Fig2:

In small-signal analysis, we can use small signal model, to extract input- output relationship around quiescent point.

2.2 Differential Cross-Coupled Circuit

In circuits where the useful bandwidth is limited by the maximum slew-rate, and in applications were

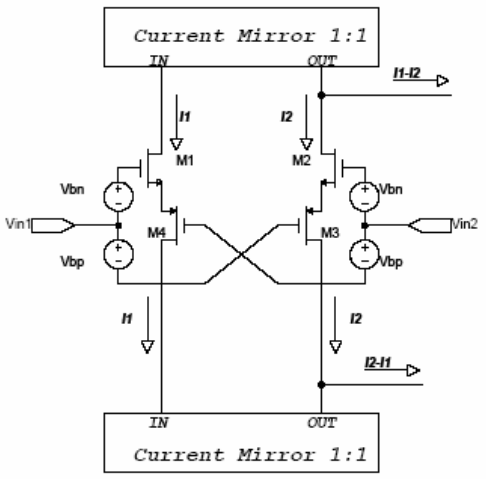

Fig. 4: A Cross-Coupled Diff. Circuit with Sample

the output current requirements vary widely (i.e. SC. Circuits), a class AB circuit may provide substantially improved performance. An example of a class AB diff. circuit for input stages is shown in fig. 4.

While this circuit allows full class AB operation with differential inputs, it will in some applications present difficulties due to fairly small common-mode input range.

To provide a large signal analysis, half the circuit is deleted and the schematics is simplified as in Fig. 5

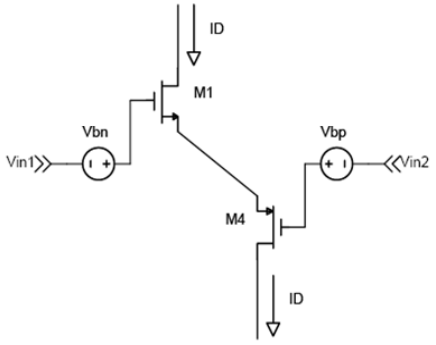

Fig. 5: Half circuit

Assuming:

$$1/\sqrt{\beta_{eq}} = 1/\sqrt{\beta_n} + 1/\sqrt{\beta_p} \quad (5)$$

$$V_{bn} = V_{thn} + \sqrt{I_{SS0}/\beta_n} \quad (6)$$

$$V_{bp} = |V_{thp}| + \sqrt{I_{SS0}/\beta_p} \quad (7)$$

While $I_{SS0}/2$ is the circuit's quiescent current. Assuming both transistors are in saturation region. An equation for the current with respect to input voltages V_{in1} and V_{in2} is drawn as follows:

$$I_{D1} = (\beta_{eq}/4)\left(\Delta V_{in} + 2\sqrt{I_{SS0}/\beta_{eq}}\right)^2$$

Where $\Delta V_{in} \geq -2\sqrt{I_{SS0}/\beta_{eq}}$, is the validity condition. Also for the other branch it is shown that the equation is

$$I_{D2} = (\beta_{eq}/4)\left(\Delta V_{in} - 2\sqrt{I_{SS0}/\beta_{eq}}\right)^2$$

Also the differential current is drawn as:

$$\Delta I = I_{D1} - I_{D2} =$$

$$(\beta_{eq}/4)\left[\left(\Delta V_{in} + 2\sqrt{I_{SS0}/\beta_{eq}}\right)^2 - \left(\Delta V_{in} - 2\sqrt{I_{SS0}/\beta_{eq}}\right)^2\right] \quad (8)$$

It is very important to mention that the above equation is a piecewise equation where in a specific region (that current flow is linear and in other sections where just one branch is on, presents a quadratic function. Thus it is instructive to represent the function as:

$$\Delta I = \begin{cases} \left(2\sqrt{I_{SS0}\beta_{eq}}\right)\cdot\Delta V_{in}, -2\sqrt{I_{SS0}/\beta_{eq}} \leq \Delta V_{in} \leq 2\sqrt{I_{SS0}/\beta_{eq}} \\ (\beta_{eq}/4)\left(\Delta V_{in} + 2\sqrt{I_{SS0}/\beta_{eq}}\right)^2, -2\sqrt{I_{SS0}/\beta_{eq}} \leq \Delta V_{in} \\ -(\beta_{eq}/4)\left(\Delta V_{in} - 2\sqrt{I_{SS0}/\beta_{eq}}\right)^2, -2\sqrt{I_{SS0}/\beta_{eq}} \leq \Delta V_{in} \end{cases} \quad (9)$$

According to above equation, the Transconductance function of this stage is a piecewise linear function that is calculated as:

$$G_m = \partial\Delta I/\partial\Delta V_{in} = \begin{cases} 2\sqrt{I_{SS0}\beta_{eq}} \\ (\beta_{eq}/2)\left(\Delta V_{in} + 2\sqrt{I_{SS0}/\beta_{eq}}\right) \\ -(\beta_{eq}/2)\left(\Delta V_{in} + 2\sqrt{I_{SS0}/\beta_{eq}}\right) \end{cases} \quad (10)$$

Here it is better to have more information about β_{eq} in eq. (5).

That equation can be rewritten as:

$$\beta_{eq} = \beta_n.\beta_p/\left(\beta_n + \beta_p + 2\sqrt{\beta_n.\beta_p}\right) \leq \beta_n.\beta_p/(\beta_n + \beta_p) \quad (11)$$

The above equation shows that for a constant $(\beta_n + \beta_p)$ that is a reasonable assumption for physical circuits, the maximum value of β_{eq} is less than $(\beta_n + \beta_p)/4$. Thus it can be shown that equivalent G_m in cross coupled circuits around equilibrium condition is less than G_m in conventional diff. pair that is a drawback of high slew rate amplifiers utilizing cross coupled circuit as input gain stage.

3 Differential Quartet

From an intuitive point of view, the new circuit is in real a combination of the previous circuits as shown in fig. 6.

It can be proved that at a region around the equilibrium where:

$$(|V_{in1} - V_{in2}| \approx 0) \quad (12)$$

Both upper and lower half circuits work almost as a current source providing a conventional current source for the other half. On the other hand when there is a large differential voltage at the inputs, a pair of the crossed transistors will become off and the other cross pair will behave in a similar manner as the differential cross coupled circuit.

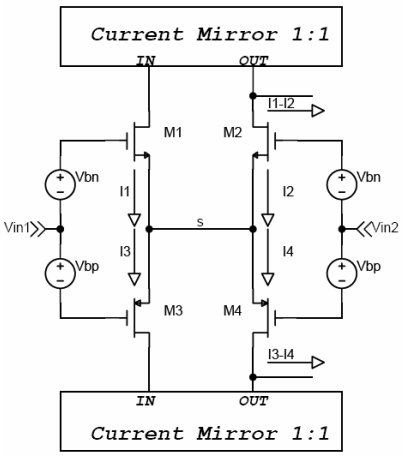

Fig. 6: Differential Quartet

With the same assumptions as equations (6-7) and:

$$I_{D1} + I_{D2} = I_{D3} + I_{D4} \qquad (13)$$

It can be shown that:

$$I_{D1} - I_{D2} = \frac{\beta_n}{2} \cdot (V_{in1} - V_{in2}) \cdot \left[\left(\sqrt{\left(\frac{2\sqrt{I_{SS0}}}{\sqrt{\beta_n} - \sqrt{\beta_p}} \right)^2 - (V_{in1} - V_{in2})^2} - \frac{2\sqrt{I_{SS0}}}{\sqrt{\beta_n} - \sqrt{\beta_p}} \right) + 2(V_{bn} - V_{thn}) \right] \qquad (14)$$

The above equation will be simplified if eq. (12) is valid hence:

$$I_{D1} - I_{D2} = \frac{\beta_n}{2} \cdot (V_{in1} - V_{in2}) \cdot \left[2(V_{bn} - V_{thn}) \right] \qquad (15)$$

$$= (V_{in1} - V_{in2}) \cdot \sqrt{\beta_n \cdot I_{SS0}}$$

The above equation shows that the G_m near equilibrium is the same for traditional diff. pair and the proposed circuit. On the other hand it is helpful to study about mention cross point voltage *Vs*.

It can be shown that:

$$V_s = \frac{V_{in1} + V_{in2}}{2} + \frac{\sqrt{I_{SS0}}}{\sqrt{\beta_n} - \sqrt{\beta_p}} - \frac{1}{2} \sqrt{\left(\frac{2\sqrt{I_{SS0}}}{\sqrt{\beta_n} - \sqrt{\beta_p}} \right)^2 - (V_{in1} - V_{in2})^2} \qquad (16)$$

This will be simplified to well known equation:

$$V_s \approx (V_{in1} + V_{in2})/2 = V_{cm} \qquad (17)$$

If there is equilibrium condition $|V_{in1} - V_{in2}| \approx 0$ or $\beta_n \approx \beta_p$.

Thus cross point voltage Vs behaves as same as virtual ground point in conventional diff pair around equilibrium. This shows that the new circuit has a similar frequency response to conventional diff. pair. Also it must be mentioned that a similar equation is valid for the lower half circuit.

It must be mentioned that in the new circuit there is a transition region where a pair of crossed transistor are going to off state while the other cross pair will have current near I_{SS0}. The transition region is not suitable for hand calculations thus instead it seams to be better using computer simulation for this part.

Thee simulations show in this region the G_m a value around G_m in the cross coupled pair (see fig. 9).

On the other hand when the differential voltage large enough, one of the cross pairs will go off and the equations describing the circuit will be same as cross coupled differential circuit.

Anyway in real circuit implementations the bias voltage sources must be replaced with voltage level shifters. A real implementation [6] is shown in fig. 7.

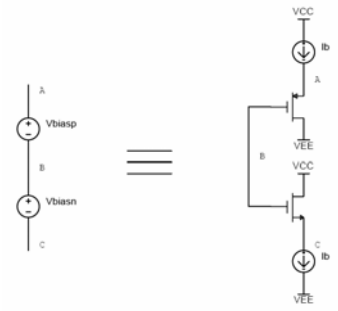

Fig. 7: A typical biasing circuit

3.1 Simulation Results

A DC SWEEP simulation is provided for the new circuit using a typical 0.6μm 5V CMOS technology to show the G_m for the above mentioned circuits. The proposed circuit with real biasing is shown in fig. 8.

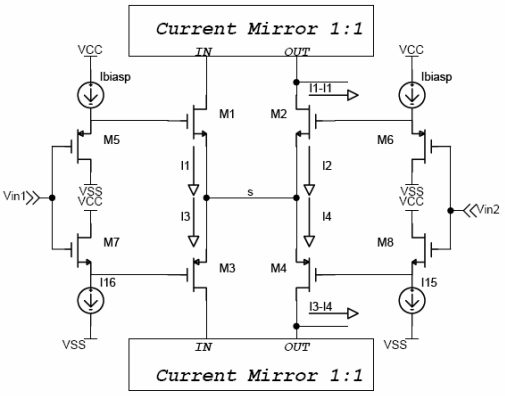

Fig. 8: Simulated circuit schematic

For all the transistors $W/L = 10/1$ and for all the circuits it is assumed $I_{SS0} = 50\mu A$.

The results in fig. 9 show the superior performance of the proposed circuit in compare to the traditional differential circuits.

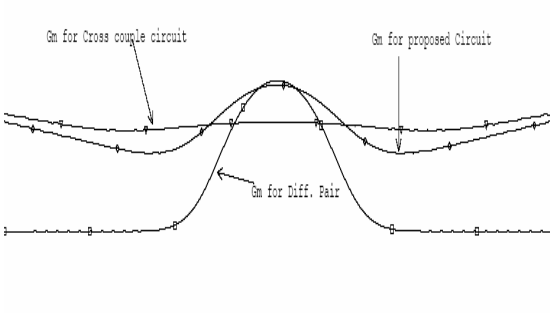

Fig. 9: Comparision of simulated G_m for the circuits

4 Conclusion

A new class AB differential circuit is proposed. The hand calculations and simulation results shows the new has the higher G_m of class A traditional diff. pair around equilibrium while having high current drive capability of the cross coupled circuit.

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