New Switched-Capacitor Pipelined ADC

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Abstract: - The paper deals with a new 12-bit low power switched-capacitor (SC) ADC for portable applications, such PDA, notebook etc. The paper describes design of ADC and its behavioural modelling regarding low power consumption. The Op-Amp sharing technique and capacitor scaling approach are utilized to obtain it. The basic block topology design is outlined too. The cancellation techniques to avoid the error sources rising of using SC technique for i.e. capacitor mismatch, clock feedthrough, finite gain and offset of Op-Amp etc. are utilized in the design.

Key-Words: - Pipelined ADC, switched-capacitor technique, portable application

1 Introduction

The switched-capacitor CMOS technology is a popular architecture for high-speed data conversion in communication systems, imaging, ultrasound front-ends, and many other applications. Fuelled by aggressive device scaling in modern integrated circuit technology, practically attainable operating speeds of this converter have increased by almost two orders of magnitude in the last 15 years. In addition to the ever-growing demands in conversion bandwidth, low power dissipation, and compatibility with deep-submicron technology have emerged as important metrics in state-of-the-art designs.

For the most part, this trend is explained by the increasing demand for portability, as well as recent efforts in system-on-chip (SoC) integration. In SoC implementations, data converters are embedded on the same chip with powerful fine-line digital signal processing, resulting in a limited budget for their total heat and power dissipation.

Among the key building blocks in pipelined ADCs are the residue amplifiers that interface successive converter stages. Especially in the converter front-end, these gain elements have to meet very stringent speed, noise, and linearity requirements and tend to dominate overall power dissipation. To address this issue, a variety of techniques have been developed to minimize amplifier power in pipelined ADCs.

In this paper, a 12-bit ADC combines several design approaches to reach low power consumption and high performance with a pipelined architecture.

2 Pipelined ADC Architecture

Generally, a pipelined ADC architecture uses a number of similar pipelined stages [1], [3], [4]. Here, the analog input V_{IN} is first sampled and held steady by a S&H, while the ADC (usually flash ADC) in each stage quantizes it with resolution of B+1 raw bits. The B+1-bit output is then fed to a B+1-bit DAC, and the analog output is subtracted from the input. This residue is then multiplied by a factor of 2^B and fed to the next stage. This gained-up residue continues through the pipeline, providing B+1 bits per stage until it reaches the flash ADC, which resolves the last LSB bits. Since the bits from each stage are determined at different points in time, all the bits corresponding to the same sample are time-aligned with shift registers before being fed to the digital-error-correction logic.

Fig. 1 shows the most common implementation technique of the multiplying DAC (MDAC), which is well-known switched-capacitor approach. Note MDAC consists of the S&H, the DAC, the summation node and the gain amplifier. The DAC function is performed by charging/discharging a set of capacitors with a reference voltage source $\pm V_{ref}$. Depending on the resolved bits, one of the capacitors is moved as a feedback capacitor of the amplifier, while the others are connected to the $+V_{ref}$ or $-V_{ref}$ source to perform the subtraction and amplification for the residue signal, which is passed to the next stage for more fine conversion. Then, B+1 bits from all stages are combined to produce a full digital representation of the applied analog input.

The residue generated in each stage of the ADC is

$$V_{out}(i) = K\left[\left(1+\frac{C_S}{C_F}\right)V_{in}(i) - \frac{C_S}{C_F}D_i V_{ref} + \delta\right],$$

$$K = \frac{A}{1+\frac{C_S}{C_F}+A}, \qquad (1)$$

where parameter K is an Op-Amp finite gain error coefficient (ideally unity), D is ±1 or 0 depending on the input voltage level and A is the finite Op-Amp gain.

Differential charge injection has been included in the above Eq. (1) as an additive error term δ. Ideally, the expected residue voltage is

$$V_{out}(i) = 2V_{in}(i) - DV_{ref} . \qquad (2)$$

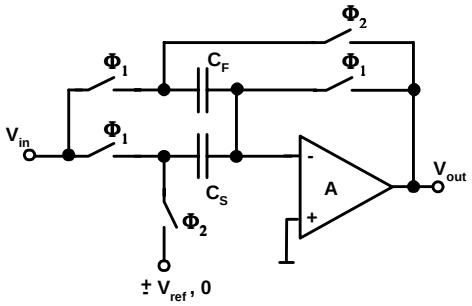

Fig. 1 Switched-capacitor MDAC

In an SC circuit with the single-pole Op-Amp such as a common-source MOS amplifier, the closed-loop bandwidth (BW) is given by

$$BW = \frac{G_m}{C_L . f}, \qquad (3)$$

where G_m is the transconductance of the Op-Amp, C_L is the output load capacitance, and f is the feedback factor. The feedback factor f of the i-th stage SC circuit shown in Fig. 1 is given by

$$f = \frac{C_i}{2^B . C_i + C_{opamp}}, \qquad (4)$$

where C_{opamp} is the input capacitance of the Op-Amp. The total output load capacitance of the i-th stage is given by

$$C_L = (1 - f) . C_i + 2^B . C_{i+1} + C_{comp}, \qquad (5)$$

where C_{comp} is the total input capacitance of the comparator.

Based on these equations, the 1.5-bits/stage architecture has two benefits. The first is to maximize the bandwidth of the SC circuit, which limits the overall conversion rate. With a resolution of 1.5 bits/stage, the closed-loop gain of 2 allows for a low load capacitance and a large feedback factor, and as a result, a large interstage amplifier bandwidth can be achieved compared with architectures employing larger per-stage resolution. The second is that a resolution of 1.5 bits/stage allows for a large correction range for comparator offsets in the flash ADC, where only two comparators are required for 1.5 bits/stage. Thus, comparator offsets up to $\pm V_{ref}/4$ can be tolerated without degradation of the overall linearity or SNR.

Beyond the mentioned constraints (large BW of Op-Amps, relatively high speed, high accuracy and low power consumption), there are several non-ideal effects, which have to be compensated. There are mainly finite gain of Op-Amps, charge injection, clock feedthrough and capacitor mismatch. The improved pipelined ADC uses design approaches, which resolves these requirements.

3 A New Pipelined ADC

A low power usage is critical in portable application. The suitable resolution for each stage has been proposed and the error correction techniques have been chosen and used in design to satisfy mentioned requirements. These problems has been solved simultaneously because of the used approaches and developed background calibration technique.

3.1 Error Sources Correction and Used Design Approaches

As was mentioned before many error sources rise by utilization of SC technique in ADC. Fig. 2 shows some of them.

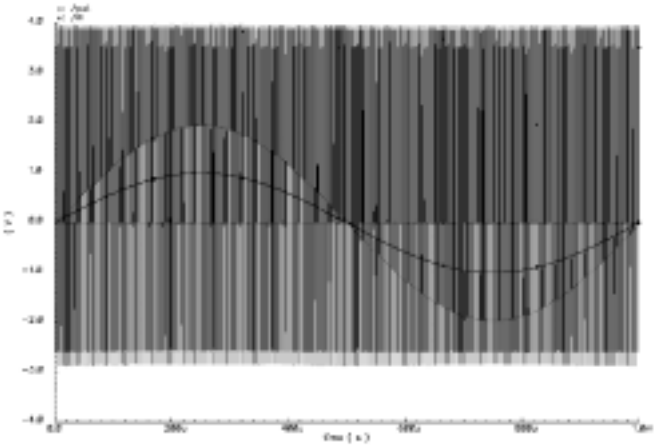

Fig. 2 Illustration of finite gain and clock feedthrough problem

Ideally the input analog signal with frequency of 1 kHz and 1 V magnitude has to be doubled on the output. It is seen that in reality it is not true. Since the Op-Amps with finite gain were used the output signal has only 1.986 V and there is also seen the clock feedthrough effect.

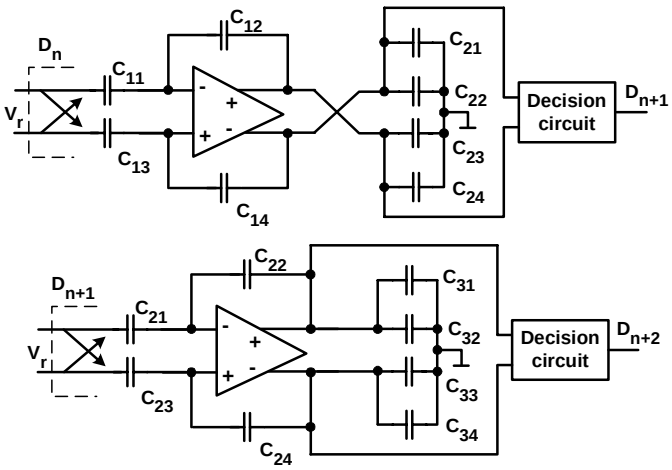

Fig. 3 Improved Op-Amp sharing approach

These problems has been solved in paralel with lowering of power consumption. The improved fully differential Op-Amp sharing technique [1] has been used in the design, Fig. 3.

This technique has one drawback. Since the Op-Amp is still in active state, there is no time to reset the nonzero voltage due the finite gain and Op-Amp voltage offset. This problem was solved by background digital correction.

The power consumption is roughly lowered by 30 %.

The next Fig. 4 shows output when the described approaches has been used.

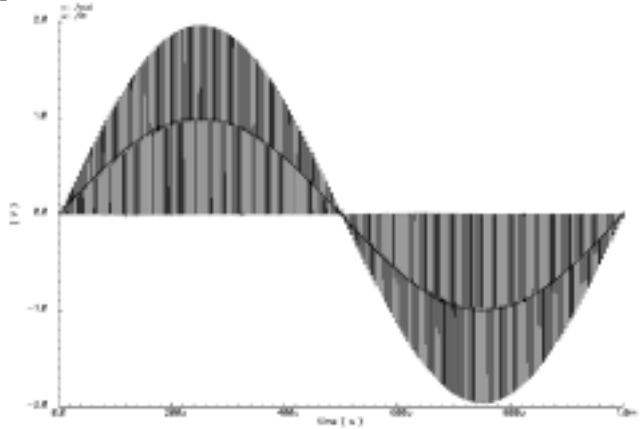

Fig. 4 Output obtained using improved Op-Amp sharing approach

The power consumption will be also significantly reduced with capacitor scaling approach [2] and has been utilized in this design.

A special lower-power Op-Amps has been designed for the application. The schema of the Op-Amp is on Fig. 5.

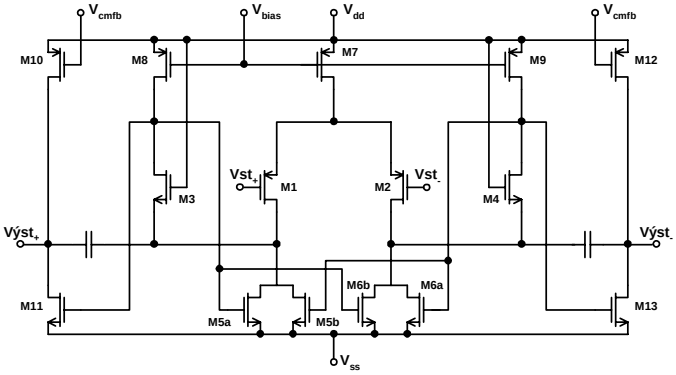

Fig. 5 The proposed Op-Amp

As was explained above the 1.5-bits/stage resolution is optimal to gain large Op-Amp BW without degradation of the overall linearity or signal-to-noise ratio (SNR).

A new background digital correction has been developed, which in conjunction with described circuit techniques satisfy high accuracy of the conversion. The error correction circuitry also solves the capacitor mismatch problem. The correction algorithm utilizes LMS approach with radix calculation. It reduces the non-ideal effects caused by error sources effectively.

4 Conclusion

A new 12-bit, low power (3,3 V) and 10 MS/s pipelined SC ADC is presented. The ADC utilizes several advanced techniques to obtain low power consumption (shared Op-Amps and capacitor scaling) large bandwidth of Op-Amps and it also reduces errors caused by non-ideal effects (capacitor mismatch, finite Op-Amp gain, charge injection). The modeling of the ADC includes study and simulation of the used techniques and calculations. Then it focuses on improving of used techniques. It also includes canceling of unwanted effects caused by error sources. At least it holds modeling and simulation of the proposed basic blocks and the verification of the utility.

The next step based on simulation results of behavioural modeling is design of the proposed stages using CMOS technology, its simulation, verification and testing of the real produced samples.

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