Analog-Digital versus DSP Implementation of Park's Current Calculators for AC Mains Self-Powered Systems

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Abstract: - This paper presents a comparison between an analog-digital dedicated circuit that evaluates the *Park's* current components on three-phase systems and its counterpart implementation with a DSP. Both circuits operate with the instantaneous active and reactive current component i_d-i_q method. These currents are obtained with a synchronous reference frame which derives from the mains voltage vector. The calculators presented are suitable to perform the direct and inverse current transformations in many self-powered systems connected to the ac mains even at nonideal mains voltage conditions. Laboratorial implementation aspects of the proposed current calculators are shown. Experimental results showing their steady-state performance operation applied to a shunt active filter application are also presented.

Key-Words: Park's transformation, analog-digital systems, digital signal processing, current measurement, current calculator, active filter, harmonics.

1 Introduction

The use of *Park's* transformations is very useful for the study of electrical machines and power electronic converters. The *Park's* current calculators presented in this paper are based on the instantaneous active and reactive current component i_d-i_q method [1]. This method is specially suited to the control of many self-powered systems connected to the ac mains, like active filters (AF's), unified power flow controllers (UPFC's), advanced static VAr compensators (ASVC's), PWM rectifiers, uninterruptible power supplies (UPS's) and neutral current compensators (NCC's). In active filtering it as been proved that better performances are achieved under unbalanced and nonsinusoidal voltage conditions compared with other control methods [1]-[3]. The adopted control method is based on a synchronous rotating frame derived from the mains voltages without the use of a phase-locked loop (PLL) [4]-[6]. Using the i_d-i_q control method many synchronisation problems are avoided and truly frequency-independent systems can be achieved.

2 Control Method

In the instantaneous active and reactive current component i_d-i_q method [1]-[3] the conversion between the nonlinear load currents i_{li} and their corresponding *dq* components, i_{ld} and i_{lq}, are obtained from a direct (1), (3) and inverse (1), (2) *Park's* transformations. A null value for the zero voltage sequence is considered. The zero current sequence is also null since there is absence of neutral connection.

The load current components are derived from a synchronous reference frame where θ represents the instantaneous voltage vector angle.

$$\mathbf{T}_{dq}(\theta) = \frac{2}{\sqrt{3}} \cdot \begin{bmatrix} \cos(\theta) & -\sin(\theta) \\ \cos(\theta - \frac{2\pi}{3}) & -\sin(\theta - \frac{2\pi}{3}) \\ \cos(\theta - \frac{4\pi}{3}) & -\sin(\theta - \frac{4\pi}{3}) \end{bmatrix} \quad (1)$$

$$\begin{bmatrix} i_{ld} \\ i_{lq} \end{bmatrix} = \mathbf{T}_{dq}^{T}(\theta) \cdot \begin{bmatrix} i_{l1} \\ i_{l2} \\ i_{l3} \end{bmatrix} \quad (2)$$

$$\begin{bmatrix} i_{l1} \\ i_{l2} \\ i_{l3} \end{bmatrix} = \mathbf{T}_{dq}(\theta) \cdot \begin{bmatrix} i_{ld} \\ i_{lq} \end{bmatrix} \quad (3)$$

In Fig. 1 the instantaneous voltage and current vectors in the stationary and rotating frames are shown. The transformation angle is sensible to voltage

harmonics and unbalanced voltage sources therefore dθ/dt may not be constant.

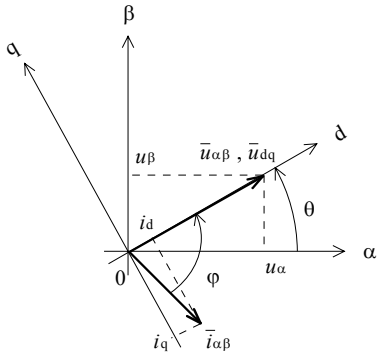

Fig. 1. Instantaneous voltage and current vectors.

Instead of using a PLL to obtain the θ angle, thus avoiding improper current determination, the real instantaneous voltage vector angle can be obtained by,

$$\theta = \tan^{-1}\frac{u_\beta}{u_\alpha}, \tag{4}$$

where u_α and u_β are $\alpha\beta$ components of the mains supply voltage, (5).

$$\begin{bmatrix} u_\alpha \\ u_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \cdot \begin{bmatrix} 1 & \frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} \end{bmatrix} \cdot \begin{bmatrix} u_{12} \\ u_{23} \end{bmatrix} \tag{5}$$

Since the zero current sequence is considered null, as stated before, the *Park's* transformations can be obtained by the following expressions.

$$\begin{bmatrix} i_{l_d} \\ i_{l_q} \end{bmatrix} = \sqrt{2} \cdot \begin{bmatrix} \sin(\theta+\frac{\pi}{3}) & \sin(\theta) \\ \cos(\theta+\frac{\pi}{3}) & \cos(\theta) \end{bmatrix} \cdot \begin{bmatrix} i_{l_1} \\ i_{l_2} \end{bmatrix} \tag{6}$$

$$\begin{bmatrix} i_{l_1} \\ i_{l_2} \end{bmatrix} = \sqrt{\frac{2}{3}} \cdot \begin{bmatrix} \cos(\theta) & -\sin(\theta) \\ -\cos(\theta+\frac{\pi}{3}) & \sin(\theta+\frac{\pi}{3}) \end{bmatrix} \cdot \begin{bmatrix} i_{l_d} \\ i_{l_q} \end{bmatrix} \tag{7}$$

3 Analog-Digital Implementation

The calculator circuit proposed can perform the direct and the inverse *Park's* transformations [7]. The block diagrams are presented in Figs. 2 and 3.

To perform the inverse *Park's* current calculation the phase-to-phase voltages u_{12} and u_{23} have to be measured. After the measurement operation the voltage signals pass through an anti-aliasing filter and a voltage limiter before the digital conversion. Using two 8-bit semi-flash analogue-to-digital converters (ADC's) a high conversion rate can be achieved (sampling time or frequency of $t_s < 5$ μs, $f_s > 200$ kHz). An address bus is established from the 7 most significant bits (MSB) of each ADC. The loss of 1 bit in the conversion is irrelevant since it represents the ADC error. The bus will address two 32 kb erasable programmable read-only memories (EPROM's) where the sinusoidal functions presented in (6) are stored, with the θ angle determined by (4). The outputs of the EPROM's are converted by two dual 8-bit 4-quadrant multiplying digital-to-analogue converters (DAC's).

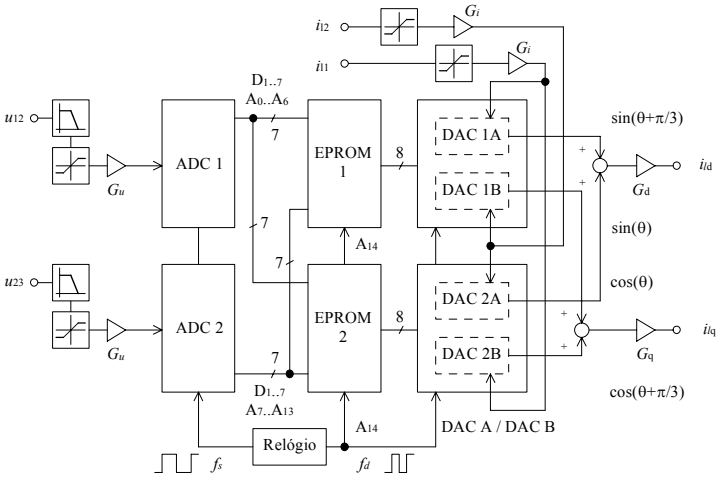

Fig. 2. Inverse *Park's* transformation.

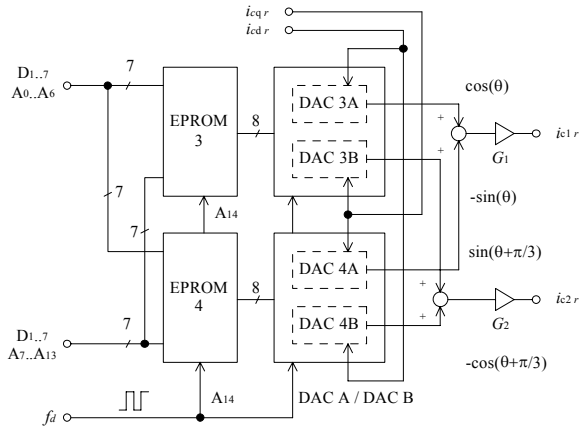

Fig. 3. Direct *Park's* transformation.

The measured current values i_{l1} and i_{l2} are limited and multiplied by the DAC's. The sum of these signals gives the currents i_{ld} and i_{lq}. The operation of the direct *Park's* current calculation is similar to the last circuit. However the sinusoidal functions stored in the EPROM's are based in (7) and (4), so the result will be the reference currents i_{c1r} and i_{c2r}. The synchronisation circuit signals are obtained with a master clock built with a voltage-controlled oscillator (VCO) and a D type flip-flop (FF). These signals enable us to choose the sinusoidal functions in the EPROM's since they are

multiplexed, and the proper selection of the 'read' (RD) and 'write' (WR) operations in both ADC's and DAC's.

In Fig. 4 is presented the laboratorial implementation of *Park's* current calculator based in the circuits shown in Figs. 2 and 3.

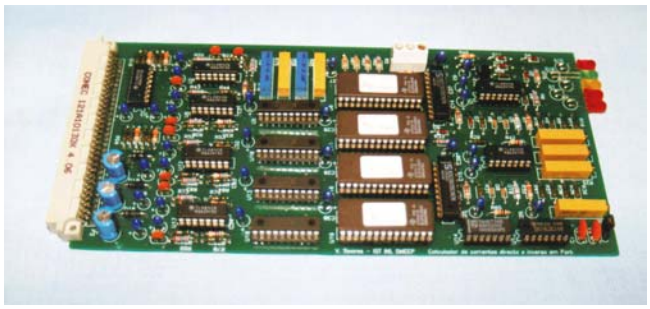

Fig. 4. Analog-digital implementation of the *Park's* current calculator.

4 DSP Implementation

The digital implementation of the *Park's* Current calculator is based on a DSP system (ADwin-Gold), Fig. 5.

Fig. 5. DSP implementation of the *Park's* current calculator.

This stand-alone and compact model is well suited for prototyping and it is equipped with the IEEE 32 bit floating point 40 MHz *Super Harvard* Architecture (SHARC) DSP ADSP 21062 from Analog Devices, Fig. 6. It presents a single-cycle instruction execution with 25 ns instruction rate. The performance values are 40 millions of instructions per second (MIPS), 120 millions of floating point operations per second (MFLOPS) of peak performance and 80 MFLOPS of sustained performance.

The DSP as an internal static random access memory (SRAM) of 256 kB (25 ns). The external dynamic random access memory (DRAM) is 4 MB (125 ns). Both memories can be used for program and data.

In the experimental prototype it is required the fastest possible program execution so the SRAM is the mainly used memory.

This processing system it is programmable by a dedicated interface and runs in real-time independent of the computer and its workload.

There is a selectable group of 2 ADC's with 16 bipolar multiplexed analog inputs (12 bit resolution with 0.8 µs conversion time plus 1 µs multiplexer settling time, or 16 bit resolution and 10 µs conversion time plus 4 µs multiplexer settling time).

Analog outputs are obtained with two non multiplexed 16 bit DAC's (3 to 10 µs of settling time depending on signal range).

For digital data there are 16 bit TTL digital inputs/outputs.

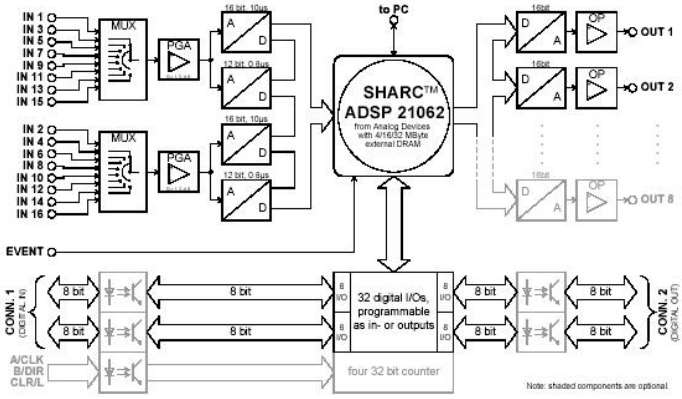

Fig. 6. DSP internal structure of the *Park's* current calculator.

5 Experimental Results of the *Park's* Current Calculators

Applying the proposed *Park's* calculators to a shunt AF for harmonic current compensation, the inverse and direct current calculations can be easily performed, Fig. 7. The AF control circuits are described in [1] and [2].

The variables i_{ld} and i_{lq} are the nonlinear load currents in *dq* components that have to be filtered in order to eliminate the DC components, i.e., to obtain the harmonics to be injected in the main supply, i_{cdr} and i_{cqr}. Therefore the variables i_{c1r} and i_{c2r} represent the reference currents of the three-leg voltage source converter (VSC) and so the harmonic currents that must be eliminated from the mains.

An AF experimental prototype was built with a 2 kVA three-leg IGBT VSC. Hall-effect current and voltage sensors and simple digital and analog interface circuits were used.

The ac current control and dc voltage regulation were performed by analog-digital controllers/regulators or by the DSP system.

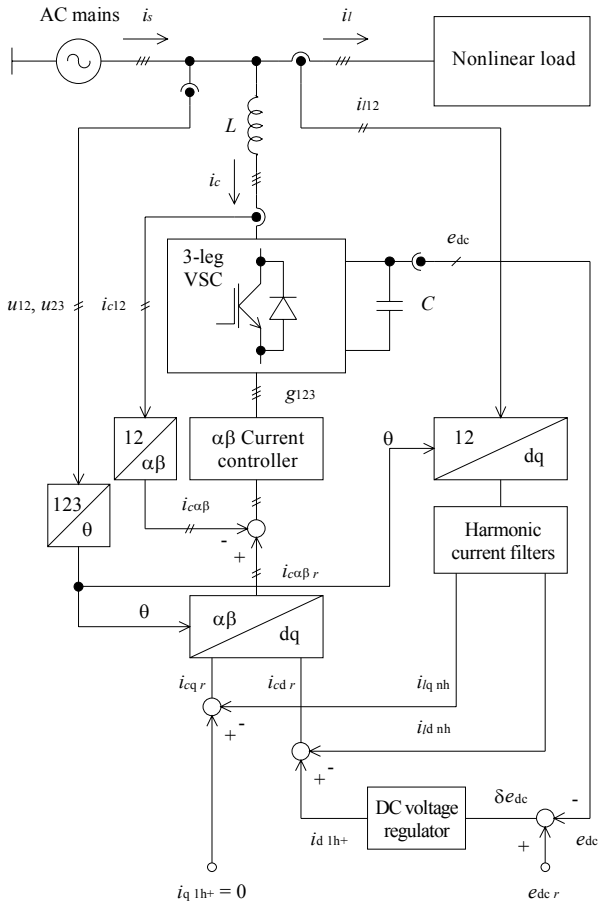

Fig. 7. Shunt AF control circuits.

The variables measured in the prototype were: currents i_{c123}, voltages u_{12}, u_{23} and e_{dc}. Switching signals and IGBT enabling signals g_{123} and E_{123}, respectively, were used to control the three-leg VSC. The global DSP execution time which corresponds to the sampling time of all variables measured was 35 μs (sampling frequency of 28.6 kHz).

The following results show the operation of the *Park's* current calculators applied to an AF under mains balanced and sinusoidal voltage conditions, $f = 50$ Hz. The harmonic current compensation is performed over a nonlinear load made with a three-phase full converter (firing angles $\alpha = 0°$ and $\alpha = 60°$).

With the analog-digital *Park's* current calculator a great decrease in the total harmonic distortion (THD) is obtained, Figs. 8 and 9.

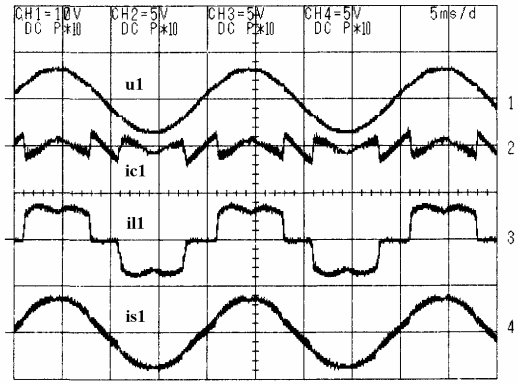

Fig. 8. AF performance with the analog-digital *Park's* current calculator. (1) Mains voltage u_1 (100 V/div). (2) Compensating current i_{c1} (15 A/div). (3) Converter current i_{l1} (15 A/div), $\alpha = 0°$, $THD_{il1} = 28{,}0$ %. (4) Mains current i_{s1} (15 A/div), $THD_{is1} = 4{,}0$ %. 5 ms/div.

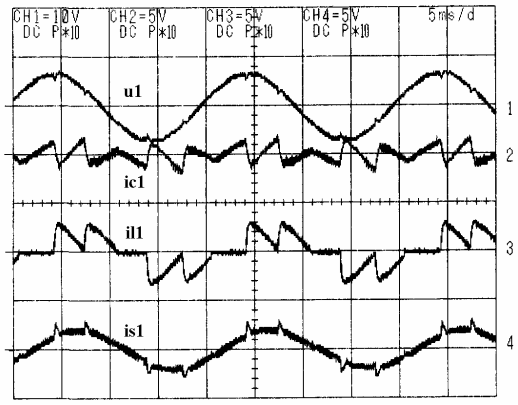

Fig. 9. AF performance with the analog-digital *Park's* current calculator. (1) Mains voltage u_1 (100 V/div). (2) Compensating current i_{c1} (15 A/div). (3) Converter current i_{l1} (15 A/div), $\alpha = 60°$, $THD_{il1} = 56{,}0$ %. (4) Mains current i_{s1} (15 A/div), $THD_{is1} = 13{,}0$ %. 5 ms/div.

Similar performance values are obtained with the DSP *Park's* current calculator, Figs. 10 and 11. From the THD values obtained in all experimental results it can be concluded that the greater resolution provided by the DSP system partially compensates its lower sampling frequency (12 bit, 28.6 kHz) compared to the analog-digital system (8 bit, 200 kHz).

It also should be pointed out that the DSP executing time (acquisition plus processing time) is a critical parameter with respect to current control in the AF.

The effectiveness of the harmonic current compensation is very dependable from it.

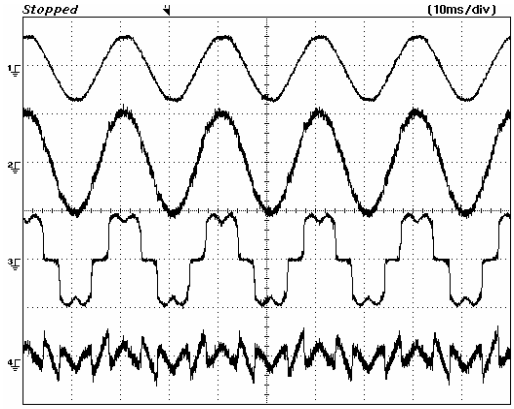

Fig. 10. AF performance with the DSP *Park's* current calculator. (1) Mains voltage u_1 (100 V/div). (2) Mains current i_{s1} (10 A/div), THD_{is1} = 3,8 %. (3) Load current i_{l1} (10 A/div), α = 0°, THD_{il1} = 25,9 % . (4) Compensation current i_{c1} (10 A/div). 10 ms/div.

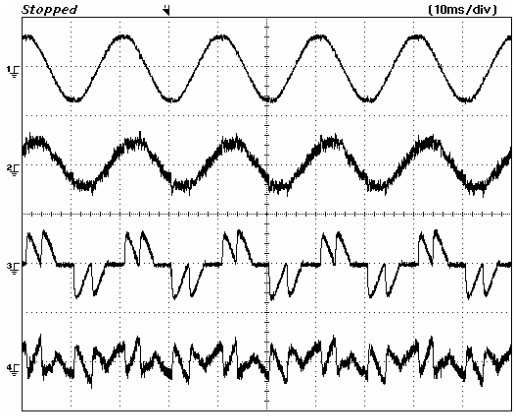

Fig. 11. AF performance with the DSP *Park's* current calculator. (1) Mains voltage u_1 (100 V/div). (2) Mains current i_{s1} (10 A/div), THD_{is1} = 8,7 %. (3) Load current i_{l1} (10 A/div), THD_{il1} = 60,8 % , α = 60°. (4) Compensation current i_{c1} (10 A/div). 10 ms/div.

6 Conclusions

The control method used in the *Park's* current transformations is based upon the instantaneous active and reactive current component i_d-i_q method. This method enables to obtain current calculators for AF that may operate in variable frequency conditions without any adjustments. Therefore, the harmonic compensation systems can work properly in a large range of frequencies covering both 50 Hz and 60 Hz distribution systems. The analog-digital *Park's* current calculator is built with inexpensive electronic circuits. The DSP version of this current calculator is much more expensive. However, since it's not an hardware dedicated circuit it presents the advantage of being programmable with great gains on signal processing capability and flexibility. Both systems proposed exhibits a very fast dynamics and present a good accuracy in the currents calculation. In an AF application the nonlinear load current harmonics are deeply decreased. There are no significant differences in the performance values between them.

For *Park's* current calculation there is not a unique solution between analog-digital and DSP implementations, in spite of being quite similar with respect to performance values. The choice between them as to do with cost effective issues and depends in what type of application the calculator is needed.

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