A pipelined ADC with Digital Correction for IEEE 802.11a WLAN

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Abstract: - In this paper, a 10-bit 50-MS/s Nyquist-rate CMOS pipelined analog-to-digital converter (ADC) with digital correction is presented for the WLAN application. The digital correction technique adapted by this pipelined ADC can give more accurate demands in application. The simulated SNDR is 60.5dB at the rate of 50-MS/s with a 5MHz input frequency. The DNL and INL of the presented pipelined ADC are suppressed within ± 0.45 LSB and ± 0.46 LSB, respectively. This presented circuit has been fabricated in a 0.35-μm 2P4M process. The dissipation power of the ADC is 93mW at 2.5V supply voltage, and the core area without PADs is 2.8×1.5 mm^2.

Key-Words: - Sample and hold, Nyquist-rate converter, ADC, pipelined, IEEE 802.11a, and WLAN.

1 Introduction

High-speed Nyquist-rate ADCs are widely used to wireless communication, storage, and display systems [1]-[2]. These ADCs specifications are decided cautiously due to different receiver architecture. For direct conversion receivers, two 20-MS/s ADCs are needed, while, for low-IF receivers only one 40-MS/s ADC might be sufficient [3]. And for wide signal bandwidth applications, the ADCs and DACs are demanded for operating at the high sampling rate. Hence the 50M sampling rate of the proposed pipelined ADC used for the IEEE 802.11a WLAN is adopted for providing demanding signal bandwidth. In addition the OFDM modulation used in the IEEE 802.11a standard also demands a high resolution for these analog-to-digital converters. For the typical receiver designs, at least 10 bits are needed to avoid an increased bit-error rate due to ADC's quantization [3].

This paper describes the design of the 1.5-bit stage pipelined ADC. The architecture of the pipelined ADC is introduced in Section 2. The implementation of the presented ADC is described in Section 3. Simulation results of this pipelined ADC are depicted in Section 4. At the end, the conclusion is given in Section 5.

2 ADC Architecture

The whole block diagram of the proposed pipelined ADC is shown in Fig. 1. An accurate sample and hold (S/H) circuit is added in the front of the ADC for the succeeding discrete-time signal processing [4]-[6]. In this paper, the 1.5-bit stage strategy is chosen to immune the offset caused by multi-bit comparator. Eight 1.5-bit stages and one 2-bit stage are adapted to perform a 10-bit pipelined ADC. A 1.5-b sub-ADC and a multiplying digital to analog converter (MDAC) are included in each 1.5-bit stage to perform the "slice" and "zoom-in" functions for the signal quantization and the consequential similar procedures, respectively. The final 2b flash ADC quantizes the residue signal from the last 1.5-bit stage to a 2-bit code which does not need to be corrected anymore and terminates the pipeline.

The generated digital codes from eight 1.5-bit stages and the 2-bit stage are synchronized by the registers since the time difference among these outcomes caused by the domino translation on each specific signal processed. The final 10-bit digital output is derived from the digital error correction circuit by overlapping 0.5-bit in each stage for the tolerance in the quantization errors.

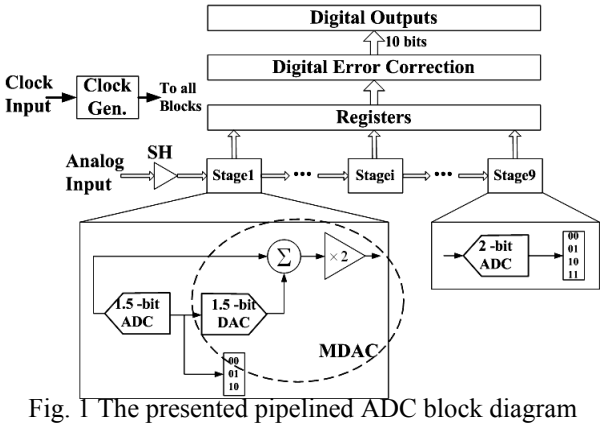


Fig. 1 The presented pipelined ADC block diagram

3 Circuit Implementation

3.1 Sample and Hold Circuit

In order to achieve 10-bit resolution for the ADC, the linearity in the front end S/H should be guaranteed higher than 10-bit. In other words, to the achieve 60dB SFDR in the S/H, a high gain opamp is demanded for the high-resolution request. In the other hand, to accommodate this circuit can be operated properly at a high sampling rate, a wide bandwidth opamp should be accomplished. Therefore, a gain-boosted folded-cascode amplifier is utilized to acquire both the high DC gain and high unit-gain frequency requirement. A PMOS input differential pair is chosen to compress noise coupled by the switching clocks compared to NMOS one. An 87dB DC gain and 540MHz unit- gain frequency are designed and simulated in the applied opamp [7].

The S/H circuit and its corresponding clocks are shown in Fig. 2. The phases ph1a and ph2a are turned off in advance of phases ph1 and ph2, respectively to reduce the signal-dependent charge injection. Furthermore, the dummy switches are added in those connected to the inputs of the opamp to avoid the charge injection from corrupting the performance. The sampling switches should be chosen to be as large as possible to reduce the turn-on resistance and increase the linearity [1].

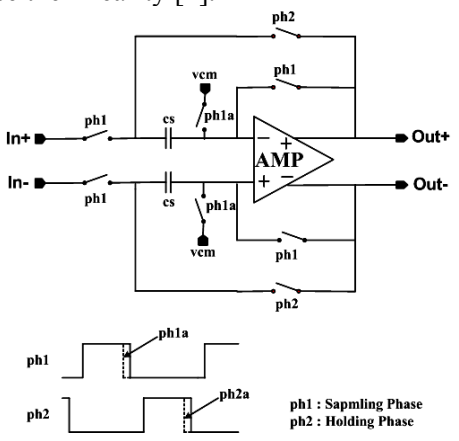


Fig. 2 Sample and Hold Circuit

3.2 1.5-Bit Stage

As illustrated in Fig. 3, a 1.5-bit stage is composed of a sub-ADC, an amplifier, and switched capacitors. The sub-ADC is implemented with a series of resistors and two comparators to accomplish a 1.5-bit quantization. Since the inherent process variation exists in the integrated circuits, the resistors employed in the i.5-bit stage are placed in common centroid to avoid degrading its fidelity. The amplifier and switched capacitors nearby perform like a simple DAC to converter the output of the sub-ADC to analog ones and given subtraction with the input and be amplified by two in turn.

There is a 1.5-bit stage that performs a arithmetic function as shown in equation (1). During the phase ph1d, the capacitors CS1, CS2, CF1, and CF2 are sampled in differential input V_{IN}, and a precise decision points are pursued in the sub-ADC to give digital output 00, 01, or 10. In order to converter the digital codes to corresponding analog signals from the differential input V_{IN} at precise decision levels, which are $+V_{ref}/4$ and $-V_{ref}/4$, the digital signal Dctrl from the 1.5b sub-ADC is applied to the reference selection block at the end of the sampling phases. That is, the bottom plates of CS1 and CS2 are connected to the Ref+ or vcm or Ref- depending on the Dctrl due to the differnt input.

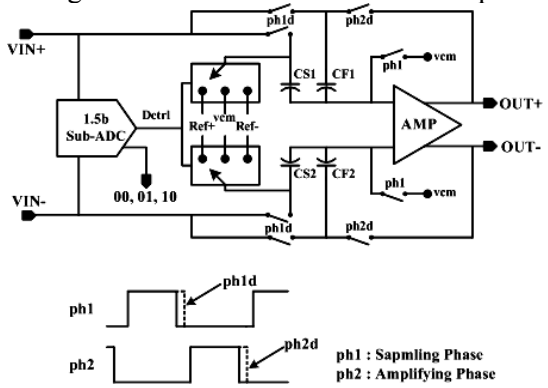


Fig. 3 1.5b Stage

$$V_{OUT} = \begin{cases} 2V_{IN} - V_{REF}, & V_{IN} < -V_{REF}/4 \\ 2V_{IN}, & |V_{IN}| \le V_{REF}/4 \\ 2V_{IN} + V_{REF}, & V_{IN} > +V_{REF}/4 \end{cases} \quad (1)$$

4 Simulation Results

The presented ADC has been fabricated in a standard 0.35μm COMS 2P4M technology. The total chip area without pads is 2.8×1.5 mm^2, and the whole chip layout is shown in Fig. 4.

The HSPICE simulation results of this ADC are preformed under 50-MHz of sampling rate at 2.5V supply voltage. From the simulation results, 60.5dB of SNDR can be obtained from the 1024-point FFT of output signal under 50 MSample/s and 5MHz input signal applied, as shown in Fig. 5. The 9.7 effective number of bits (ENOB) can be reached.

The differential nonlinearity (DNL) and the integral nonlinearity (INL) of this ADC are simulated using 5MHz full scale input signal. From 1,024 samples are collected under 50 MS/s, the simulated INL and DNL range are within ±0.45 LSB and ±0.46

LSB, respectively, as shown in Fig. 6(a) and (b).

5 Conclusion

In this paper, a 2.5V 10-bit 50MSamlpe/s Nyquist-rate CMOS pipelined ADC for IEEE 802.11a WLAN is presented. The pipelined ADC exhibits 70dB of SFDR and 60.5dB of SNDR with a 5MHz input, which corresponds to 10 effective bits of resolution. The power dissipation is 93mW at 2.5V supply voltage under 50MHz of sampling rate.

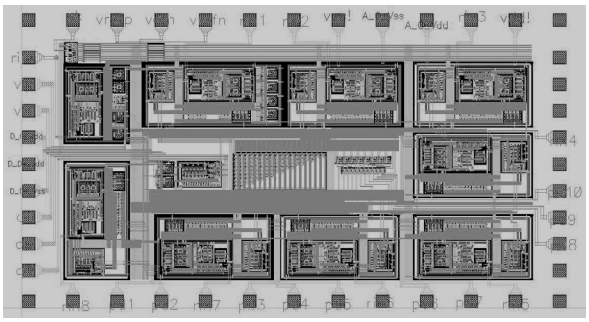


Fig. 4 The Whole Chip Layout

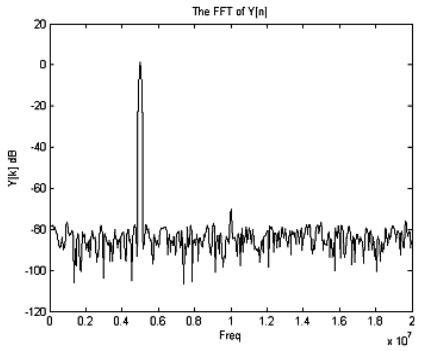
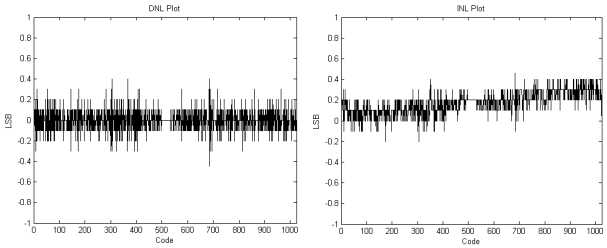


Fig. 5 Simulation SNDR with fin=5MHz



(a) (b)

Fig. 6 Simulated (a) DNL (b) INL

Table 1 Performance Summary

Resolution	10 bits
Sampling Frequency	50MHz
Supply Voltage	2.5V
Signal Range	$2.4V_{pp}$
SNDR	60.5dB @ Fin=5MHz
DNL	±0.45 LSB
INL	±0.46 LSB
Power Consumption	93 mW @2.5V
Core Area (without PADs)	2.8×1.5 mm^2
Process Technology	0.35μm 2P4M CMOS process

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