A Digital-Front-End Enhanced Multi-Mode/Multi-Standard Wireless Receiver

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Abstract: - This paper presents a multi-mode receiver concept for different transmission standards like UMTS and IS95. Due to the use of a Digital-Front-End (DFE) the requirements for the analog part of the well known direct conversion receiver (DCR) architecture decrease because channelization and fine frequency tuning are shifted from the analog into the digital domain. The adaptation of the channelization requirements subjected to the different transmission standards is limited in the analog domain by nature of their implementation. Shifting this functionality into the DFE greatly easies this task due to the availability of highly reconfigurable digital filter structures. Another challenge is the analog to digital conversion which is carried out with a high dynamic-range/low-power $\Delta\Sigma$-analog-to-digital-converter (ADC). The DFE also carries out an integer and fractional sample rate conversion to expand the flexibility and satisfy the requirements of different digital base band integrated circuits (BB-IC).

Key-Words: - Direct-conversion-receiver, Analog-to-digital-converter, Software-defined-radio, Multi-mode, WCDMA, Fractional-sample-rate-conversion

1 Introduction

The ideal software defined radio (SDR) receiver architecture, which directly samples the radio frequency (RF) signal after some amplification and filtering by an analog to digital converter (ADC), is shown in Fig.1. The whole digital signal processing is carried out in software by a digital signal processor (DSP) [1].

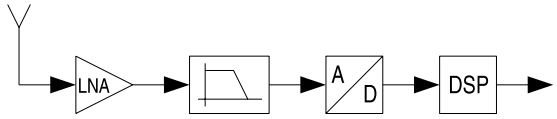

Fig.1 Ideal software design radio receiver

With this structure maximum flexibility can be achieved because only some fixed amplification and antialiasing filtering take place in the analog domain and the rest of the signal processing is carried out in a fully programmable DSP. Due to the high requirements for the ADC in terms of sampling frequency and dynamic range the ideal SDR is technically not feasible yet. In this paper an enhancement of the currently used direct conversion receiver (DCR) will be presented. To expand the flexibility as much as possible analog functions like channel selection filtering are shifted into the digital domain. As a consequence the requirements on the ADC increase, but are still much more relaxed compared to the original SDR architecture of Fig.1, because the input to the ADC is at base-band rather than RF. Reusing configurable blocks like, e.g. programmable FIR filters, for the supported wireless standards reduces the needed silicon area and thus costs of a multi-mode/multi-standard radio frequency integrated circuit (RFIC). This enables the use of one common reconfigurable front end to receive different transmission standards.

This paper is organized as follows: in the next section an explanation of the main parts of the receiver will be given. The following chapter will specify the used blocks of the DFE. A performance characterization for different wireless standards follows based on their specified test-cases. Finally, a conclusion will be given.

2 Receiver architecture

Fig.2 depicts the chosen receiver architecture with an analog DCR, which is currently the dominant architecture in the cellular market. The key advantage of the DCR architecture over the intermediate frequency (IF) receiver structure in terms of integration level is the replacement of the external IF-SAW (Surface Acoustic Wave) filter by low-pass filters, which are amenable to monolithic integration. Disadvantageous is the limited isolation between local oscillator to the RF path.

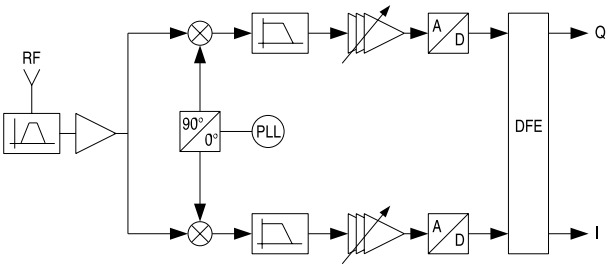

Fig.2 Block diagram of the DCR-receiver

Therefore, a part of the LO signal leaks into the RF path, is down converted to the base band by the mixer and results in an unwanted DC-offset. Furthermore, DCR receivers have stringent second order intercept point requirements of the IQ-mixers to limit the down- conversion of large amplitude modulated interferers to base-band. Also I/Q amplitude and phase mismatch can be a critical issue [2].

With the advent of RF-CMOS the implementation of the DFE locally on the RFIC has become technical feasible and also economically reasonable. The advantages of the RF-CMOS technology are:

- Analog base band filters and ADC with digital post-filtering can all be realized in the same technology
- Digital base band processing can be implemented in a state-of-the-art CMOS technology, which lowers costs and current consumption of the DFE

The main disadvantage of RF-CMOS based DCRs is the flicker noise at the mixer outputs, which leads to higher noise figures especially for narrow band systems like GSM.

2.1 RF Front-End

By using an oversampled ADC architecture the specification for the analog anti-aliasing low-pass filter (AAF) can kept simple. Simulationeously, the channelization is facilitated in DFE. An analog gain control is implemented to use the available ADC-dynamic range more efficiently.

2.2 Analog–To-Digital Converter

To relax the specifications of the analog low pass filters in front of the DFE, an over-sampled $\Delta\Sigma$-ADC architecture with a high clock rate in the order of 100 MHz is proposed [3]. Especially the selectivity of the analog filter can be relaxed, i.e. different radio standard can use the same or only a slightly modified analog filter. The ADC has to handle signals with very large dynamic range and bandwidth due to the fact that the worst case adjacent channel interferers have to be converted, too, without deteriorating the wanted signal. An overview of the specifications for the different transmission standards is given in Table 1. The signal to noise ratio of a $\Delta\Sigma$-ADC is defined by

$$SNR_{OSR}^{L} = 20\log\frac{\sigma_x}{V_{pp}} + 10.8 + 6.02N + 10\log\frac{2L+1}{\pi^{2L}} + \\ + 10(2L+1)\log \mathrm{OSR} \qquad \text{for } \mathrm{OSR} \geq 4 \qquad (1)$$

with bitwidth N, loopfilter order L and over sampling ratio OSR.

Table 1 Specification of Multi-Mode ADC

Mode	No. of eff. bits	Dynamic range	Bandwidth
IS95	14	86dB	650 kHz
UMTS	11.5	71dB	1920 kHz

2.3 Digital Front End

The DFE architecture considered in this paper is shown in Fig.3. The main tasks are channel selection and decimation.

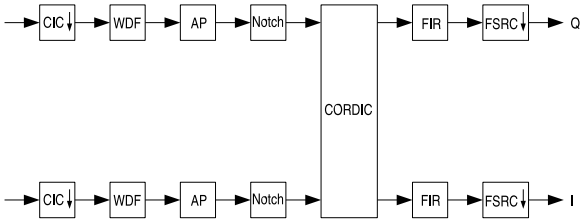

Fig.3 Proposed DFE-receiver architecture

This is realized for the different standard requirements by highly configurable filter blocks. Due to the fact that not all blocks are required for the different standards also the sequencing of the blocks with the exception of the CIC filter can be changed. The cascaded-integrator-comb (CIC), wave digital filter (WDF), all-pass (AP), FIR and fractional sample rate conversion (FSRC) are used for channelization and decimation. CIC and WDF filter are chosen due to their efficient implementation in terms of die area and power consumption. To achieve a fine frequency resolution a coordinate-rotation-digital computer (CORDIC) is implemented in the DFE. This eases the PLL design in terms of required minimum frequency

step size. The different blocks will be detailed in the following section.

3 DFE Filter Implementation

For high reconfigurability the sequencing of the filter moduls can be adapted. Therefore, the filters are optimized for a 16 bit data-path and the filter-coefficients use 12 Bit. CIC filters are used to effectively change the sampling rate by an integer factor [4].

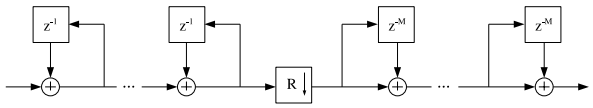

Fig.4 Block diagram of a N-th order CIC decimator

The N-th order CIC decimator is built of N cascaded integrators clocked at input sample rate, a configurable sample rate reduction and N cascaded comb stages running at the reduced output sample rate. The transfer function of the CIC with a sample rate reduction R at input sample rate is given by

$$H_{cic}(z) = \left(\frac{1 - z^{-RM}}{1 - z^{-1}} \right)^N \tag{2}$$

where M defines the number of delay elements used in the comb stage and N is the number of integrator and comb stages. The major drawback in using CIC filters is the pass-band droop and loss in anti aliasing attenuation if the signal is decimated directly from the high ADC-rate to 2 times or 4 times chip- or symbol rate.

The channelization and final integer decimation is performed in WDF [5]. An N-th order lattice low-pass WDF is built of N adaptors (all-pass sections) distributed over two branches. Each adaptor requires one hardware multiplier. The transfer function of a first and second order lattice adaptor is defined by

$$A_1(z) = \frac{1 - \gamma_1 z}{z - \gamma_1} \tag{3}$$

$$A_2(z) = \frac{1 + (\gamma_2 - 1)\gamma_1 z - \gamma_2 z^2}{-\gamma_2 + (\gamma_2 - 1)\gamma_1 z + z^2} \tag{4}$$

The transfer function of the 7-order WDF is given by:

$$H_{WDF7}(z) = \frac{1}{2}\left[\left(A_1(z) A_2(z) \right) + \left(A_2(z) A_2(z) \right) \right] \tag{5}$$

Due to the fact that the adaptors are all-pass stages, only the phase of the signal is changed and the amplitude is constant. An additional advantage is the robustness in quantization noise of data and coefficients. For some modes the WDF can also be used perfectly for last stage integer decimation by factor 2 using half band configuration and a 5-th order WDF. A disadvantage of the WDF is the introduced group delay ripple. The filter can be optimized in terms of constant group delay with numerical optimization methods. This normally leads to a reduction of the stop-band attenuation.

A FIR filter is used for two reasons. First, for pulse filtering according to the communication standard under consideration (e.g. RRC for UMTS). Since pulse shaping vary among the different standards, the FIR filter implementation must have configurable filter coefficients and the maximum number of taps has also to be chosen to satisfy the required stop-band attenuation.

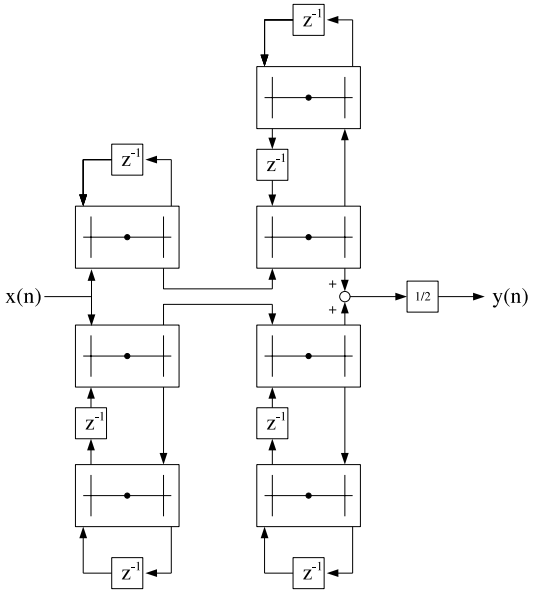

Fig.5 Block diagram of the 7-th order lattice low-pass WDF build of seven adaptors in two branches

Second, the FIR filter acts as equalizer to reduce the amplitude ripple in the pass band introduced by the CIC and WDF stages. Due to implementing the filter using polyphase decomposition, the effective number of hardware resources can be reduced significantly.

To correct the pass-band group delay ripple introduced by the WDF a reconfigurable AP is used. The CORDIC adjusts fine frequency offsets and its function is sketched shortly below:

The CORDIC-algorithm is an iterative algorithm [6]. During the n-th CORDIC iteration, the input vector (I_0,Q_0) is rotated by successively decreasing elementary rotations with the pre-defined basic angle

$$\alpha_n = \arctan(2^{-n}) \qquad n = (0,1,...,N-1)\,. \tag{6}$$

The resulting iterative process to realize all micro-rotations by simple shift-add operations can be described by the following equations

$$I_{n+1} = I_n - d_n \cdot Q_n \cdot 2^{-n} \tag{7}$$

$$Q_{n+1} = Q_n + d_n \cdot I_n \cdot 2^{-n} \tag{8}$$

$$z_{n+1} = z_n - d_n \cdot \alpha_n \tag{9}$$

with

$$d_n = \begin{cases} -1 & \text{if } z_n < 0 \\ +1 & \text{otherwise} \end{cases} \tag{10}$$

specifying the direction for each rotation. The transfer characteristic of a CORDIC after N iterations result in

$$\begin{bmatrix} I_N(k) \\ Q_N(k) \end{bmatrix} = K \cdot \begin{bmatrix} I_0(k) \\ Q_0(k) \end{bmatrix} \cdot \begin{bmatrix} \cos(z_0(k)) & -\sin(z_0(k)) \\ \sin(z_0(k)) & \cos(z_0(k)) \end{bmatrix} \tag{11}$$

with $z_N \approx 0$ and the constant scaling factor

$$K = \prod_{n=0}^{N-1} \sqrt{1 + 2^{-2n}} \approx 1.6 \quad . \tag{12}$$

which is independent of the rotation angle z_n.

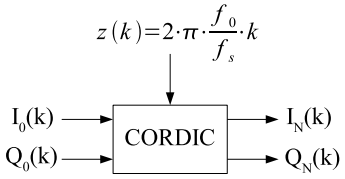

Fig.6 CORDIC based frequency correction

Let f_0 be the frequency offset to be corrected, then the complex-valued base-band signal $I(k)+jQ(k)$ is multiplied by $e^{-jz(k)}$ with

$$z_0(k) = -2\pi \frac{f_0}{f_s} k \tag{13}$$

and f_s is the sampling frequency.

The ADC of the proposed architecture is normally driven by a fixed sample clock in the order of 100 MHz. If the digital interface towards the base-band should deliver samples at a rate that is an integer multiple of the symbol rate of the standard under consideration, a FSRC must be considered. To reduce the aliasing requirements the FSRC is performed as last filter. Thus, the previous filter stages have already attenuated a possibly present adjacent channel signal. To limit power consumption the desired sample rate of the digital interface should be as low as possible. Due to the Nyquist-theorem the lowest possible data rate at the digital interface is two times the symbol/chip rate. In some cases it is advantageous for the succeeding base-band processing that the sample rate is four times higher than the respective symbol/chip rate. The FSRC block is implemented as a second order Lagrange interpolation FSRC and interpolates between three sampling in- stances as shown in Fig.7. The advantage compared to the linear interpolation which is simpler to implement is the higher image rejection and anti aliasing property. This leads to a better performance in terms of Error Vector Magnitude (EVM) and Bit Error Rate (BER).

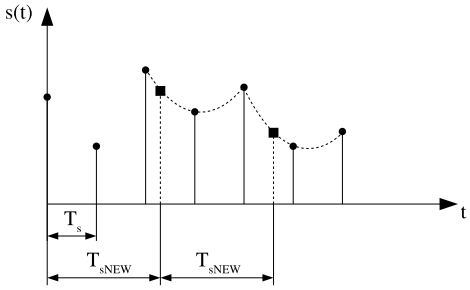

Fig.7 Principle of 2-nd order FSRC

4 Simulation results

A simulation chain of the proposed DFE architecture together with a $\Delta\Sigma$-ADC model has been implemented and simulated for the cellular communication standards UMTS and IS95. The used $\Delta\Sigma$-ADC was clocked in the order of 100 MHz. The designed DFE frequency response for UMTS with an OSF of two at the DFE output is shown in Fig.8. The resulting amplitude- and group delay ripple at the output of the DFE are 0.05 dB and 12 ns compared to the ideal RRC-transfer function.

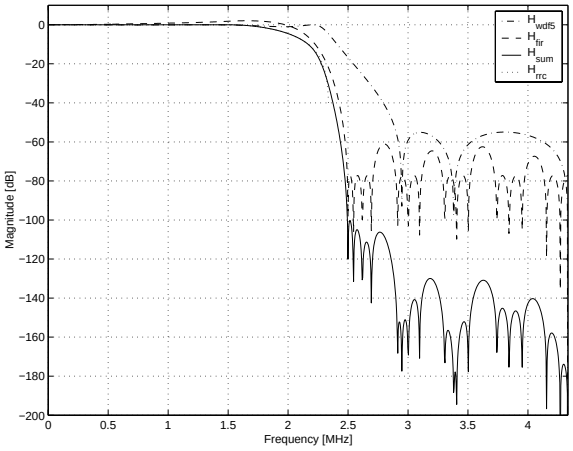

Fig.8 Frequency response of the DFE designed for UMTS-signals for two times OSR at the output

The delivered signal fidelity after the DFE was checked by means of EVM and in the case of UMTS also by BER-simulations. These simulations were performed with and without adjacent channels. The BER simulations as shown in Fig.9 of the implemented UMTS-DFE (dotted lines) are compared to an ideal RRC-filtered front end (solid lines) depending on a change of the interfering noise power (I_{oc}). It can be seen that without an adjacent channel a degradation of only 1dB by a BER of 10^{-3} occur compared to the ideal, floating point, front end. The degradation of the BER performance for the ideal RRC-filtered front end with the adjacent channel selectivity testcase is 1.5 dB at a BER of 10^{-3}. The powerlevel of the adjacent channel signal is in this testcase 40 dB above the level of the desired frequency channel. The impairment due to the implemented DFE is additionally about 0.5 dB.

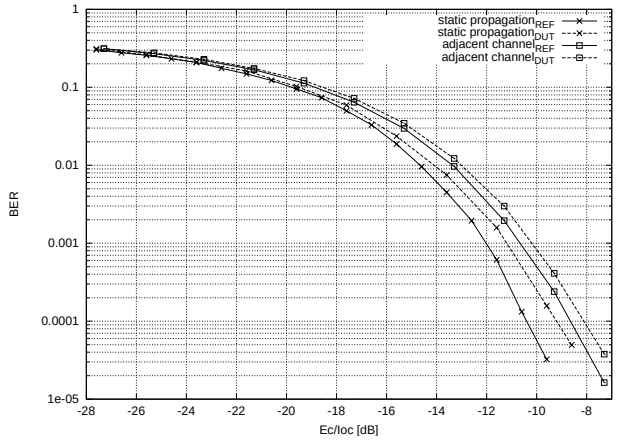

Fig.9 Bit error performance for the static propagation conditions UMTS-testcase and the adjacent channel selectivity testcase

Fig.10 shows the signal at the ADC input for the UMTS (ACS) testcase. Fig.11 clearly shows that the adjacent channel is suppressed by at least 80 dB at the DFE output. Simultaneously the signal is decimated to two times the UMTS symbol/chip rate of 7.68 Mcps. Fig.12 shows the signal at the ADC input for the IS95 single tone desensitization testcase. The interfering signal has a frequency modulation with a bandwidth of 30 kHz and a frequency offset of only 900 kHz from the center frequency of the desired channel. The interfering signal power level is 71 dB larger than the desired channel power. Fig.13 shows that the suppression at the interfering signal frequency is about 120 dB and the signal is decimated to four times the IS95 symbol/chip rate of 4.9152 Mcps. The EVM- results are summarized in Table 2.

Table 2 EVM Simulation results for the specified testcases with and without interferer

Mode	EVM (w/o) adj	EVM (w/ adj)
UMTS	3.1%	7.2%
IS95	3.3%	7%

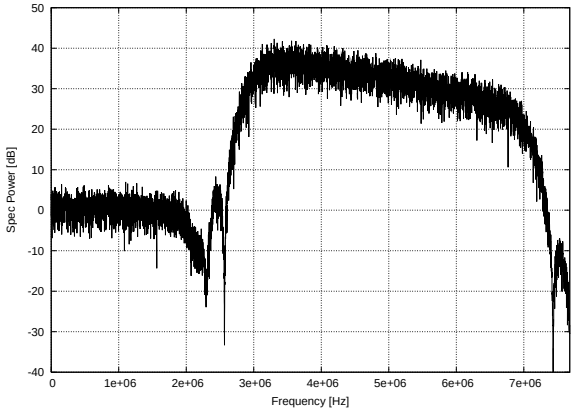

Fig.10 Input spectrum of the DFE with adj. channel in UMTS-mode

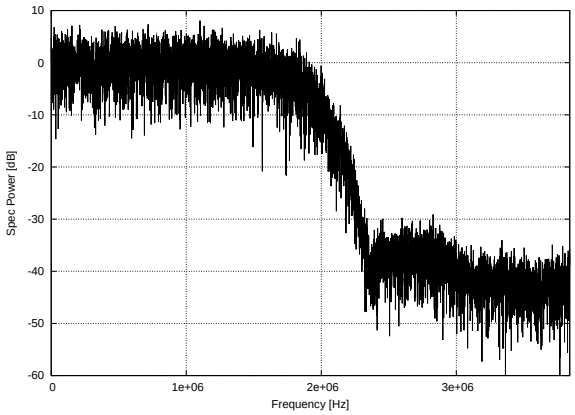

Fig.11 Output spectrum of the DFE with adj. channel in UMTS-mode

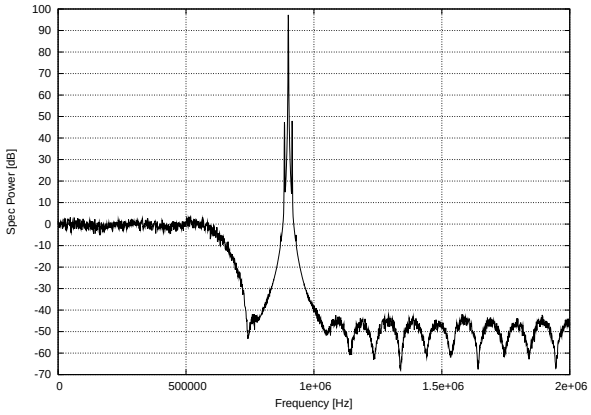

Fig.12 Input spectrum of the DFE with AMPS interferer in IS95-mode

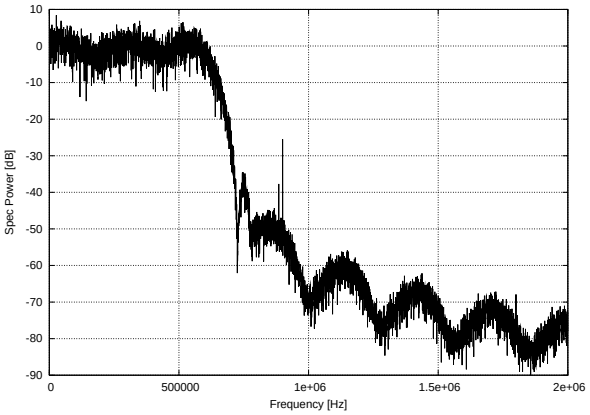

Fig.13 Output spectrum of the DFE with AMPS interferer in IS95-mode

5 Conclusion

In this work the enhancement of the state of the art DCR architecture with a DFE has been investigated. It is a first step into a fully reconfigureable RF front-end. Due to shifting analog functionalities like channelization into the digital domain it is possible to reconfigure the DFE for different transmission standards. The used $\Delta\Sigma$ -ADC relaxes the requirement for the analog filter. Tuneable band pass filters could be a further extension for the analog front end.

It can be stated that this concept has a high level of flexibility and is a feasible solution for future multi-mode/multi-standard wireless communication systems.

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