A 1000W RMS Class D Amplifier with Feedback

F.R.S. Vincenzi; L.C. Gomes de Freitas; N. J. Moreira Jr; E.A.A. Coelho; J.B. Vieira Jr. and L.C. de Freitas
Faculty of Electrical Engineering - FEELT
Federal University of Uberlândia - UFU
Campus Santa Monica – Bloco 3N – Uberlandia/MG
Brazil
http://www.feelt.ufu.br

Abstract: - This paper presents a new Class D power amplifier suitable for sub-woofer and woofer. The proposed topology has high efficiency (more than 90%) when operating at nominal power. The proposed topology does not need an output low pass filter to remove the high switching frequency because it uses two current sources to modulate the desired waveform in an output capacitor. This operation plus the feedback control provides low THD (less than 1%) and there is no need to use controlled voltage source supplies as in the conventional Class D structure.

Key-Words: - Class D amplifier, THD, Current source

1 Introduction

The principal advantage of the Class D amplifiers over the traditional linear amplifiers (Class A, B and AB) is that the efficiency rate can reach over 90% if well designed [1]. The higher efficiency of the Class D amplifier over the linear amplifiers make it more attractive for use with battery operated equipment such as car amplifiers, walkmans, small radios, walkie-talkies, etc. There is no advantage in using linear amplifiers in power applications as they are heavy, big and have low efficiency compared to a Class D amplifier.

The conventional Class D amplifier, Fig. 1, has a pulse width modulator (PWM), a power stage and a low pass band filter in the output stage. At the PWM stage the reference signal is compared with a high frequency triangular wave. The comparison result is composed of digital pulses so that the duty cycle is proportional to the instantaneous input voltage.

Due to the low voltage supply, the output stage is usually configured as a bridge output to increase the power by four times (over a single ended output). The output low pass filter is used to remove the harmonic components of the PWM output leaving only the amplified reference signal on the load.

The fundamental problem of the digital PWM-based topology is that the power stage can not easily be encompassed by general feedback. Since the power-supply level “generates” the PWM signal directly, any power-supply variation will be reflected as distortion in the audio waveform. [2]

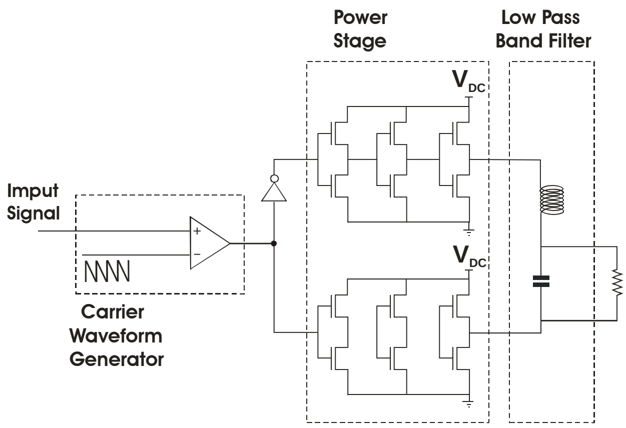

Fig. 1 - Conventional Class D amplifier

The proposed topology does not need controlled voltage source supply because the control uses feedback so THD below 1% is achieved without an additional output low pass filter. The proposed topology presented in this paper, Fig. 3, has the following main advantages over the topology presented in previous papers, Fig.2, [3]-[6].

- It has two switches and consequently two isolated gate drivers against four switches and consequently four isolated gate drivers compared to the topology presented in previous works
- It is not necessary to use snubbers on the two switches
- It has higher efficiency

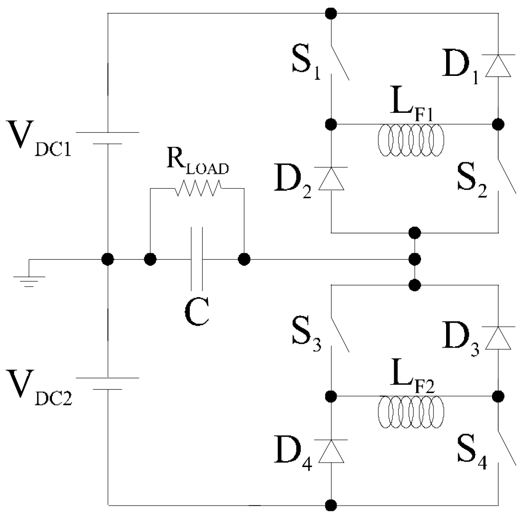

Fig.2 – Class D amplifier from previous papers [3]-[6].

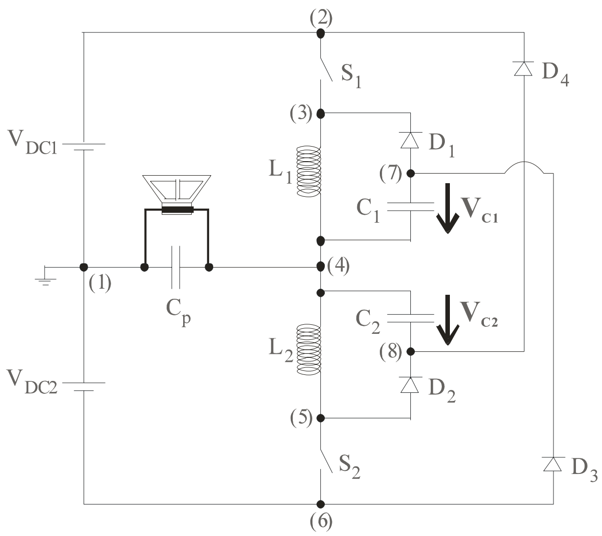

Fig.3 – Proposed Class D amplifier

The proposed arrangement can be used to compose a full-bridge configuration with the advantage of using only one power supply but it would double the switches, diodes, inductors and isolated drivers.

The proposed half-bridge configuration uses a non controlled symmetrical power-supply that can be built using a voltage multiplier configured as a voltage doubler.

For example, a voltage multiplier that increases the peak input voltage twice is called a voltage doubler. Voltage multipliers increase voltages through the use of series-aiding voltage sources.

2 Design Guide

The maximum slew-rate has to be considered for correct amplifier design. To determine the slew rate it is necessary to choose either triangle waves or sine waves as an input signal to test the amplifier. It makes no sense to talk about the slew rate of a square wave, since theoretically the slew rate of a perfect square wave is infinite.

The mathematical analysis based on sine wave input signal simplifies the mathematical study and in this case the instantaneous input signal is represented by equation (1).

$$V(t) = V_{pk}.\sin(\omega.t) \qquad (1)$$

where:

- V_{pk} - is the peak potential of the sine wave;
- ω - is the angular velocity, or radian frequency, and it is equal to $2.\pi.f$;
- t - is the instantaneous time of interest.

The differentiation of equation (1) results in the desired slew-rate, equation (2).

$$\frac{V(t)}{dt} = \omega.V_{pk}.\cos(\omega.t) \qquad (2)$$

The maximum rate occurs at the zero crossing over to the maximum frequency to be amplified when $\cos(0)=1$. This means that the term $\cos(\omega.t)$ in equation (2) can be dropped resulting in equation (3).

$$\frac{V(t)}{dt} = \omega.V_{pk} \qquad (3)$$

Equation (4) relates current and capacitance. This equation is very important for calculating the current needed to produce the desired slew rate on a capacitor.

$$I = C.\frac{dV}{dt} \qquad (4)$$

Combining (3) and (4), it is found that the current can be calculated by equation (5).

$$I_{pk} = 2.\pi.f_{\max}.C.V_{pk} \qquad (5)$$

where:

$f_{\max}$ - is the maximum frequency to be amplified

For the positive slope on C_p capacitor Fig. 4 and Fig. 5 show that inductor L_1 charges capacitors C_p and C_1 and discharges capacitor C_2. The charging and discharging processes happen basically at the same time because the switching frequency is high. So the circuit shown in Fig. 6 can be used to find the current equation that produces the maximum slew-rate.

where:

- Capacitor C_T is the sum of capacitances C_p, C_1 and C_2;
- At t = 0s the inductor's current is zero;
- At t = 0s the capacitor's voltage is zero.

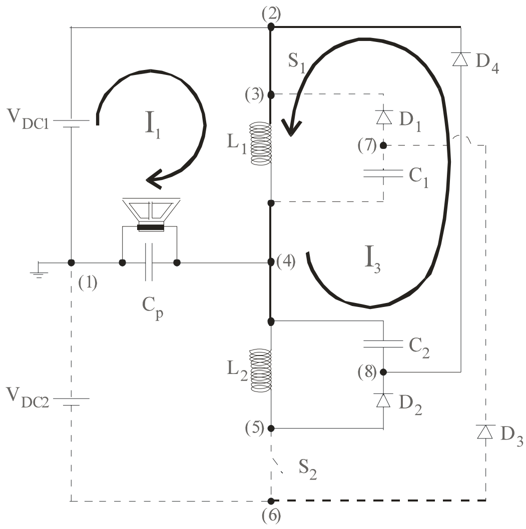

Fig.4 – Charging C_p and discharging C_2 (Positive Slope).

Equation (6) represents the instantaneous current of the LC circuit shown in Fig. 6.

$$I(t) = \frac{V_{DC}}{Zo}.\cos(\omega.t) \qquad (6)$$

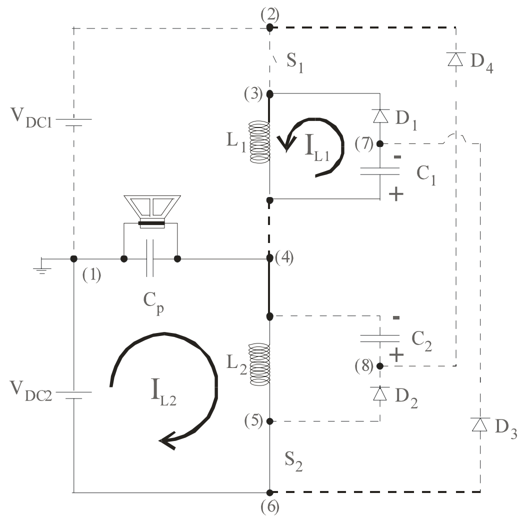

Fig.5 - Charging C_1 and discharging C_p (Positive Slope).

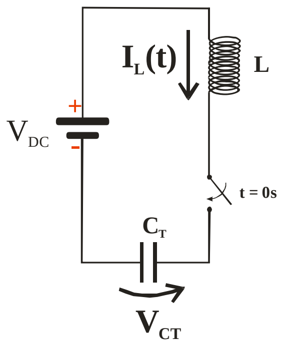

Fig.6 - LC equivalent circuit (Positive Slope).

The maximum current occurs when t=0 since $\cos(0)=1$. This means that the term in Equation (6) can be dropped resulting in Equation (7).

$$I_{pk} = \frac{V_{DC}}{Zo} \qquad (7)$$

where:

$$Zo = \sqrt{\frac{L}{C_T}}$$

Combining Equation (5) and (7) results in Equation (8).

$$L = \frac{V_{DC}{}^2}{4.\pi^2.f_{max}{}^2.V_{pk}{}^2.C_T} \qquad (8)$$

Notice how driving impedance is never considered. This is because it has nothing to do with slew-rate. The impedance is considered for frequency response and/or filter analysis. It is interesting to note that the maximum slew-rate occurs (at the zero crossing) when the current is maximum and voltage is zero. If the voltage is zero the impedance is unable to drive any current.

The total capacitance C_T is the sum of capacitances C_p , C_1 and C_2. Good values for C_1 and C_2 are $C_p \le (C_1 = C_2) \le 2.C_p$.

3 Design Example

The aim of this project is to drive a 800W RMS, 18 inch and $8\,\Omega$ woofer. Fig 7. shows that the three way system divide the frequency as follows:

- 10 – 700Hz (woofer)

- 700 – 4kHz (midrange)

- above 4kHz (tweeter)

The amplifier will be designed to supply the 45% of total power to the woofer and it will have a cut-off frequency of 2kHz which is more than necessary to drive a woofer. A sub-woofer amplifier design has to assume a cut-off frequency of 4kHz.

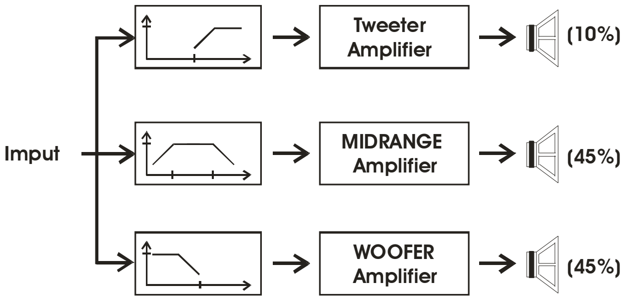

Fig.7 - Active loudspeaker system (three-way) based on separate amplifiers for each band. Also shown is the typical necessary relative power-handling capability of the power amplifiers on each band.

Fig. 7 shows that 45% power of a 3 way sound system goes to the woofer, 45% goes to midrange and 10% goes to tweeter.

Frequency signals (lower than 10Hz) must be removed, before it is amplified, to avoid unpleasant pumping effect.

Table 1: Design Specification

Po	800W
$Vo_{(pk)}$	114V
$f_{\max}$	2kHz
$I_{L1(pk)} = I_{L2(pk)}$	$\cong I_{LOAD}$
V_{DC}	144V

Table 1 shows a 800W switched power amplifier specification.

The nominal RMS load voltage (Vo) is:

$$Vo = \frac{Vo_{(pk)}}{\sqrt{2}} \tag{9}$$

$$Vo = \frac{114}{\sqrt{2}} = 80V$$

$$Po = Vo.Io \tag{10}$$

where:

Po = nominal RMS output power
Vo = nominal RMS output voltage
Io = nominal RMS output current

The nominal RMS load current is given by Equation (10).

$$Io = \frac{800W}{80V} = 10A$$

The load peak current is:

$$Io_{(pk)} = 10A.\sqrt{2} = 14{,}14A$$

Using Equation 5 C_T is calculated as follow:

$$C_T = \frac{14{,}14A}{2.\pi.2kHz.114V} = 10\mu F$$

Making $C_1 = C_2 = 2.C_S$ the capacitance C_p, C_1 and C_2 is:

$$C_1 = C_2 = \frac{2}{5}.C_T = \frac{2}{5}.10\mu F = 4\mu F$$

$$C_p = \frac{C_T}{5} = \frac{10\mu F}{5} = 2\mu F$$

Finally the L_1 and L_2 inductance value is obtained by Equation 8.

$$L_1 = L_2 = \frac{(144V)^2}{4.\pi^2.(114V)^2.(2kHz)^2.(10\mu F)}$$

$$L_1 = L_2 = 1mH$$

4 Control Strategy

A very simple control method was developed and constituted basically from a comparator with a very narrow hysteresis, Fig. 8(a).

The desired signal is faithfully reproduced on the C_p capacitor because the complementary switching (when one switch is off the other is on) of S_1 and S_2 switches is originated from the comparison between the reference signal (applied to the non inverting input of the operational amplifier) and the output voltage sample (applied to the inverting input of the operational amplifier). If the comparator output voltage is positive the switch S2 is turned off and S1 on. If the comparator output voltage is negative S1 is turned off and S2 on as can be seen in Fig. 8(b).

The switching frequency depends on how fast the comparator, feedback and gate driver are. For the implemented converter the switching frequency is above 50kHz.

It is desirable that the conventional Classe D operates on a determined switching frequency which simplifies the output low pass filter design. Although the proposed topology uses two current sources in order to modulate the desired signal on the output Cp capacitor so that THD at less than 1% can be achieved.

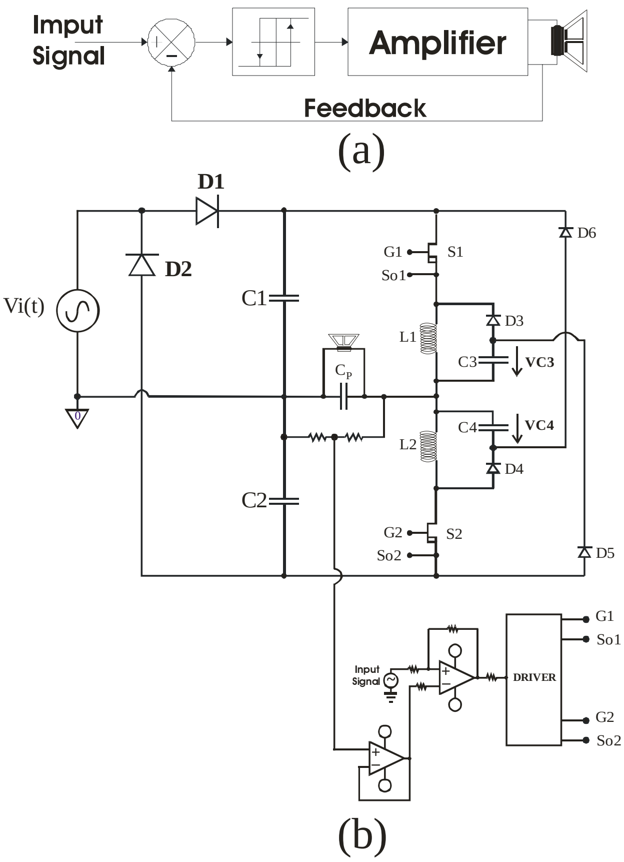

Fig. 8: (a) Control block diagram, (b) Voltage doubler, control circuit and proposed topology.

5 Experimental Results

Fig. 9 and Fig. 10 shows the efficiency and THD experimental results from a laboratory prototype built with the same specification presented in Table 1. One can see in Fig. 9 that for a 800W output power the efficiency is 92% and THD is 0,84% (Fig. 10). The 1137W output power was measured using a 5Ω resistive load. This was made possible as the inductors and switches used on the prototype have a greater design specification than those presented in the design example of section three.

For a better understanding of the converter's behaviour, Bode plots were drawn from experimental data. In the Bode plots one observes that the curve falls at a rate of approximately 12dB/oct, characterizing a second order system response and that the cut-off frequency is in accordance with design specification.

Fig. 12 shows a experimental result waveform where the upper signal is the output voltage on Cp capacitor and the lower waveform is the input reference signal.

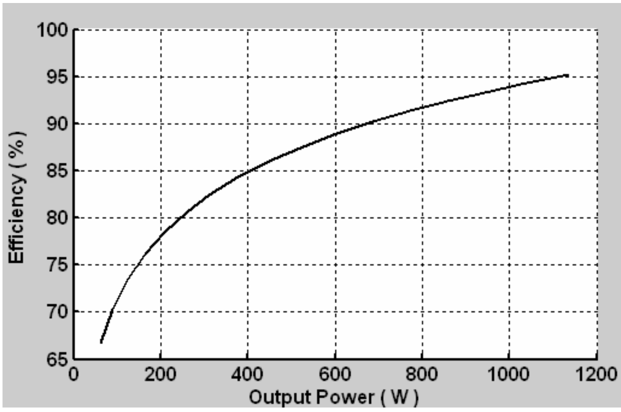

Fig. 9. - Efficiency of the proposed amplifier.

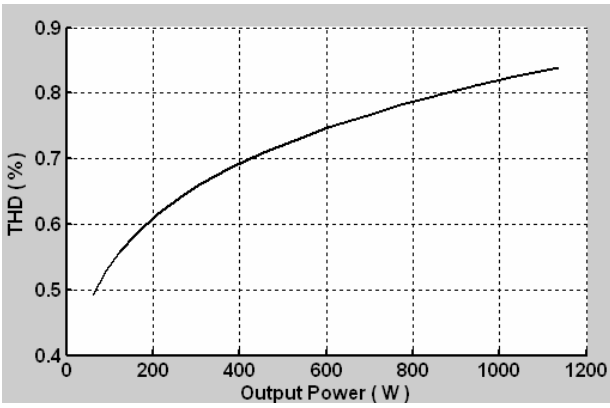

Fig. 10. - THD of the proposed amplifier.

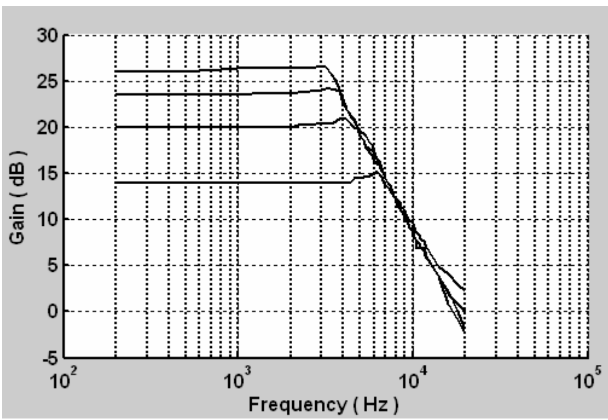

Fig. 11.- Voltage gain response.

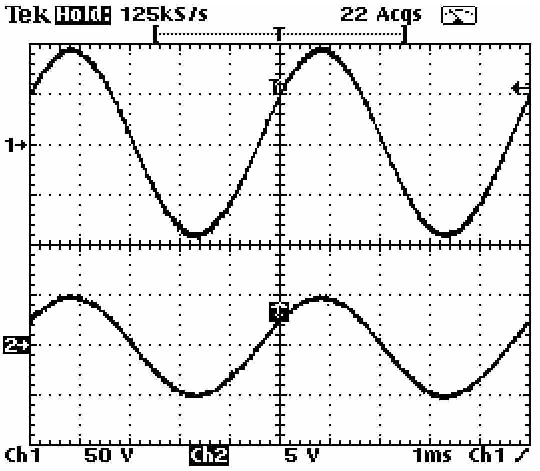

Fig. 12.- Experimental Waveform
Upper Wave Form – Output Voltage on V_{CP} ;
Lower Wave Form – Reference Input Signal;

6 Conclusion

This paper presented a new Class D power amplifier with efficiency over 90% and THD at less than 1%. This structure does not need controlled power source supply and neither an output low pass filter as with the conventional Class D amplifiers.

References:

[1] Chang, M. T. Tan, Z. Cheng and Y. C. Tong. “Analisys and Design of Power Efficient Class D Amplifier Output Stages.” IEEE Trans. Circuits and Systems I: Fundamental Theory and Applications, vol. 47, no. 6, pp. 897-902, 2000.

[2] K. Nilsen “High-Fidelity PWM-Base Amplifier Concept for Active Loudspeaker Systems with Very Low Energy Consumption” J. Audio Eng. Soc., vol. 45, no. 7/8, pp. 554-570, 1997.

[3] F. R. S. Vincenzi, et al., “Amplificador de Áudio Chaveado” SEMEA- Seminário de Engenharia de Áudio, Belo Horizonte - MG. Editora da UFMG, CD-ROM, vol. único, 2002.

[4] F. R. S. Vincenzi, et al., “A New Audio Switched Power Amplifier” INTELEC - International Telecommucations Energy Conference, Copenhege. Proceedings of IEEE INTELEC'1999. Psicataway - NJ - USA: IEEE PRESS. vol. único, pp. 01-06, 1999.

[5] F. R. S. Vincenzi, et al., “A Switched power Amplifier for Audio Application” COBEP - V Congresso Brasileiro de Eletrônica de Potência, Foz do Iguaçu PR. Anais do COBEP'1999. Foz do Iguaçu PR: Imprensa Universitária da UFPR, vol. 02, pp. 521-526, 1999.

[6] F. R. S. Vincenzi, et al., “A new switched Power Amplifier for High Power Applications”. INTELEC – International Telecommucations Energy Conference Copenhage. Proceedings of IEEE'1999. Psicataway - NJ- USA: IEEE PRESS, vol. único, 1999.