High Speed Pipelined Booth Multiplier for DSP Applications

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Abstract: - In this paper, a new MBE (modified Booth encoding) recoder, and a new MBE decoder are proposed in CMOS transistor level to improve the performance of traditional multipliers. The proposed pipelined Booth multiplier can reduce the delay time of the critical path by levelizing the complex gate in the MBE decoder. As a result, MBE decoder is no more the speed bottleneck of a pipelined booth multiplier, and the speed of the MBE decoder can be improved up to 66.3 percent. Besides, an 8-bit by 8-bit glitch-free Booth multiplier is pipelined as a traditional pipelined array multiplier without any bottleneck in the MBE encoder and decoder, but with better performance in both power and speed. Finally, a low voltage, high speed pipelined glitch-free Booth multiplier architecture is presented at 1 GHz in TSMC 0.35um process with a power consumption of only 100.52mw.

Key-Words: - Booth multiplier, MBE recoder, MBE decoder, Pipeline, DSP, Glitch-free

1 Introduction

A digital multiplier is one of the main fundamental cells in digital signal processors (DSP) and central processing units (CPU). The performance of a multiplier is usually the speed bottleneck of above-mentioned digital systems [1].

The modified Booth algorithm is a common approach to the VLSI design of high speed multipliers because the number of additions in multiplication is halved [1]. The Wallace tree architecture is also usually used to accelerate multiplication by compressing number of partial products, however, the power and area become large due to the large number of transistors and the complexity of interconnect. Furthermore, Wallace tree is not suitable for the pipelined multiplier because of complex serial computations [1]. As for Booth multiplier, its major problem is the large power dissipation due to lots of unnecessary glitches caused by different propagation delay times through different paths in both the MBE recoder and MBE decoder [1, 2]. Recently, a glitch-free MBE recoder and MBE decoder which eliminates the unnecessary glitches associated with the Booth multiplier is proposed to reduce the multiplier array power dissipation by about 30% and to increase speed by about 10% [2, 3]. In this paper, the MBE recoder design is further improved in CMOS transistor level which provides a better performance.

The pipelining is a popular technique to increase throughput of a high speed system, which divides total system into several small cascade stages and adds some registers to synchronize outputs of each stage. Also parallel-pipeline architecture is considered to be most suitable for low voltage and low power systems [4, 5, 7]. In a pipelining system, the maximum operating frequency is limited by the slowest stage which has the longest delay time. In the pipelined Booth multiplier, MBE recoder and MBE decoder is the slowest stage that becomes the critical path (bottleneck). In this paper, we will propose a new MBE decoder to reduce the delay time in the critical path by about 66.3% by levelizing the complex gate in the MBE decoder and dividing it into small cascade stages.

Some techniques used to improve sign extension in both aspects of speed and power by sign generating skills [2, 3, 8] are also adopted

in our design. Besides, a high performance register called PTTFF (pulse triggered TSPC flip flop) is adopted to reduce both extra delay time and power consumption [9].

2 Modified Booth Encoder and Partial-Product Generator

According to the modified Booth algorithm [1], the MBE can be defined and implemented in many ways. Traditional implementations of the modified Booth algorithm are slow and consume large power because of large difference between gate delays. A glitch-free MBE recoding scheme using the redundant encoding technique which only has two gates delay is illustrated in Table 1 and Figure 1 [2].

Table 1 Truth table of glitch-free MBE

Y_{2i+1}	Y_{2i}	Y_{2i-1}	Yb	NEG	X1	X2P	ZP
0	0	0	0	0	0	1	1
0	0	1	+1	0	1	0	1
0	1	0	+1	0	1	0	0
0	1	1	+2	0	0	1	0
1	0	0	-2	1	0	1	0
1	0	1	-1	1	1	0	0
1	1	0	-1	1	1	0	1
1	1	1	0	1	0	1	1

In Table 1, Yb represents the recoding value according to the modified Booth algorithm. NEG implies Yb is negative or positive, X1 implies $|Yb| = 1$ or not, X2P = X1, and ZP implies $|Yb| = 2$ or $|Yb| = 1$. In this scheme, a fast glitch-free modified Booth algorithm is implemented with only 12 transistors in MBE recoder and 20 transistors in MBE decoder.

In this previous work, all XOR/XNOR gates are realized only by 4 transistors, however, all of them either need complementary inputs which are implemented by 2 transmission gates or can not provide full swing output signals by XOR/XNOR gates proposed in [10]. Besides, all such implementations are unable to produce both the XOR and complementary XNOR functions at the same time. Therefore we implement all XOR/XNOR gates in the MBE recoder and MBE decoder by a 6-transistor CMOS XOR circuit with complementary outputs [11]. As a result, our new MBE recoder can provide full swing output signals to eliminate the static leakage current in the next stage. Our new MBE recoder circuit is illustrated in Figure 2.

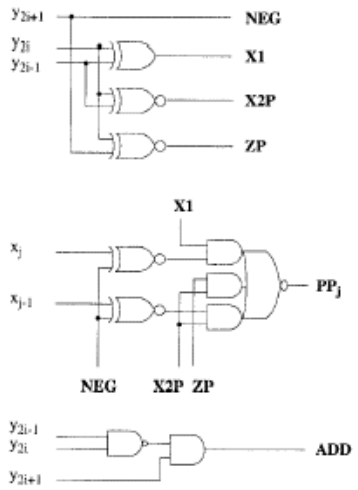
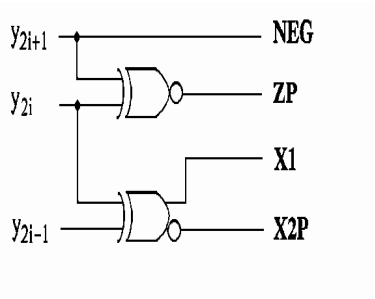


Figure 1 Implementation of traditional glitch free modified Booth algorithm.



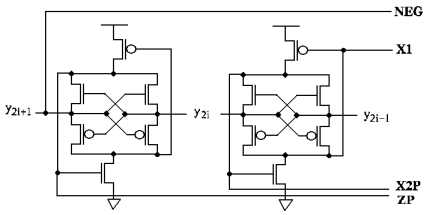


Figure 2 Proposed encoder for the glitch-free MBE scheme in gate level and in transistor level.

In the Figure 1 design, the delay from X and Y to PP_j is one XOR/XNOR gate delay plus one complex gate delay. However, the delay time in the complex gate of MBE decoder is still large to be the bottleneck in a pipelined Booth multiplier because of its large fan-in. To reduce the delay time in the complex gate, we can levelize the complex gate into 3 stages by the following equation:

$$
\begin{aligned}
PPj &= \overline{\overline{X1 \cdot \overline{Xj \oplus NEG}} + \overline{X2P \cdot ZP} + \overline{X2P \cdot \overline{Xj-1 \oplus NEG}}} \\
&= \overline{\overline{X1 \cdot \overline{Xj \oplus NEG}} + \overline{X2P \cdot (ZP + \overline{Xj-1 \oplus NEG})}} \\
&= \overline{(X1 \cdot \overline{Xj \oplus NEG}) \cdot \overline{(X2P \cdot (ZP + \overline{Xj-1 \oplus NEG}))}} \\
&= \overline{\overline{(X1 \cdot \overline{Xj \oplus NEG})} \cdot \overline{(X2P \cdot (ZP + \overline{Xj-1 \oplus NEG}))}} \quad \cdots\cdots (1)
\end{aligned}
$$

From equation (1), the delay time in one complex gate of fan-in 6 can be divided into the delay time of 3 stages which include one complex gate of fan-in 3, one NAND gate of fan-in 2, and one inverter. Because of much smaller loading capacitance at each stage of the levelized new MBE decoder, we can accelerate the speed of critical path in the MBE decoder. Also we can provide fast rise time and fall time because of the inverter in the output stage of the levelized new MBE decoder. As a result, the new MBE decoder with better performance in both speed and power respects because of larger driving force in a very high speed multiplier. The new MBE decoder is presented in transistor level in Figure 4 compared to the MBE decoder proposed in [2] in Figure 3.

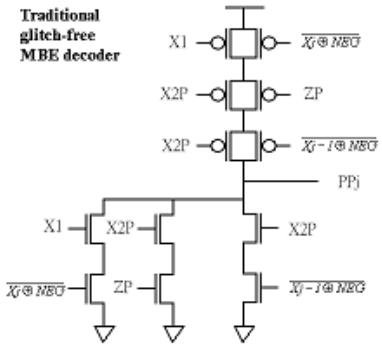


Figure 3 The MBE decoder in transistor level proposed in [2].

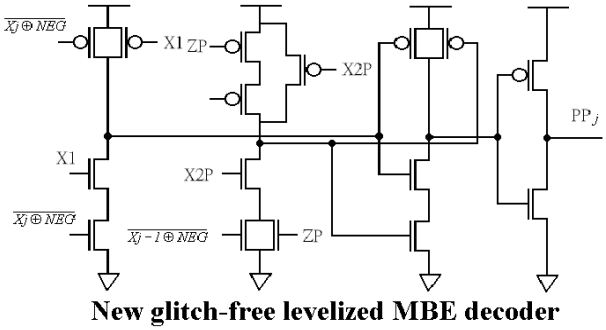


Figure 4 The new MBE decoder in transistor level.

3 Pipelined Booth Multiplier

An improved 8-bit by 8-bit high speed pipelined Booth multiplier is proposed in Figure 5. In a pipelined Booth multiplier, the maximum operating frequency is limited by the slowest stage which has the longest delay time. In order to get the correct and stable output results in each stage, we define the maximum secure clock period as follows:

Tmax=(Tmaxre,Tmaxdec,Tmaxfa) + Tmaxdff… (2)

Tmax may be a little larger than the period from input to output at each stage because we must ensure all data are stable at each stage every clock period. In equation (2), Tmax implies the maximum time between T_{PLH} + T_R and T_{PHL} + T_F at each stage, re denotes MBE recoder, dec denotes MBE decoder, fa denotes full adder, and dff denotes D flip-flop. T_{PLH} defines the response time of the gate for a low to high output transition, while T_{PHL} refers to a high to low transition. T_F and T_R refer to the rise time and fall time, respectively.

It can be proved by [6], and Table 3 that MBE decoder is slowest stage in a pipelined Booth multiplier. In Figure 5, an improved high speed pipelined multiplier is implemented by the new levelized MBE decoder to reduce the delay time in the critical path. As a result, MBE decoder is never the bottleneck in a pipelined Booth multiplier, and it can also provides larger driving force to next stage to get a better power performance for whole system. With regard to high speed system, large driving force and fast rise/fall time can have a better guarantee to ensure correct data operation. Especially while clock frequency raises from 660 MHz to 1 GHz, we need an output signal from MBE decoder with large driving force to overcome the speed bottleneck of the full adder.

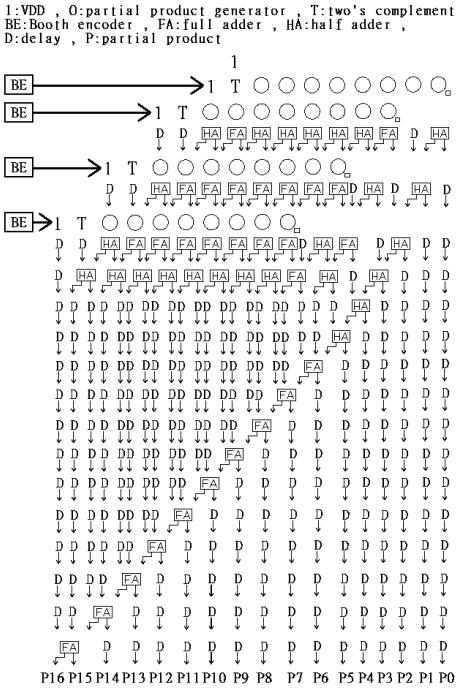


Figure 5 Architecture of the proposed high speed pipelined Booth multiplier.

4 Simulation Results

Transistor level simulation results are performed based on TSMC 0.35um process, 3.3V supply voltage, and 1GHz clock frequency by HSPICE. To find out the worst case, we suppose every simulated circuit stage with 0.1pF loading at the output.

Simulation waveforms and results are illustrated as follow: Figure 6 illustrate the comparison waveforms of traditional MBE decoder, traditional MBE decoder with 2 times/4 times size, and new MBE decoder. Table 2 presents the simulation results of new glitch-free MBE decoder in comparison with the glitch-free MBE decoder shown in Figure 1. Judging from these results, we can find out the speed bottleneck of a pipelined Booth multiplier is removed by our improved new MBE decoder. It is also noted that the new glitch-free MBE decoder, traditional MBE decoder with 2 times/4 times size, and new MBE decoder. Table 2 presents the simulation results of new glitch-free MBE decoder in comparison with the glitch-free MBE decoder shown in Figure 1. Judging from these results, we can find out the speed bottleneck of a pipelined Booth multiplier is removed by our improved new MBE decoder. It is also noted that the new glitch-free MBE decoder has a superior speed enhancement of 66.3%. If the size of the glitch-free MBE decoder [2] is increased as 2 times and 4 times, our new glitch-free MBE decoder is still superior with improvement of 46.5% and 20.0%, respectively. Furthermore, our new glitch-free

MBE decoder has a improvement of 50.4%, 42.0%, 43.6% in power delay product over the glitch-free MBE decoder proposed in [2] with standard size, 2 times size, and 4 times size, respectively.

Table 3 illustrates the comparison results of traditional MBE decoder, new MBE decoder, 14-T full adder implemented by 6-T CMOS XOR/XNOR circuit, 16-T transmission gate full adder, and new MBE recoder. In table 3, it is clearly that the traditional MBE decoder (Dec) will result in the speed bottleneck of about 500MHz in a pipelined Booth multiplier, and it can be removed by our new MBE decoder (New Dec). As a result, the speed bottleneck of about 930MHz is caused by the adopted 16t transmission gate full adder (TFA). To further raise the clock frequency to 1GHz, we need to support a faster input signal to drive both the full adder and the MBE recoder (MBER). In such high speed pipelined multiplier, our new MBE decoder can provides large driving force to drive Full adder in every partial product generation output to get a better performance for whole system in both speed and power respects.

Figure 7 demonstrates the partial output result of our improved high speed pipelined Booth multiplier simulated in 1GHz. Table 4 illustrates performance results of the improved high speed pipelined Booth multiplier. In the whole multiplier, the power dissipation includes the pulse clock generator and sign-extension part is 47.50mw in 330MHz, 69.53mw in 660MHz, and 100.52mw in 1GHz, respectively.

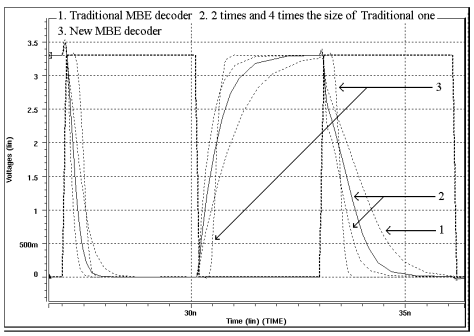


Figure 6 Comparison of traditional MBE decoder and proposed new decoder.

Table 2 Simulation results of new MBE decoder and Figure 1 MBE decoder [2]

	Dec	Dec*2	Dec*4	New Dec
TN	12	12	12	16
Area	25.2	50.4	100.8	26.6
Size	2.10	4.20	8.40	1.66
Tmax	2.02ns	1.27ns	0.85ns	0.68ns
Improve	66.3%	46.5%	20.0%	
Fmax	495Mhz	787Mhz	1176Mhz	1471Mhz
Power	0.121mw	0.167mw	0.257mw	0.181mw
PDP	0.244	0.212	0.218	0.123
Improve	50.4%	42.0%	43.6%	

Table 3 Comparison results of each pipelined stage

	Dec	New Dec	14TFA	TFA	MBER
TN	12	16	14	16	12
Area	25.2	26.6	28.8	30.8	24.0
Size	2.1	1.67	2.06	1.93	2.00
Tmax	2.02ns	0.68ns	1.27ns	1.08ns	1.06ns
Fmax	495Mhz	1471Mhz	787Mhz	926Mhz	943Mhz
Power	0.121mw	0.181mw	0.318mw	0.328mw	0.261mw

*Simulation with 0.2ns rise/fall time at 330MHz

CLK and X0 to X7 output signal

Figure 7 Partial result of proposed high speed pipelined Booth multiplier at 3.3V, 1GHz.

Table 4 Summary of performance results

Process	TSMC 0.35um		
Supply Voltage	3.3V		
Transistor count	4812		
Operating Frequency	330Hz	660MHz	1GHz
Average Power	47.50mw	69.53mw	100.52mw

5 Conclusion

In this paper, a new MBE (modified Booth encoding) recoder, and a new MBE decoder are proposed in CMOS transistor level to improve the performance of traditional multipliers. A low voltage, high speed pipelined modified Booth multiplier architecture is also presented in 3.3V, 1 GHz. The proposed pipelined Booth multiplier can reduce the delay time of the critical path by levelizing the complex gate in the MBE decoder to overcome the speed bottleneck of pipelined booth multiplier, and the speed improvement is up to 66.3 percent. Besides, an 8-bit by 8-bit glitch-free Booth multiplier is pipelined as a traditional pipelined array multiplier without any bottleneck in the MBE encoder and decoder, but with better performance in both power and speed. In TSMC 0.35um process, the complete multiplier circuit overcomes the speed bottleneck of about 500 MHz and instead it can operate at 3.3V, up to 1GHz with 100.52mw power only.

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