Simulation Models for Photogate Active Pixel Sensor

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Abstract: - The constant reduction in the transistors sizes for the design and the integration of smart sensors on chip requires accurate simulations of electrical characteristics. To this end, new simulation models of photogate active pixel sensor for CMOS imagers are proposed. A preliminary study describes the existing simulation techniques and shows their inaccuracy. Also, from the analysis of the charges transfer and of the photons carriers generation mechanisms in a photogate, two new simulation models are proposed, namely a functional model and a theoretical one. These models, described in Verilog-A language in the CADENCE environment design tool, offer a compromise between precise calculation and simulation time.

Key-Words: - Photogate Active Pixel Sensor, Optoelectronic Devices, Modelling and Simulation

1 Introduction

In the early 1990s, monolithic pixel sensors were proposed as a viable alternative to charge-coupled devices (CCDs) in visible imaging. These sensors are made in standard VLSI technologies, usually CMOS, and called CMOS imagers. Two main families of sensors are distinguished, i.e., the passive pixel sensor (PPS) and the active pixel sensor (APS) [1]. In the former, a photodiode is integrated in a pixel together with a selection switch, which connects the photodiode directly to the output line for readout. In the latter, an amplifier located in each pixel buffers the charge signal coming from the photosite. Today, due to APS structure, most CMOS imagers have better performances, low cost, low power consumption and smart sensors.

	Conversion Gain ($\mu V/e^-$)	Readout Noise (e^-)	S/N (dB)	Fill Factor (%)
CCD	4	16	75	100
PD PPS	48	300	62	70-80
PD APS	2-5	75-100	54	70
PG APS	11	10-15	74	50

Table 1. Performances of some pixel sensors

Table 1 summarises the main characteristics of sensors families [2], where PD indicates the photodiode and PG the photogate [3-4]. It is known that the conversion gain value is inversely proportional to the collection capacitance value of the pixel. In the case of PD PPS, this capacitance depends essentially of the photosite sizes. In addition for PD and PG APS, we must also consider the gate capacitance of the source follower (local amplifier). The read noise is composed by three main noise sources: KTC noise due to reset, shot noise due to leakage current and transistor noise (thermal and 1/f) [5]. KTC noise, which is directly proportional to the storage capacitance, is generally larger than all others noise sources. However, in the case of PG APS, KTC noise is reduced since the photocell is isolated from the source follower by a transfer transistor. Fill factor which is the ratio (in %) of the photosite area versus pixel area is of course smaller for PG APS since this pixel is composed of 4 transistors (4T cell), compared to 3T cell for PD APS. In conclusion, Table 1 indicates us that PG sensors have good performances compared to others CMOS solutions, for instance in terms of high conversion gain and low readout noise.

Then, our research will be orientated on PG APS design to develop CMOS imager. In the SoC design context, efficient smart sensors development need accurate and reliable simulation models. So, this paper will focus on the definition of three different levels for PG APS model, all of them being of different complexities. Fig.1 presents these three levels of simulation models. The functional model (level 1, section 3) simulates exclusively the behaviour of a PG APS. Level 2 corresponds to a theoretical model that considers equations from solid-state physics. This model is developed in section 4. Finally, a 3rd level of model could be an improvement of level 2 where sensitive parameters values are fitted with measures extracted from silicon. Sensitive parameters are essentially

technology characteristics such as doping, mobility, oxide thickness, passivation layer, Bayer filters, micro lens, etc. This article develops models 1 and 2.

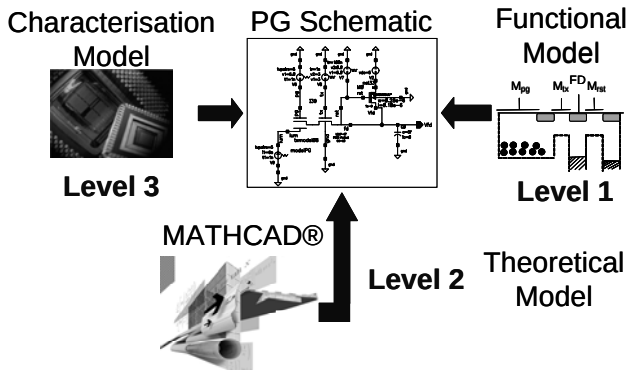

Fig.1: Three model levels for PG APS

This paper is organised as follows: section 2 introduces the PG architecture and operation modes, section 3 indicates conventional techniques for PG electrical simulations and describes a new functional model (level 1). Section 4 develops the PG theoretical model (level 2) and provides some simulations results. Conclusion is given in section 5.

2 Photogate Active Pixel Sensor

As illustrated in Fig.2, a PG APS is composed by five transistors (4T cell + photosite). The collection capacitance C_{pg} is located under the gate of M_{pg}. The M_{tx} transfer transistor acts like an anti-blooming for the exceeding charges. Before each transfer, the transistor M_{rst} initialises the floating node FD that realises the current-voltage conversion of the charges generated by photons. M_{sf} is the input transistor of the source follower and M_{sl} is an address line switch.

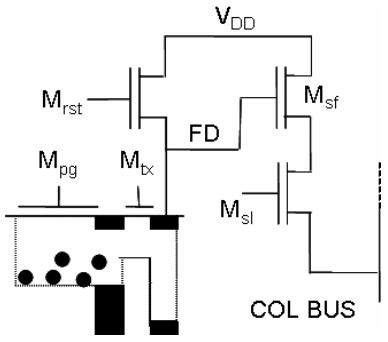

Fig.2: Equivalent schematic of a PG APS

The image sensor operations are illustrated in Fig.3 [6]. V_{DD} is fixed at 3.3V and the M_{tx} transfer gate is biased around $V_{DD}/2$. During accumulation time (Fig.3a), the photons collection is carried out by the accumulation of the charges under M_{pg} gate maintained at a constant potential (e.g. V_{DD}). The gate of the M_{rst} reset transistor is set to 0V to act like a barrier of potential. For an active reset ($M_{rst} = V_{DD}$), the potential well of the floating node FD is emptied (Fig.3b). Then, transistor M_{rst} is biased to 0V and the M_{pg} transistor gate is supplied to 0V to empty the collection capacitance under the PG (Fig.3c). Thus, charges transferred decrease the storage capacitance voltage at node FD. Finally, the M_{pg} transistor gate is biased to V_{DD} for a new acquisition cycle and when the line-column selection transistors are switched, the signal is transferred by the source follower (Fig.3d). With this pixel, charges are maintained in the substrate during their transfer and the advantage is a weak charge loss [1].

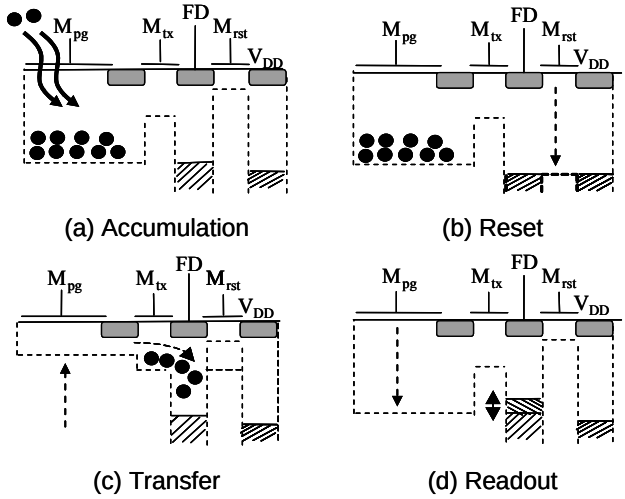

Fig.3: Four steps reading cycle of a PG APS

3 Electrical Simulations of PG APS

Three equivalent schematics models are traditionally used to simulate PG APS [7], but in fact none of them are really satisfactory. In the following we proposed an overview of these techniques and the description of a new functional simulation model.

3.1 Conventional electrical simulation models

Conventional proposals [7-8] consider various equivalent electrical models for the M_{pg} photogate transistor while others transistors M_{tx} and M_{rst} are simulated with conventional MM9 Spice electrical models [9].

In a 1st technique, transistor M_{pg} is instantiated as an open drain transistor and the photonic effect is modelised with a constant current source I_{ph}. Most often, electrical simulations with this model are not successful since transistor M_{pg} has its drain unconnected to any voltage and is considered as a floating node. This prevents from the simulation to succeed. In a 2nd model, transistor M_{pg} has its drain and source nodes connected together and the photonic effect is modelised by the same way as with technique 1. However, transistor M_{pg} is considered as a collection capacitance which value

depends on the drain and source electrostatic potentials. So clearly, results obtained by simulation do not modelise perfectly the photonic effects since the capacitance value varies with integration time. With a 3rd technique, transistor M_{pg} is modelised with a simple capacitance of constant value; i.e. 50pF. As with previous solutions, the photonic effect is instantiated with a constant current source. With this model, since transistor M_{pg} is equivalent to a constant collection capacitance, results obtained by simulation does not consider variations of the M_{pg} gate voltage transistor. Obviously, this voltage affects the photonic transfer in the pixel.

For solutions 2 and 3, another problem concerns the M_{tx} transfer transistor operation which cannot be correctly modelised with MM9 model. In fact, due to floating electrostatic potentials on the drain-source nodes, this transistor operates in a non-conventional mode. Clearly, these techniques are not satisfactory enough.

3.2 PG functional simulation model

A more accurate model for PG APS should result from a sound comprehension of solid-state physics of this component. Then, any set of theoretical equations may constitute a theoretical model. As a 1st step, we can imagine the use of a simplified functional simulation model. As illustrated in Fig.4, such a model can be decomposed in a multi-parts equivalent schematic where transistor M_{rst} is simulated with MM9 model, while transistors M_{pg} and M_{tx} are modelised with theoretical and/or functional equations traduced in ad-hoc language. These functional equations describe the behaviour of the PG APS for the photons carriers generation process. So, a simplified calculation of the MOS capacitance for the charge/voltage conversion is used [10].

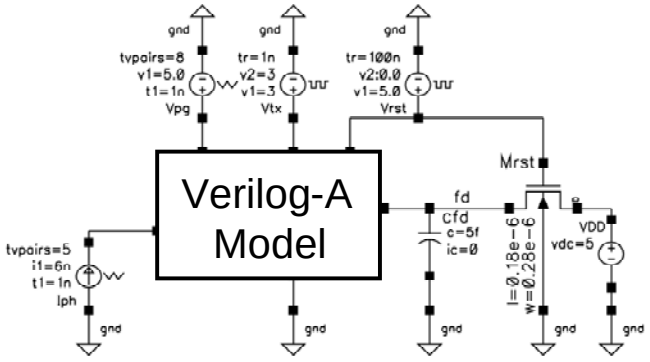

Fig.4: Functional model of a PG APS

In our context, we choose the Verilog-A language available in the CADENCE design tool environment [11] to define the PG APS behaviour; another choice like VHDL-AMS is also possible. Code written for this module is about 300 lines of Verilog-A language. Simulation results obtained with this new functional model are illustrated in Fig.5. For various switching values of V_{rst}, V_{pg} and I_{ph}, we can observe charges collection in C_{pg} and different integration slopes for V_{lum}. We can also note the effects of the charges transfer, of the charges overflow and of the light power on the output storage node FD.

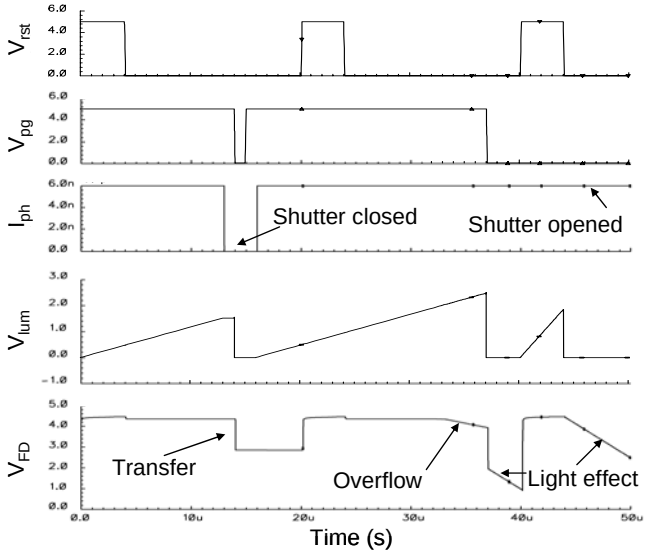

Fig.5: Simulation results of the PG functional model

From now on, we can highlight benefits of this new functional model versus the three conventional ones presented in section 3.1. Fig.6 shows simulation differences for a transient analysis up to 24 µs. Considering the same control signals V_{pg} and V_{rst} as in Fig.5, we observe: 1st - that integration slopes of V_{lum} for solutions 2 and 3 are different than one's of our model and then show different collection capacitances C_{pg} for the PG transistor, 2nd - charges transfer values when V_{pg} = 0V is wrong for solutions 2 and 3 (ΔV_{FDs3} = 2.53V and ΔV_{FDs2} = 2.73V) and should be equal to ΔV_{FD}= 1.52V as it corresponds to the maximal integration value of V_{lum} = 1.52V. Benefit of our new functional model is clear.

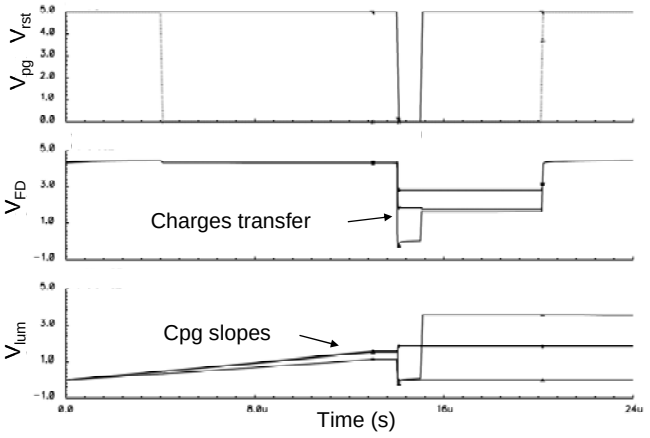

Fig.6: Comparison of simulation results for all PG models

4 PG theoretical simulation model

Section 3 describes the use of a PG APS functional model for simulation. As stated before, this model considers a set of simplified solid-state equations for the description of the PG APS behaviour. However, this equations set (or "background theory") can be more or less complex depending of the trade-off allowed between accuracy and simulation time. Less accuracy, as for the functional model allows simulation of thousands of pixels in a camera, whereas a detailed analysis of a simple pixel needs a deeper and longer simulation time. This latter case is developed in this section, both by the definition of this theoretical model and by an analysis of simulation results.

4.1 Description of the PG theoretical model

Basically, this level 2 model considers solid-state physics equations developed for the description of a MOS capacitance [10]. Fig.7 provides a simplified cut view of a PG APS where can be observed the MOS capacitance under gate of PG transistor but also the M_{tx} charges transfer transistor and the M_{rst} reset transistor. Drain potential of M_{tx}, also node V_{FD}, is close to V_{DD} during the reset phase. Since the M_{tx} transistor gate, node V_{tx}, is biased at a fixed potential (e.g. $V_{DD}/2$), the initial source potential V_{lum} is then temporarily close to V_{tx} potential during the reset phase. Consequently, V_{lum} reset potential influences the collection capacitance value of the PG. So, we will study both the biasing and the calculation of this MOS capacitance as well as the role of V_{lum} reset potential.

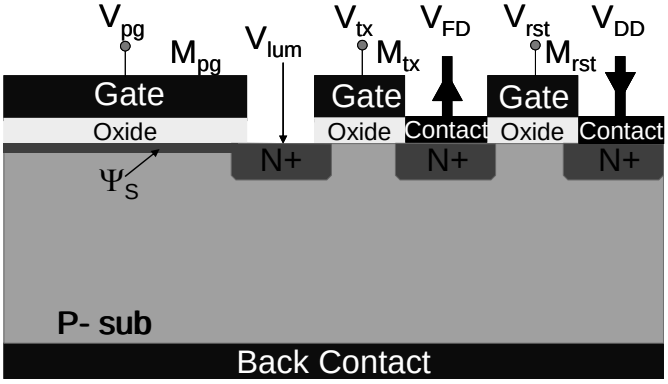

Fig.7: Cut view of a PG and internal potentials

As described in numerous books [10], the main operating regions for a MOS capacitance are (assuming 1st that $V_{lum} = 0$):

1- for $V_{pg} < V_{fb}$ (flat band voltage) system is in accumulation mode,

2- for $V_{fb} < V_{pg} < V_{th}$ (threshold voltage) system is in desertion mode

3- for $V_{th} < V_{pg}$ system is in inversion mode.

The PG channel charge, noted Q_{INV} inversion charge, depends directly of the V_{pg} gate potential but also of the MOS surface potential Ψ_S and of the Fermi levels gap between materials. However, the surface potential Ψ_S is also dependent of the gate voltage V_{pg} and Poisson equation must be solved to know the complete charge in the semiconductor Q_{SC} and the charge in the depleted layer Q_D.

Starting with Poisson equation:

$$\frac{\partial E}{\partial y}(x,y) = \frac{\rho(x,y)}{\varepsilon} \tag{1}$$

and the expression of the volume charges density:

$$\rho = q \cdot \left[p(x,y) - n(x,y) + ND(x,y) - NA(x,y) \right] \tag{2}$$

$$\rho = q\left\{ p_0 \cdot \exp\left[-\frac{q}{kT}\Psi(y) \right] - n_0 \cdot \exp\left[\frac{q}{kT}\left(\Psi(y) - V_{lum}\right) \right] + n_0 - p_0 \right\} \tag{3}$$

Then, equation (1) becomes:

$$\frac{d^2\Psi}{dy^2} = -\frac{\rho}{\varepsilon} = -\frac{q \cdot p_0}{\varepsilon}\left\{ -\frac{n_0}{p_0} \cdot \left(\exp\left[\beta\Psi(y) - V_{lum}\right] - 1\right) - \exp\left[-\beta\Psi(y)\right] - 1\right) \right\} \tag{4}$$

Since $\frac{d^2\Psi}{dy^2} = \frac{1}{2} d\left(\frac{d\Psi}{dy}\right)^2$, (4) becomes equal to:

$$\left(\frac{d\Psi}{dy}\right)^2 = 2\frac{q \cdot p_0}{\beta\varepsilon_{Si}}\left\{ \frac{n_0}{p_0} \cdot \left(\exp\left[\beta\Psi(y) - \beta V_{lum}\right] - \beta\Psi(y) - \exp\left[-\beta V_{lum}\right]\right) + \ldots \right\}$$
$$\left\{ \ldots - 1 + \exp\left[-\beta\Psi(y)\right] + \beta\Psi(y) \right\} \tag{5}$$

Assuming the law $\left.\frac{d\Psi}{dy}\right)_S = \frac{Q_{SC}}{\varepsilon_{Si}}$ between Q_{SC} charge and Ψ_S surface potential , we obtain the expression for Q_{SC}:

$$Q_{SC} = \pm\sqrt{2kT\varepsilon_{Si}p_0}\sqrt{\frac{n_0}{p_0} \cdot \left(\exp\left[\beta\Psi_S - \beta V_{lum}\right] - \beta\Psi_S - \exp\left[\beta V_{lum}\right]\right) + \ldots}$$
$$\sqrt{\ldots - 1 + \exp\left[-\beta\Psi_S\right] + \beta\Psi_S} \tag{6}$$

Using the same process for determining the charge Q_D in the depletion layer, that is neglecting charge in the inversion layer, we obtain:

$$\rho = q\left\{ p_0 \cdot \exp\left[-\beta\Psi(y)\right] + n_0 - p_0 \right\} = q \cdot p_0\left(\exp\left[-\beta\Psi(y)\right] - 1 + \frac{n_0}{p_0} \right) \tag{7}$$

$$\frac{d^2\Psi}{dy^2} = \frac{2kTp_0}{\varepsilon_{Si}}\left(\exp\left[-\beta\Psi\right] + \beta\Psi - \frac{n_0}{p_0}\beta\Psi - 1 \right) \tag{8}$$

$$Q_D = \sqrt{\frac{2kTp_0}{\varepsilon_{Si}}}\sqrt{\exp\left[-\beta\Psi_S\right] + \beta\Psi_S - \frac{n_0}{p_0}\beta\Psi_S - 1} \tag{9}$$

Combining equations (6) and (9), we obtain the final expression Q_{INV} of the charge in the inversion layer:

$$Q_{INV} = Q_{SC} - Q_D \tag{10}$$

This set of Equations 1-10 represents the core of the theoretical simulation model implemented for the PG. This set has been implemented both with MATHCAD tool [12] for debugging and in a 2nd step in Verilog-A language in CADENCE environment design tool.

4.2 Simulation results

Level 2 model allows the simulation of some important effects, such as V_{lum} initial voltage or photonic generation. They are discussed in the following.

4.2.1 Effect of V_{lum} on collection capacitance value

In a conventional MOS transistor, a voltage difference between drain and source creates the channel

conduction. In our case, a PG can be seen as a MOS transistor without any source. So, the drain-source voltage of a PG is null and the surface channel voltage Ψ_S is constant all over the gate.

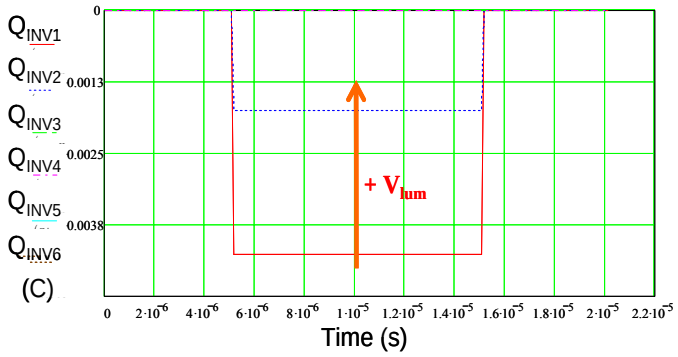

Fig.8: Effect of V_{lum} on Q_{INV} inversion charge

Fig.8 shows the inversion layer charge Q_{INV} for different values of V_{lum} initial reset voltage. As can be seen, the larger is the V_{lum} initial voltage, the smaller is $|Q_{INV}|$. This result originates from Q_{SC} semiconductor charge that decreases with V_{lum} (Eq.6), while Q_D remains constant (Eq.9). Then, with a MATHCAD iterative calculation process, we calculate the equivalent PG collection capacitance. This capacitance value depends essentially on W/L sizes of M_{pg} transistor but also of the gate-bulk voltage V_{pg}. Fig.9 illustrates this PG collection capacitance and its various operating modes. Effect of V_{lum} initial reset voltage on this capacitance is represented where a positive value for V_{lum} shifts the beginning of the strong inversion region. For instance, with V_{pg} = 0.5V we move from the strong inversion mode (V_{lum} = 0V) towards the weak inversion region (V_{lum} = 1V).

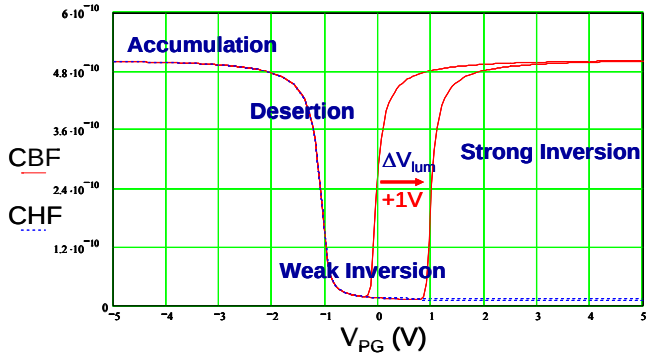

Fig.9: Effect of V_{lum} on collection capacitance value

4.2.2 Effect of light power Po on V_{lum}

To complete the previous set of Equations 1-10, it's mandatory to modelise the photons carriers generation process in the substrate. Assuming an ambient light of power Po and wavelength λ_C, an expression for the photonic generation rate is given by [10]:

$$G_{OPT}(XD, Po) = -\frac{\lambda_C}{h \cdot c} \cdot \alpha \cdot \exp(-XD \cdot \alpha) \cdot Po \qquad (11)$$

where α is the substrate absorption coefficient, h the Plank constant and c the light velocity. In this expression, XD is the width of the depletion layer that is the thin substrate region where photons carriers charge generation occurs.

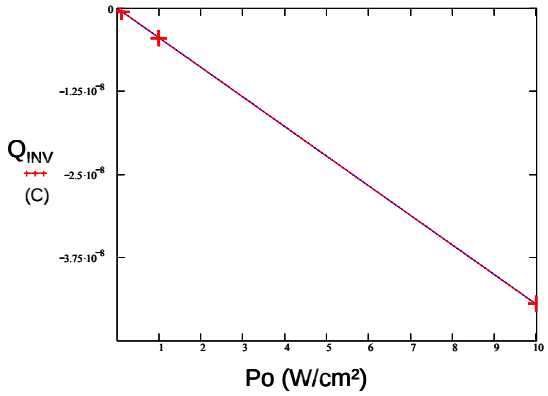

Fig.10: Effect of Po light power on Q_{INV}

Adding Eq.11 in calculations of Q_{INV}, we can show that variation of Q_{INV} is linear with Po, see Fig.10:

$$Q_{INV} = Q_{INVinit} + (-1.82 \cdot 10^{24}) \cdot Po \cdot XD \cdot \Delta t \cdot q \qquad (12)$$

where $Q_{INVinit}$ is the initial channel charge in the inversion layer under PG, q the electron charge and Δt the integration time. In addition, assuming that Δt and XD are constant, we obtain:

$$Q_{INV} = A_0 \times Po + B_0 \qquad (13)$$

In our model simulation, for a standard PG technology, we obtain coefficients A_0 = -4.419e-09 and B_0 = -3.627e-20. So, charge Q_{INV} varies linearly with Po.

The next step is to determine the resulting value of V_{lum} after photonic charges accumulation. For the simulation, we consider a signal V_{pg} that rises from 0V to 3.3V at 5ns and decreases to 0V at 15ns. Also, the light power Po varies from 10nW/cm² to 10W/cm². The final V_{lum} voltage is measured at 16ns.

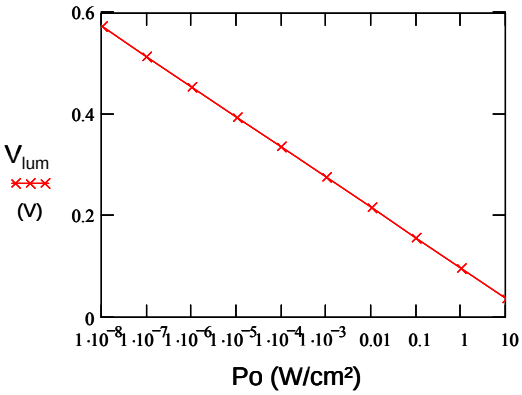

Fig.11: Logarithmic variation of V_{lum} with Po

Results of V_{lum} voltage in terms of Po are given in Fig.11. We observe that V_{lum} voltage is directly proportional to the logarithm of Po by:

$$V_{lum} = A_1 \times \log(B_1 \cdot Po^2 + C_1 \cdot Po) + D_1 \qquad (14)$$

Again, coefficients A_1, B_1, C_1 and D_1 depend on the technology parameters and are equal to A_1 = -0.059, B_1 = 2.24e-10, C_1 = 1.521e-04, D_1 = 0.132. Since coefficient B_1 is negligible compared to others, then neglecting this term, we obtain finally:

$$V_{lum} = A_2 \cdot \log(Po) + B_2 \qquad (15)$$

with A_2 = 0.059 and B_2 = 0.095 determined by simulation. Fig.12 shows the final voltages for V_{lum} , or output voltage of the pixel, according various light powers Po. We can observe that higher is the Po power, lower is the V_{lum} voltage.

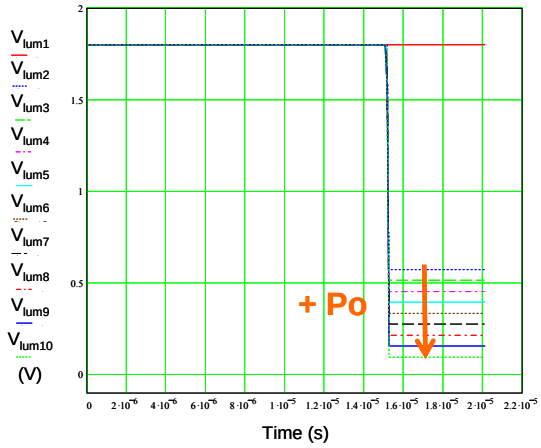

Fig.12: Variation of V_{lum} final voltages with Po

5 Conclusion

Accurate simulations of photogate pixel are necessary for smart sensors design. Usually, simulations for these pixels consider too simple models that show limits to describe the photons carriers generation mechanisms. Our proposal describes two new simulation models described in Verilog-A language in Cadence tool. The most significant improvement relates to the precise modelling of the PG collection capacitance and to the charges transfer. A first model (level 1) corresponds to a functional description of the charge transfer, of the charge overflow and of many other secondary effects. A second model (level 2) calculates the real charges under the PG and uses solid-state equations reporting the charges transfer. Simulation studies of the light power show that V_{lum} obeys to a logarithmic law and that the inversion charge Q_{INV} varies linearly. A 3rd level model is also suggested by correcting the level 2 model parameters values after silicon measures and technology characterisation. Chip fabrication is also undergoing. In conclusion, accuracy of these new PG simulation models has been demonstrated and shows their interests for the design of CMOS imager.

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