Universal Conveyor – novel active device suitable for analog signal processing

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Abstract: - Universal Conveyor (UC) is presented as a generally usable active device in analog signal processing. It substitutes all kinds of classical current and voltage conveyors.

Key-Words: - current conveyor, voltage conveyor, universal conveyor, analog signal processing

1 Introduction

Since the 1960's 3 generations of current conveyors (CCs) have been defined by Sedra, Smith and Fabre. In the 1990's the evolution headed towards CCs equipped with either a differential Y port or multiple Y ports [1, 2]. This led to the definition of 8-port Universal Current Conveyor (UCC) [3], which is a versatile building block replacing previously specified CCs. The UCC device is of CCII origin and it has 3 input Y ports and 4 output Z ports. Its universality is based on the direct connection between a Y port and a Z port and thus it simulates the first- and third-generation CCs (CCI, CCIII). No extra ports in the UCC structure are needed.

Voltage conveyors (VCs) are counterparts to CCs [4]. Again, 3 generations of VC can be determined. The CDBA device is of the DCVC+ type [5]. In current-mode analog signal processing, the development of VCs required a new active element to have currents as both the input and the output quantities. The CDTA device [6] is not a genuine conveyor, because it contains a transconductance element (BOTA). Similarly to the UCC definition, the Universal Voltage Conveyor (UVC) [7, 8] was designed to supersede all known types of VCs. Unlike the UCC device, UVC needs a single or double auxiliary voltage port to support voltage sources in Y ports.

2 Universal Conveyor Definition

A major function of the novel Universal Conveyor is to substitute all 24 kinds of the CC and the VC. Moreover it replaces the types of CCs and VCs with differential input port (DVCC, DCVC) and those with differential output port (CC+/–, VC+/–). The UC symbol is depicted in Fig. 1. Two versions of UC are available – the 9-port named UC9 and the 13-port UC13. The more extensive version has a differential current output port and a differential voltage input port doubled.

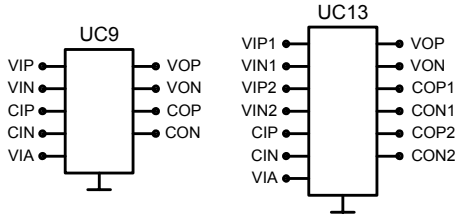

Fig. 1: Symbols of the UC device

Both variants of the UC device are equipped with these ports:

- VIP - voltage input positive,
- VIN - voltage input negative,
- CIP - current input positive,
- CIN - current input negative,
- VOP - voltage output positive,
- VON - voltage output negative,
- COP - current output positive,
- CON - current output negative,
- VIA - auxiliary voltage input port.

The VIP, VIN, COP, and CON ports of the UC9 device are doubled and thus the UC13 device is proposed. Duplications of the voltage input ports and the current output ports are necessary for extending the universality of the UC device.

The ideal transfer equations valid for the UC13 device are as follows:

$$
\begin{aligned}
&V_{\mathrm{CIP}} = a_1 V_{\mathrm{VIP1}} + a_2 V_{\mathrm{VIN1}} + a_3 V_{\mathrm{VIP2}} + a_4 V_{\mathrm{VIN2}} = \\
&= V_{\mathrm{CIN}},\ a_1 = +1,\ a_2 = -1,\ a_3 = +1,\ a_4 = -1, \\
&I_{\mathrm{COP1}} = -I_{\mathrm{CON1}} = I_{\mathrm{COP2}} = -I_{\mathrm{CON2}} = \\
&= b_1 I_{\mathrm{CIP}} + b_2 I_{\mathrm{CIN}},\ b_1 = +1,\ b_2 = -1, \\
&V_{\mathrm{VOP}} = d_1 V_{\mathrm{VIA}},\ V_{\mathrm{VON}} = d_2 V_{\mathrm{VIA}}, \\
&d_1 = +1,\ d_2 = -1.
\end{aligned}
\tag{1}
$$

In the case of UC9, $a_3 = 0$, $a_4 = 0$, $I_{\mathrm{COP2}} = -I_{\mathrm{CON2}} = 0$.

The universality of the UC device resides in the presence of the basic analog signal processes: voltage addition/subtraction: VIP, VIN → CIP, CIN, current addition/subtraction: CIP, CIN → COP, CON, voltage distribution: VIA → VOP, VON, current distribution: CIP, CIN → COP, CON.

3 Universal Conveyor Utilization

Table 1 shows how UC13 can be utilized.

Conveyor	pin relations	grounded
	connected	open
any CC except UCC	Z+ → COP(N)1{2} Z– → CON(P)1{2} X → CIP(N)	VIA
	-	CIN(P), VOP, VON
CCI+/–	Y → VIP1[2]	VIN1,2, VIP2[1], CON(P)2{1}
	VIP1[2] – COP(N)2{1}	-
ICCI+/–	Y → VIN1[2]	VIP1,2, VIN2[1], CON(P)2{1}
	VIN1[2] – COP(N)2{1}	-
CCII+/–	Y → VIP1[2]	VIN1,2, VIP2[1], COP2{1}, CON2{1}
	-	-
ICCII+/–	Y → VIN1[2]	VIP1,2, VIN2[1], COP2{1}, CON2{1}
	-	-
CCIII+/–	Y → VIP1[2]	VIN1,2, VIP2[1], COP(N)2{1}
	VIP1[2] – CON(P)2{1}	-
ICCIII+/–	Y → VIN1[2]	VIP1,2, VIN2[1], COP(N)2{1}
	VIN1[2] – CON(P)2{1}	-
DVCC+/–	Y+ → VIP1[2] Y– → VIN1[2]	VIP2[1], VIN2[1], COP2{1}, CON2{1}
	-	-
UCC	Z1+ → COP(N)1, Z1– → CON(P)1, Z2+ → COP(N)2, Z2– → CON(P)2, Y1+ → VIP1, Y3+ → VIP2, Y2– → VIN1[2], X → CIP(N)	VIN2[1], VIA
	-	CIN(P), VOP, VON
Any VC including UVC	Z+ → VOP, Z– → VON, X → COP(N)1{2}	COP(N)2{1}, CON(P)1{2},2{1}
	VIA → COP(N)1{2}	-
VCI+/–	Y → CIP	VIP2[1], VIN1,2
	VIP1[2] – COP(N)1{2}	CIN
IVCI+/–	Y → CIN	VIP2[1], VIN1,2
	VIP1[2] – COP(N)1{2}	CIP
VCII+/–	Y → CIP	VIP1,2, VIN1,2
	-	CIN
IVCII+/–	Y → CIN	VIP1,2, VIN1,2
	-	CIP
VCIII+/–	Y → CIP	VIN2[1], VIP1,2
	VIN1[2] – COP(N)1{2}	CIN
IVCIII+/–	Y → CIN	VIN2[1], VIP1,2
	VIN1[2] – COP(N)1{2}	CIP
DCVC+/–	Y+ → CIP, Y– → CIN	VIP1,2, VIN1,2
	-	-
UVC	Y+ → CIP, Y– → CIN, VP → VIP1[2], VN → VIN1[2],	VIP2[1], VIN2[1]
	-	-

Table 1: The utilization of the UC13 device

The user must connect some pins and leave others unconnected. Original pins of replaced CCs and VCs correspond to those of the UC (indicated by arrows). Three independent variant levels - (), [], {} - are depicted in Table 1 to show the variability in the usage of the UC device.

4 Linear Symbolic Simulations

Fig. 2 displays the block diagram of the UC9 device. Practical linear properties - transfer functions and immittances are included in the 1st-level model.

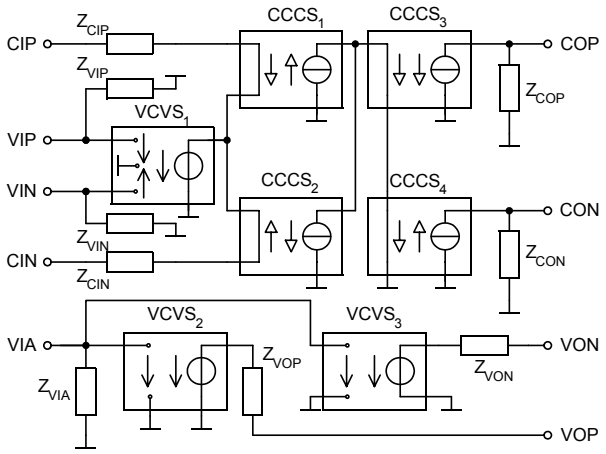

Fig. 2: Linear block diagram of the UC9 device

The whole detailed structure of the UC9 device is illustrated in Fig. 3.

The basic building block of the proposed UC devices is the Voltage-Controlled Voltage Source (VCVS) with OTAs modified from [9]. Its structure is shown in Fig. 4.

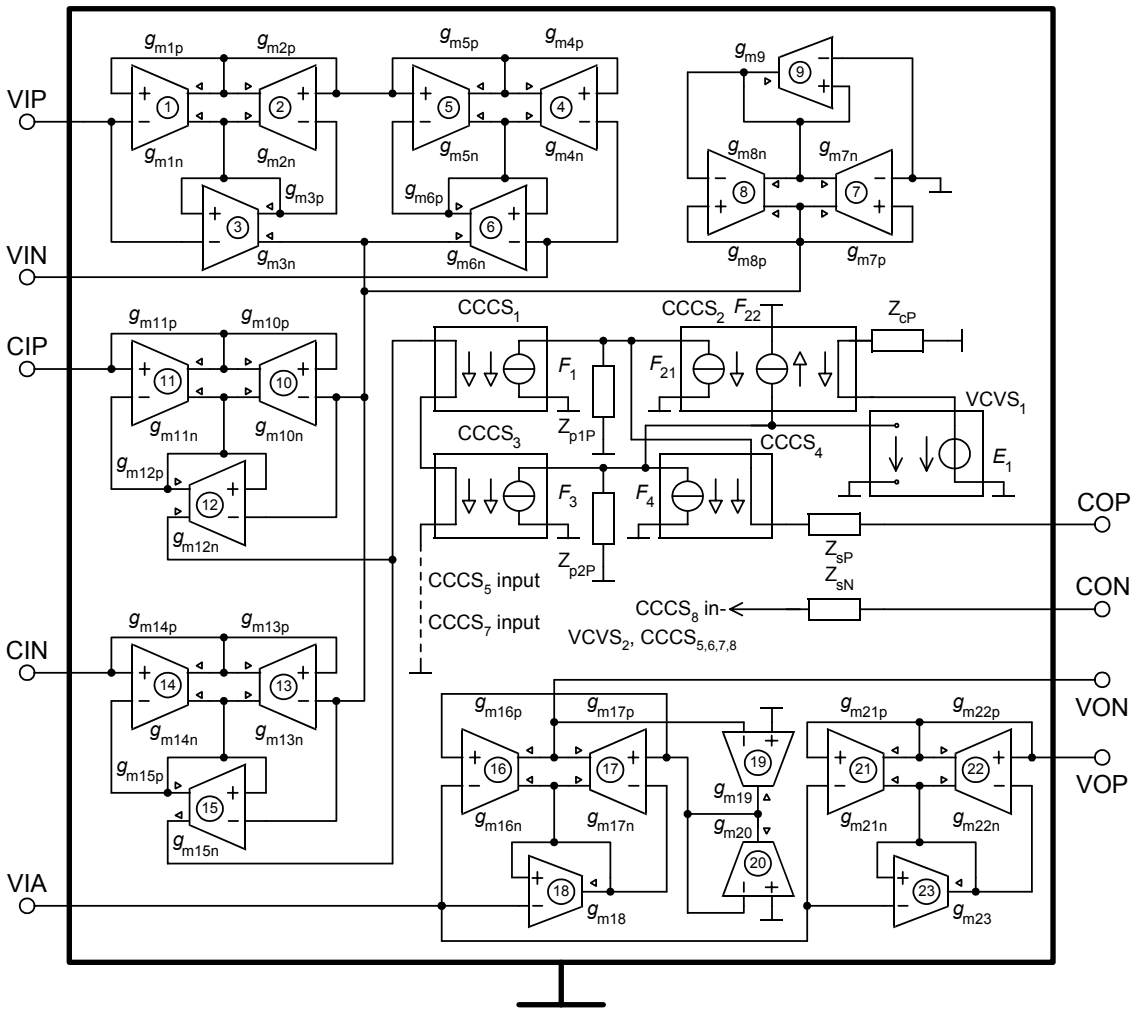

Fig. 3: Block diagram of the 9-port Universal Conveyor

The CMOS implementation of the VCVS in Fig. 4 assumes $g_{m1p} = g_{m1n}$ and $g_{m2p} = g_{m2n}$.

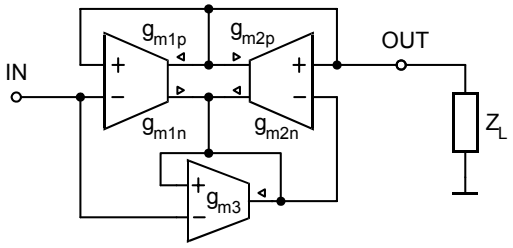

Fig. 4: VCVS employing three OTAs

The voltage transfer function of the single-input single-output voltage follower is in the form:

$$K_V = 1 + \frac{g_{m3} - g_{m2n}}{\left\{\begin{array}{l}\left(g_{m3} - g_{m2n}\right)\left(Z_L g_{m1p} - 1\right) + \\ + Z_L g_{m2p}\left(g_{m1n} + g_{m3}\right)\end{array}\right\}}. \quad (2)$$

The output impedance of the VCVS plotted in Fig. 4 is as follows:

$$Z_{OUT} = \frac{g_{m2n} - g_{m3}}{g_{m1p}\left(g_{m3} - g_{m2n}\right) + g_{m2p}\left(g_{m1n} + g_{m3}\right)}. \quad (3)$$

If we meet the conditions $g_{m3} = g_{m2n}$ and $g_{m1p(n)} >> g_{m2p(n)}$, then we reach the ideal state with frequency-independent $K_V = +1$ and $Z_{OUT} = 0\ \Omega$. In a practical implementation using the AMIS CMOS 0.35 μm technology we must ensure $g_{m3} > g_{m2n}$ to get $Z_{OUT} > 0\ \Omega$ due to the feedback stability of the VCVS used.

For example, if $g_{m2p} = g_{m2n} = 1.02$ mS, $g_{m3} = 1.00$ mS, $g_{m1p} = g_{m1n} = 10.0$ mS, and $Z_L = 1$ kΩ then DC and low-frequency $Z_{OUT} = 1.815\ \Omega$ and $K_V = 1.00175$ [-]. In the UC9 structure in Fig. 3 we suggest $g_{m10p(n)} = g_{m14p(n)} = g_{m16p(n)} = g_{m21p(n)} = = 10$ mS, $g_{m11p(n)} = g_{m13p(n)} = g_{m17p(n)} = g_{m22p(n)} = 1.02$ mS, $g_{m12p(n)} = g_{m15p(n)} = g_{m18p(n)} = g_{m19p(n)} = g_{m20p(n)} = g_{m23p(n)} = 1.00$ mS. OTAs No. 1-6 comprise

differential voltage buffer summating currents flowing through voltage sources with output impedances of 1 kΩ into a common active impedance of 1 kΩ made from OTAs No. 7-9. Other transconductance parameters are: $g_{m1p(n)} = g_{m4p(n)} = g_{m7p(n)} = 1$ mS, $g_{m2p(n)} = g_{m5p(n)} = g_{m8p(n)} = 2$ mS, $g_{m3p(n)} = g_{m6p(n)} = g_{m9p(n)} = 500$ μS.

The voltage follower (VF) at the CIN pin is of the same structure as the VF at the CIP pin. The high output impedance CCCS with improved frequency performance, which comprises subsidiary $CCCS_{1,2,3,4}$ and $VCVS_1$, is doubled as well ($CCCS_{5,6,7,8}$, $VCVS_2$), but with the negative transfer sign.

5 Numerical Results

Results of linear simulations of UC9 transfers and VCVS output impedance are shown in Figs. 5 to 7.

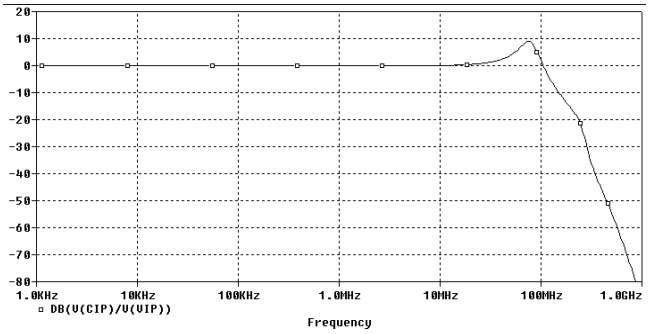

Fig. 5: Voltage frequency response VIP → CIP

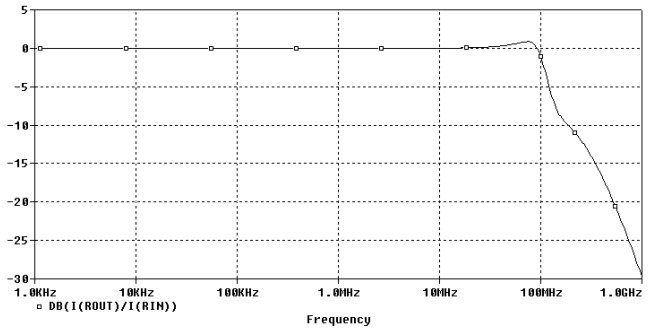

Fig. 6: Current frequency response CIP → COP

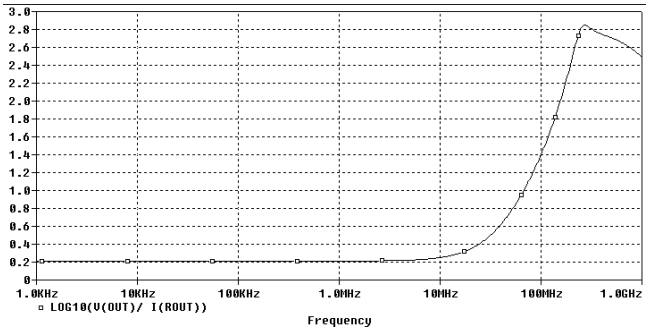

Fig. 7: VCVS output impedance (log scale)

6 Conclusion

Universal Conveyor was defined as a novel active device suitable for analog signal processing. Linear simulations indicate a usable bandwidth of 100 MHz.

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