Design of a CMOS on-chip high voltage generator

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Abstract: - In this paper, an original CMOS on-chip high voltage generator has been proposed. Having a hybrid charge pump structure, this high voltage generator benefits advantages of two charge pumps used and allows obtaining an output voltage that neither of the two charges pumps can reach individually. Simulation results show that an output voltage as high as 41V, which is inferior to the breakdown voltage of the 0.8µ CMOS process used.

Key-words: charge pump, CMOS, high voltage generator, on-chip high voltage generator, voltage multiplier

1 Introduction

The realization of a system on chip (SoC) sometimes needs a high voltage generator to control micro-actuators. In our application, a voltage as high as 40V is needed to control a micro-mirror. To offer such a high voltage, an off-chip generator is usually used. However, an on-chip generator is always preferred towards a real SoC.

Charge pump circuits can be used to realize on-chip high voltage generators. The most often used charge pump circuit is Dickson charge pump [1], because it is simple in structure. However, in Dickson charge pump, the voltage across each pump capacitor increases along the charge path towards its output. So, the maximum output voltage of Dickson charge pump will be limited by the breakdown voltage of the pump capacitor usually made up of poly1/poly2. This breakdown voltage is less than 40V for a 0.8µ CMOS process. Consequently, only Dickson charge pump cannot satisfy our design requirement.

Stacking charge pump [2] can also be used for on-chip high voltage generators. Unlike Dickson charge pump, the voltage across each pump capacitor is constant. More sensitive to parasitic capacitances than Dickson charge pump is, the stage number of stacking charge pump is preferred to be less than 3, which limits the maximum output voltage.

One solution is to use a hybrid charge pump. In the following, the architecture of the CMOS high voltage on-chip generator is given in next section, followed by the description of its operation in section 3. Some design considerations are discussed in section 4. Finally, simulation results are illustrated in section 5 followed by conclusion.

2 Architecture of the proposed on-chip high voltage generator

The architecture of the proposed CMOS on-chip high voltage generator is shown in figure 1. Combining Dickson charge pump and stacking charge pump, it has a hybrid structure. The clock signals Φ_1 and Φ_2 are out of phase. Dickson charge pump is simple in structure and less sensitive to parasitic capacitances compared to stacking charge pump, hence high in efficiency. This is why it is chosen as the first stage to produce an output voltage as high as possible. The maximum output voltage is limited by pump capacitor's breakdown voltage.

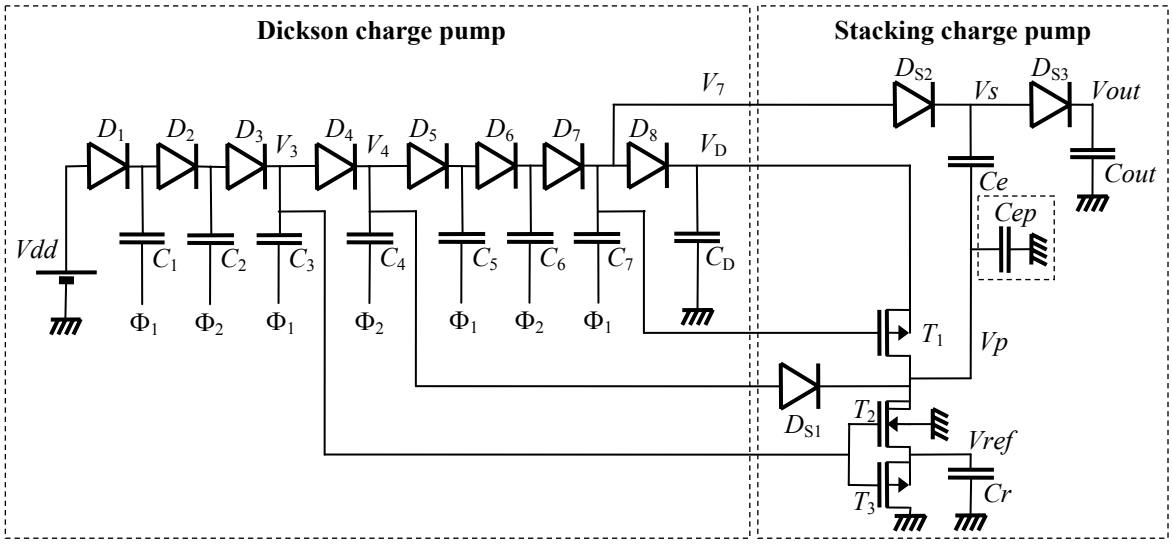
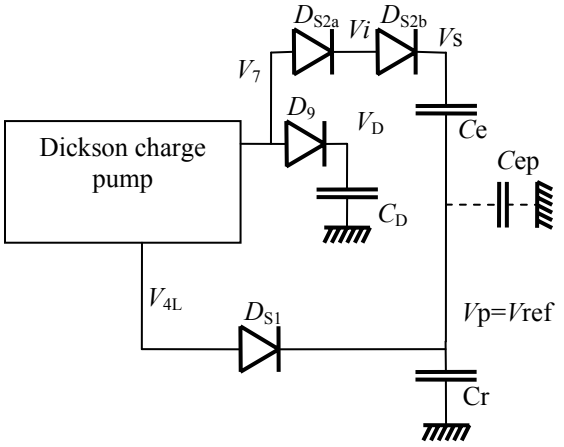
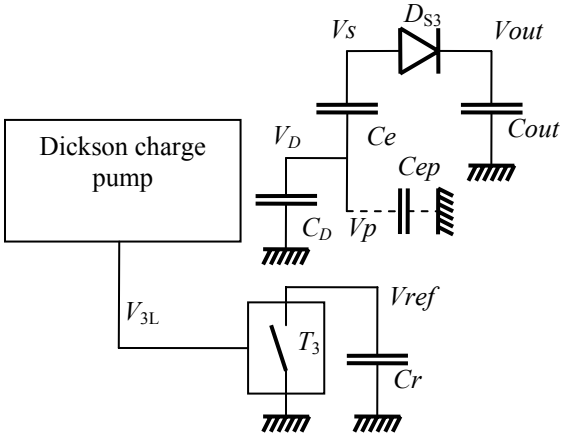


Figure 1. Architecture of the on-chip CMOS high voltage generator



(a) Φ_1 = '1' and Φ_2 = '0'



(b) Φ_1 = '0' and Φ_2 = '1'

Figure 2. Equivalent circuits corresponding to two operation phases

Having constant voltage across each pump capacitor, stacking charge pump is used as the second stage to complete the output voltage of Dickson charge pump to the required output voltage. Here only one stage is used so that the influence of parasitic capacitances can be reduced to minimum.

Two design points should be mentioned. First, the output stage of Dickson charge pump is shared with stacking charge pump. Therefore, with pump capacitors' number minimized, the hybrid charge pump is compact.

Second, stacking charge pump works in two phases: charging and stacking. In this one-stage stacking charge pump, two pump capacitors, C_D and Ce, are used. Diodes, D_{S1}, D_{S2} and D_{S3}, and transistors, T_1, T_2 and T_3, work as switches. By stacking the two pump capacitors already charged to desired voltages, we can obtain the required output voltage, as shown in figure 2 (b). V_D represents the maximum output voltage of Dickson charge pump. In order to charge Ce to desired remaining voltage ΔV, Cr is added. By adequately choosing Vref, the required remaining voltage can be obtained during charging phase, as shown figure 2 (a).

3 Operation of the proposed on-chip high voltage generator

The operation of Dickson charge pump is well known. Therefore, in the following we focus on the operation of the stacking charge pump proposed. To simplify the explanation, diodes and switches are considered as ideal ones. As mentioned above, the stacking charge pump works in two phases: charging phase and stacking phase.

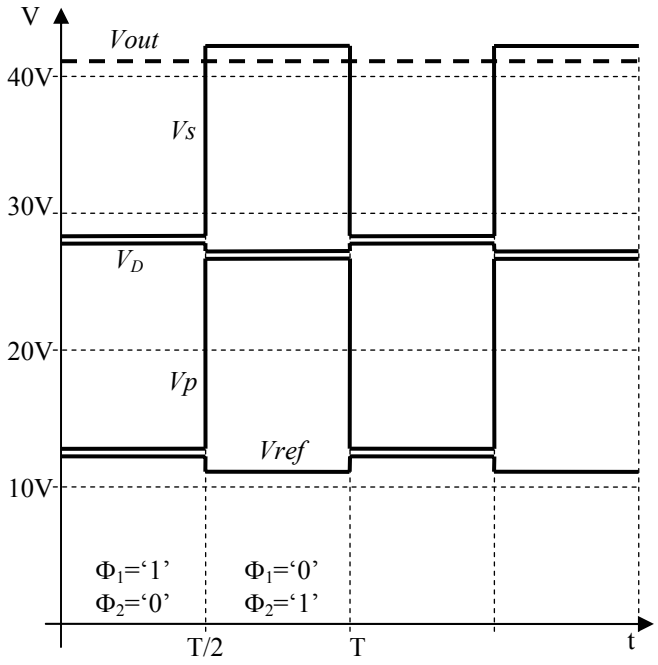


Figure 3. Chronograms of internal voltages *V*ref, *V*p, *V*s, *V*D and *V*out

During charging phase, Φ_1 = '1' and Φ_2 = '0'. The equivalent circuit is shown in figure 2 (a). Switch T_2 is closed and switches T_1 and T_3 are opened. Consequently, *C*e and *C*r are connected in series. Besides, D_9, D_{S1} and D_{S2} are conducting. As a result, *C*r is charged to V_4's low level, i.e. *V*ref = V_{4L}. Since *V*s = V_D and *V*p = *V*ref, *C*e is charge to $V_S - V\text{p} = V_D$ - *V*ref. *V*ref is chosen in such a way that V_D - *V*ref is equal to the required remaining voltage.

During stacking phase, Φ_1 = '0' and Φ_2 = '1'. The equivalent circuit is shown in figure 2 (b). With T_1 closed and T_2 opened, *C*e is stacked on C_D, resulting that *V*p > V_4 and *V*s > V_7. Consequently D_{S1} and D_{S2} are opened, and *V*out = *V*s = $V_D + \Delta V$.

It should be mentioned that T_3 is closed only during *V*ref > V_{3L}, i.e. V_3's low level. Once *V*ref = V_{3L}, T_3 is opened. During the charging phase of *C*e, as V_3 is in its high level and V_{3H} > *V*ref, which makes sure that T_2 is closed and *V*p = *V*ref. Then as long as *V*ref < V_{4L}, D_{S1} is closed and *C*r is charged until *V*ref = V_{4L}. The chronograms corresponding to different nodes are shown in figure 3.

4 Design consideration

In the following, the choice of diodes, pump capacitors, switches and stage number is discussed.

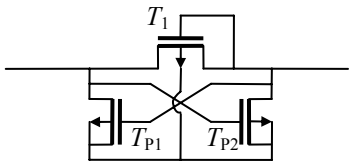


Figure 4. Diode realized by three transistors

4.1 Diodes

The simplest way to realize an integrated diode is to use a NMOS or a PMOS transistor with its gate and drain connected together. However, with a NMOS transistor, when its source voltage is greater than its bulk voltage, which is the case in both charge pumps, body effect will take place, which results in the increase of threshold voltage of NMOS transistor. Besides, with its bulk fixes to the ground, the breakdown voltages between source (drain) and bulk also limits the voltage across source/bulk and drain/bulk.

While with a PMOS transistor, as its N-well is biased to higher voltage between its source and drain, the problems met with NMOS transistor can be avoided. In fact, with a PMOS transistor-realized diode, it is the breakdown voltage between N-well and substrate that will limit the highest voltage beared by the diode and this breakdown voltage is much higher than that of *V*sb (*V*db).

To keep threshold voltage constant, a macro-diode is chosen [3]. In the macro-diode, three PMOS transistors are used, as shown in figure 4: one main transistor is connected like a diode and the other two auxiliary transistors bias the N-Well to the higher voltage between the source and the drain of the main transistor. However, different from the remaining diodes, the voltage across D_{S2} during stacking phase is more than 17V, which is superior to the breakdown voltage Vds, two diodes must be used to share the 17V to avoid the diode breakdown.

4.2 Pump capacitors

Different techniques can be used to realize an integrated capacitor. To have a good integration a capacitor made up of polysilicon plates is preferred. However, along with polysilicon capacitor, parasitic capacitance exists between bottom plate and substrate, as well as between top plate and substrate. As the parasitic capacitance between upper plate and substrate is much smaller than that between bottom plate and substrate, only the parasitic capacitance between bottom plate and substrate is taken into account, as shown in figure 5.

As we mentioned above, compared to Dickson charge pump,, the influence of parasitic capacitance in stacking charge pump cannot be neglected. *C*e's parasitic capacitance *C*ep, as shown in figure 2, is in parallel with C_D during stacking phase. Consequently, the charge stored on C_D will be redistributed between C_D and *C*ep, which lowers V_D, hence *V*s as well as *V*out. In order to reduce *C*ep's influence, *C*e should be chosen smaller than C_D because *C*ep is proportional to *C*e.

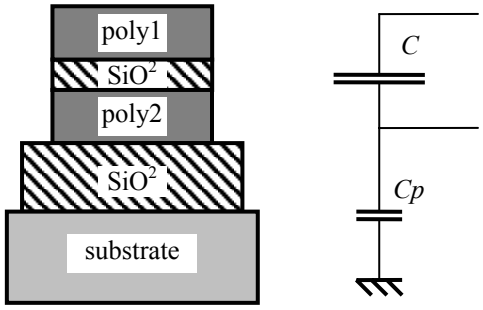


Figure 5. Section of integrated capacitor Poly1/Poly2 and its symbol with parasite capacitance

4.3 Switches

Since switches are all realized by transistors and in stacking stage high voltage must be beared, breakdown voltages of transistors must be respected. For T_2, as high voltage only appears at its drain side, a high voltages NMOS transistor HVNMOS can be used. Besides, *V*gb is kept less than breakdown voltage by design. Unlike T_2, T_1 must stand for high voltage at both source and drain sides. This is why a PMOS transistor is used so that with its source linked to its N-well, high voltage will only appear at its drain side. Their *V*ds and *V*gb is also kept within breakdown voltage by design.

4.4 Stage number

As Dickson charge pump is less sensitive to parasitic capacitances compared to stacking charge pump, it is designed to offer an output voltage as high as possible to have good efficiency. Limited by the breakdown voltage of polysilicon capacitor, the output voltage V_D of Dickson charge pump should be designed around 30V. According to $V_D = (N + 1)(V\text{dd} - V\text{th})$ where *V*th represents the threshold voltage of transistor, stage number *N* must be greater or equal to 6. However, there are two charge consuming sources: *C*ep and *C*r, which makes V_D lower than desired. Especially, the influence of Cep is equivalent to a resistive load. The same design as the resistive load [4] can be used. So *N* is chosen as 7.

TABLE I. PARAMETERS USED IN SIMULATION

Parameters	***Value***
Power supply	5V
Working frequency	10MHz
*C*out	10pF
*V*out	41V
V_D	27V
*C*ep / *C*e	20%

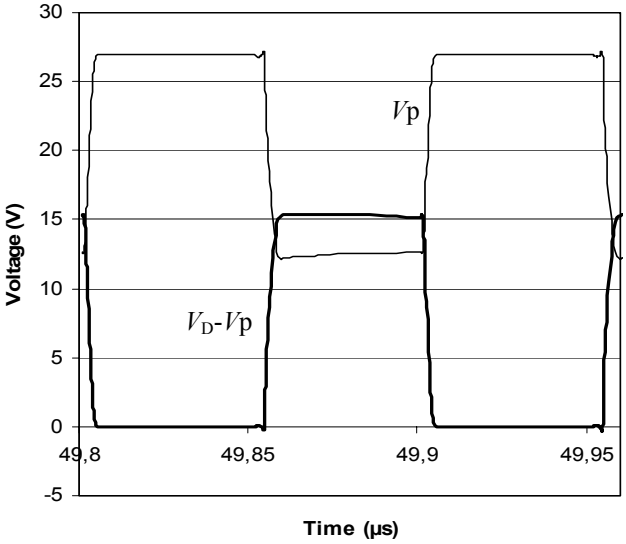


Figure 6. Simulations of internal signals

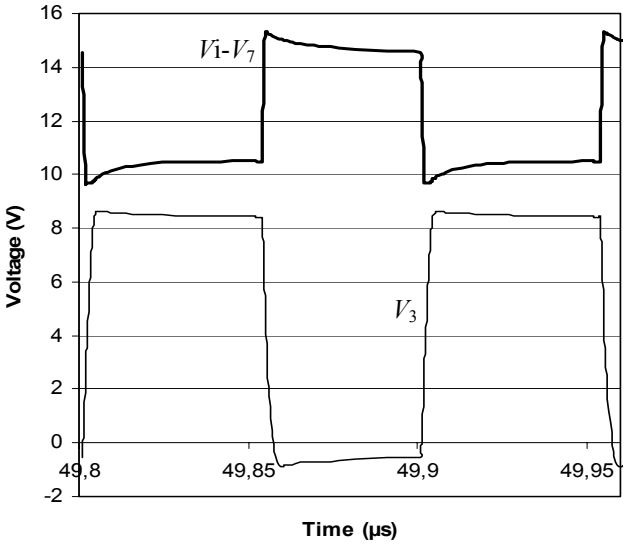


Figure 7. Simulations of internal signals

5 Simulation results and discussions

The proposed architecture is simulated with a 0.8µ CMOS process. The simulation condition is summarized in table I. The verification of internal voltages is first made. As we mentioned in above

section, no violation of breakdown voltages for transistor-realized switches is ensured by design consideration. The compromise made between Dickson pump capacitors and stacking pump capacitors makes sure that all the design conditions are satisfied. The simulation results are shown in figure 6 and figure 7.

The verification of output voltages of both Dickson charge pump V_D and stacking charge pump Vout is then carried out and the simulation results, illustrated in figure 8, show that the average output voltage V_D is around 27V and the maximum final output voltage Vout is 41V, which further confirms our choice of stage number and other design parameters.

6 Conclusion

A hybrid architecture of CMOS on-chip high voltage generator is proposed in this paper. By using a hybrid structure, the architecture benefits advantages of two charge pump circuits and offers an output voltage higher than each individual one does. Spice simulation results confirm no violation of breakdown voltages of process used and a final output voltage of 41V is obtained.

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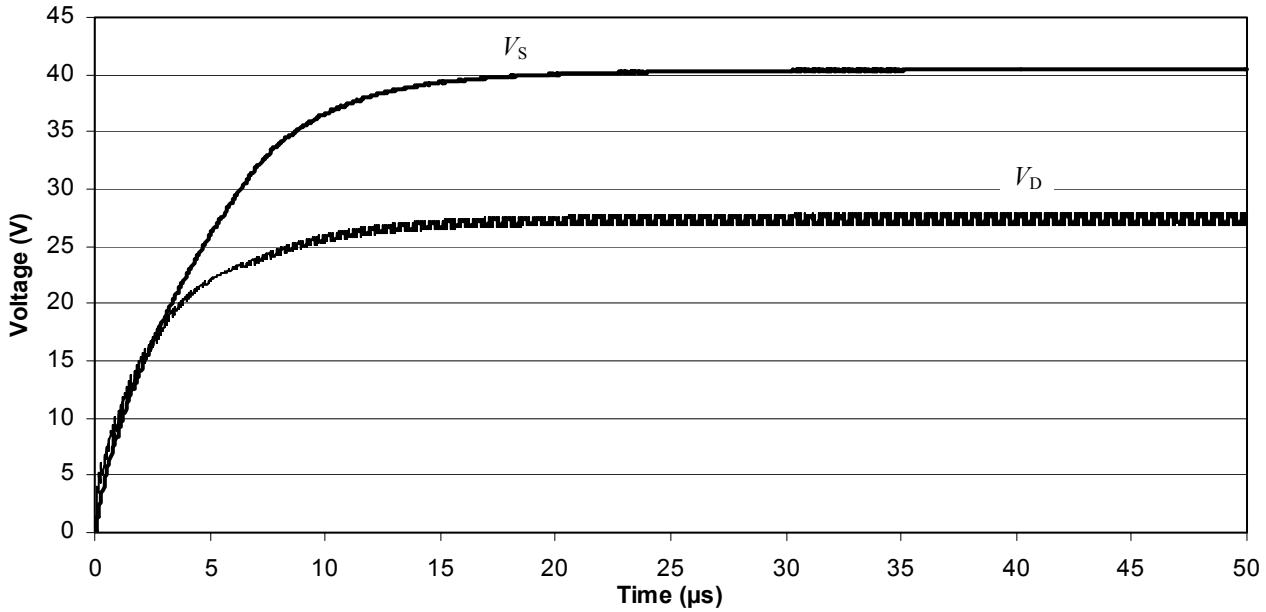

Figure 8. Simulation results of output voltage