Reduction of the gain errors in multi - input Nagaraj – 89 very large time constant integrators

NIKOLAY RADEV[1], NIKOS MASTORAKIS[2], KANTCHO IVANOV[1], VALERI MLADENOV[1]
[1]Department of Theoretical Electrical Engineering, Faculty of Automatics, Technical University of Sofia
8, Kliment Ohridski St, Sofia-1000, BULGARIA
[2]Military Institutions of University Education, Hellenic Naval Academy, Terma Hatzikyriakou, 18539,
Piraeus, GREECE

Abstract: - The multi-input very large time (VLT) constant switched-capacitor (SC) integrators, connected in a feedback loop, are considered. The corresponding gain errors are minimized by modifying the values of the integrating capacitances and the capacitances in the inverting gain branches. Analytical expressions for the prewarped capacitance values are obtained. The effectiveness of this prewarping technique is demonstrated by designing a 60 Hz notch biquad. The minimized gain errors automatically reduce the notch frequency shift.

Key-Words: - Filters, Operational Amplifiers, Switched-capacitor integrators

1 Introduction

Several difficulties arise in designing very large time constant (VLT) switched-capacitor (SC) circuits in which the pole (zero)/sampling frequency ratios are very small. If conventional SC structures are used in the above applications, the required capacitor ratios tend to be huge. Virtually all area-efficient implementations for VLT integrators suffer from higher sensitivity to finite gain A and offset voltage V_{0S} of the operational amplifiers (op amps). With the implementation of gain-and offset-compensation (GOC) technique, the effect due to A and V_{0S} can be reduced [1-8]. The phase errors of the GOC VLT integrators are smaller than those of the uncompensated circuits. However, in the GOC VLT integrators, published before 2000, the gain errors are comparable to the gain errors of the uncompensated structures except for a weaker frequency dependence.

The SC integrators are almost always connected in feedback loop containing an inverting and a noninverting integrator. Such a loop can either function alone as a "biquad" section or may form an internal loop of a multifeedback ladder-type SC filter. The gain errors of the integrators affect the pole and the zero frequencies of the biquads while the phase errors affect the pole quality factor and the magnitude of the biquads transfer function at the pole frequency.

The gain error of the integrators is equivalent to an element value variation ΔC_2 of the integrating capacitor C_2. If the op amp finite gain A is known the gain error can be reduced by modifying the capacitance C_2 [9].
In this paper the approach proposed in [9] is used for minimization of the gain errors in the multi-input Nagaraj-89 tri-phase GOC VLT integrators. The effectiveness of this prewarping technique is demonstrated by means of a 60 Hz notch biquad.

2 Theoretical results

Fig.1 shows the circuit schema and the clock waveform of the multi-input Nagraj-89 tri-phase VLT integrators [1]. The clock phases outside brackets apply to the inverting integrator, whereas those inside brackets apply to the noninverting integrator. The value of the holding capacitor C_h is not critical and can be set equal to the capacitor C_α. The integration is accomplished by N_{23} feed-in integrator branches through N_{23} capacitors connected to the "super-virtual ground" node x during the phases 2 and 3. When the Nagraj-89 integrators are used in two integrator loops the circuit from Fig.1 has N_2 inverting gain branches through N_2 capacitors connected to the input of the SC filter or to the output of one another op amp during the phase 2.
In the z-domain the output voltages of the ideal inverting and noninverting integrators ($A\rightarrow\infty$) are given by

$$V_{0i}^3(z) = -\sum_{q=1}^{N_{23}} \frac{k_q z^{-1/3}}{1-z^{-1}} V_{inq}^2(z) - \sum_{s=1}^{N_2} k_s z^{-1/3} V_s^2(z) \quad (1)$$

$$V_{0n}^2(z) = \sum_{q=1}^{N_{23}} \frac{k_q z^{-2/3}}{1-z^{-1}} V_{inq}^3(z) - \sum_{s=1}^{N_2} k_s V_s^2(z) \quad (2)$$

where

$$k_q = \frac{C_{1q} C_\alpha}{C_f (C_f + C_\alpha)} \quad and \quad k_s = \frac{C_s}{C_f}$$

are the ideal gains.

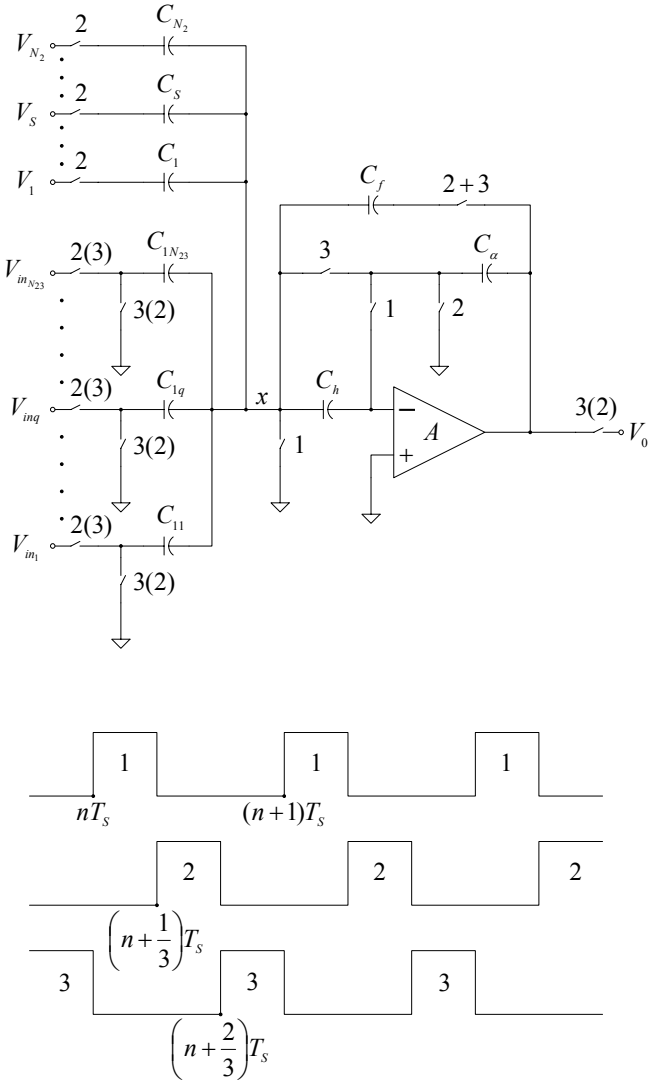

Fig.1: Nagaraj-89 integrators and clocking scheme.

Assuming a finite amplifier gain A, the nonideal transfer functions can be written in the continuous-time domain as

$$H_{iq}^{32}(j\omega)=\frac{V_0^3(j\omega)}{V_{inq}^2(j\omega)}=H_{qid}^{32}(j\omega)[1+m_i(\omega)]\exp[j\theta_i(\omega)] \quad (3)$$

$$H_{is}^{32}(j\omega)=\frac{V_0^3(j\omega)}{V_s^2(j\omega)}=H_{sid}^{32}(j\omega)[1+m_{is}(\omega)]\exp[j\theta_{is}(\omega)] \quad (4)$$

$$H_{nq}^{23}(j\omega)=\frac{V_0^2(j\omega)}{V_{inq}^3(j\omega)}=H_{qid}^{23}(j\omega)[1+m_n(\omega)]\exp[j\theta_n(\omega)] \quad (5)$$

$$H_{ns}^{22}(j\omega)=\frac{V_0^2(j\omega)}{V_s^2(j\omega)}=H_{sid}^{22}(j\omega)[1+m_{ns}(\omega)]\exp[j\theta_{ns}(\omega)]. \quad (6)$$

Here, $H_{id}(j\omega)$ are the ideal transfer functions, $m(\omega)$ are the gain errors in the transfer functions and $\theta(\omega)$ are the phase errors.

Detailed analysis gives the following expressions for the gain errors $m_i(\omega)$ and $m_n(\omega)$ of the Nagraj-89 inverting and noninverting integrators:

$$m_i(\omega)\approx-\frac{1}{A}\left(1+\sum_{q=1}^{N_{23}}\frac{C_{1q}}{C_f+C_\alpha}\right) \quad (7)$$

$$m_n(\omega)\approx-\frac{1}{A}\left(1-\frac{1}{A}+\sum_{q=1}^{N_{23}}\frac{C_{1q}}{C_f+C_\alpha}\right). \quad (8)$$

The gain errors for the inverting gain branches are

$$m_{is}(\omega)=m_{ns}(\omega)=m_s(\omega)\approx-\frac{C_\alpha}{(C_f+C_\alpha)A}. \quad (9)$$

The gain errors $m_i(\omega)$ and $m_n(\omega)$ can be minimized by modifying the feedback (integrating) capacitance C_f. This is achieved by equating the gains of the nonideal integrators for the prewarped capacitances C_{fi} and C_{fn} and for the nominal value A_0 of the op amp dc gain A, with the corresponding ideal gains k_q.

This results in the expressions

$$\frac{C_{1q}C_\alpha}{C_{fi}(C_{fi}+C_\alpha)}[1+m_i(C_{fi},A_0)]=\frac{C_{1q}C_\alpha}{C_f(C_f+C_\alpha)} \quad (10)$$

$$\frac{C_{1q}C_\alpha}{C_{fn}(C_{fn}+C_\alpha)}[1+m_n(C_{fn},A_0)]=\frac{C_{1q}C_\alpha}{C_f(C_f+C_\alpha)}. \quad (11)$$

Then the prewarped capacitances C_{fi} and C_{fn} are the solutions of the cubic equations

$$C_{fi}^3+2C_\alpha C_{fi}^2-(a_i-C_\alpha^2)C_{fi}-a_ib_i=0 \quad (12)$$

$$C_{fn}^3+2C_\alpha C_{fn}^2-(a_n-C_\alpha^2)C_{fn}-a_nb_n=0 \quad (13)$$

where

$$a_i=C_f(C_f+C_\alpha)\left(1-\frac{1}{A_0}\right),$$

$$b_i=C_\alpha-\frac{1}{A_0-1}\sum_{q=1}^{N_{23}}C_{1q},$$

$$a_n=C_f(C_f+C_\alpha)\left[1-\frac{1}{A_0}\left(1-\frac{1}{A_0}\right)\right],$$

$$b_i=C_\alpha-\frac{1}{A_0-1+1/A_0}\sum_{q=1}^{N_{23}}C_{1q}.$$

Subsequently, the gain errors $m_{is}(\omega)$ and $m_{ns}(\omega)$ can be minimized by modifying the capacitances C_s. This is achieved by equating the nonideal gains for the prewarped capacitances C_{si} and C_{sn}, and for C_{fi}, C_{fn} and A_0, with the corresponding ideal gains k_s. This gives

$$\frac{C_{si}}{C_{fi}}[1+m_s(C_{fi},A_0)=\frac{C_s}{C_f} \quad (14)$$

$$\frac{C_{sn}}{C_{fn}}[1+m_s(C_{fn},A_0)=\frac{C_s}{C_f}. \quad (15)$$

From (14) and (15) we obtain

$$C_{si} = \frac{C_s C_{fi}}{C_f \left[1 - \frac{C_\alpha}{(C_{fi} + C_\alpha) A_0} \right]} \qquad (16)$$

$$C_{sn} = \frac{C_s C_{fn}}{C_f \left[1 - \frac{C_\alpha}{(C_{fn} + C_\alpha) A_0} \right]} \qquad (17)$$

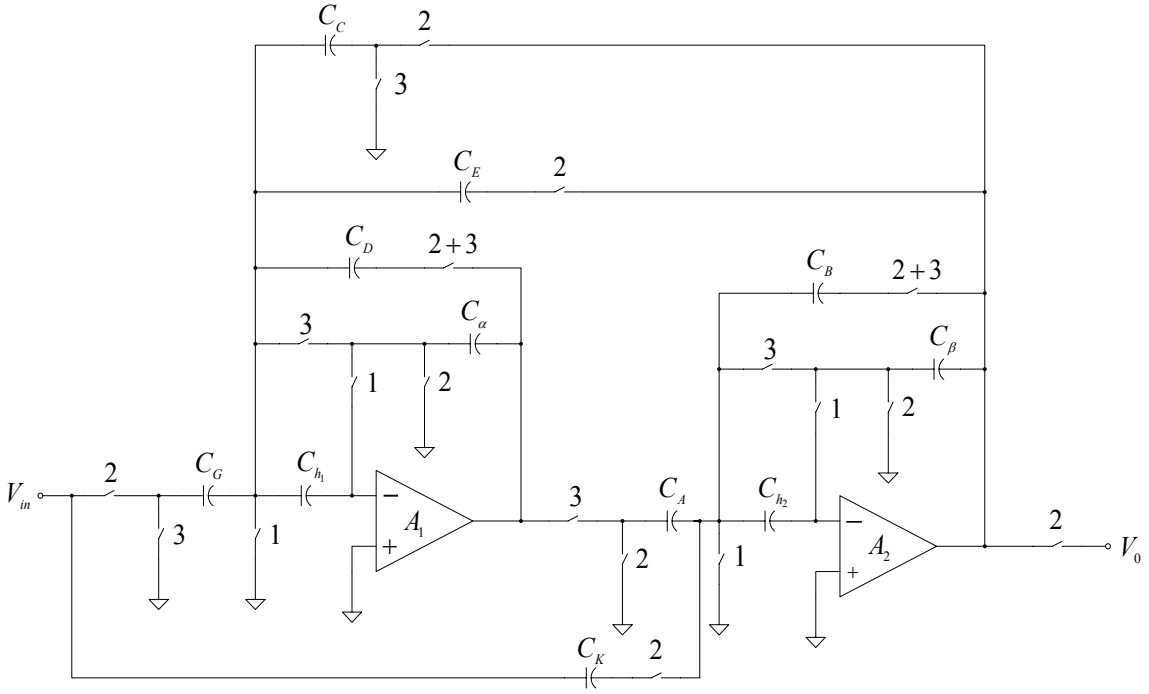

Fig. 2: 60 Hz notch SC biquad with Nagaraj-89 integrator.

3 60 Hz notch SC biquad with small notch frequency shift

The feasibility of the prewarping technique considered is illustrated by the design of a 60 Hz high-pass notch biquad with Nagaraj-89 VLT integrators [1], [10].

The circuit, shown in Fig.2, has a pole frequency f_p = 207 Hz, a pole quality factor Q_p = 0.726 and sampling frequency f_s = 128 kHz. The relative capacitor values are $C_A = C_G$ = 1, C_B = 10, C_C = 11.58, C_D=50, C_E = 43.6, C_K = 10.23568, $C_\alpha = C_{h1}$ = 1.43 and $C_\beta = C_{h2}$ = 1.9.

Table 1 summarizes the actual notch frequency f_{za}, the notch frequency shift $\Delta f_z/f_z$ and the attenuations at f_{za} and at 60 Hz for op amps with nominal finite dc gains $A_{01} = A_{02} = A_0 = 100$.

The notch frequency shift of -1.08% can be partly reduced by modifying the two integrating capacitances C_D and C_B. Then, according to (12) and (13), the prewarped capacitance values C_{Dp} and C_{Bp} are the solutions of the cubic equations.

$$C_{Dp}^3 + 2C_\alpha C_{Dp}^2 - (a_i - C_\alpha^2) C_{Dp} - a_i b_i = 0 \qquad (18)$$

$$C_{Bp}^3 + 2C_\beta C_{Bp}^2 - (a_n - C_\beta^2) C_{Bp} - a_n b_n = 0 \qquad (19)$$

Notch biquad with capacitances	f_{za} [Hz]	$\Delta f_z/f_z$ [%]	Attenuation [dB] at f_{za}	Attenuation [dB] at 60 [Hz]
C_D, C_B, C_E, C_K	59.352	-1.08	-91.37	-54.44
C_{Dp}, C_{Bp}, C_E, C_K	59.873	-0.212	-91.04	-68.66
C_{Dp}, C_{Bp}, C_{Ep}, C_{Kp}	60.001	0.0017	-91.07	-91.06

Table 1: Performance parameters of the notch biquad with Nagaraj-89 VLT integrators

where

$$a_i = C_D (C_D + C_\alpha) \left(1 - \frac{1}{A_{01}} \right),$$

$$b_i = C_\alpha - \frac{C_G + C_C}{A_{01} - 1},$$

$$a_n = C_B (C_B + C_\beta) \left[1 - \frac{1}{A_{02}} \left(1 - \frac{1}{A_{02}} \right) \right],$$

$$b_n = C_\beta - \frac{C_A}{A_{02} - 1 + 1/A_{02}}.$$

One obtains C_{Dp} = 49.68309 and C_{Bp} = 9.94146 for A_{01} = A_{02} =100.

The corresponding performance parameters of the notch biquad are also given in Table 1. It is seen that the notch frequency shift is reduced to -0.212 %.

Subsequently, the relative error $\Delta f_z/f_z$ can be further minimized by modifying the capacitances C_E and C_K in the two inverting gain branches, according to the relations (16) and (17). Then, the prewarped capacitances C_{Ep} and C_{Kp} are given by the expressions

$$C_{Ep} = \frac{C_E C_{Dp}}{C_D\left[1 - \frac{C_\alpha}{(C_{Dp} + C_\alpha)A_{01}}\right]} \qquad (20)$$

$$C_{Kp} = \frac{C_K C_{Bp}}{C_B\left[1 - \frac{C_\beta}{(C_{Bp} + C_\beta)A_{02}}\right]}. \qquad (21)$$

One obtains C_{Ep} = 43.33578 and C_{Kp} = 10.19211, for A_{01} = A_{02} =100.

The resultant notch frequency shift, shown in Table 1, is 0.0017%.

The prewarping technique proposed is effective for operational amplifiers with low but precisely known and stable dc gain [11]. Table 2 summarizes the performance parameters of the notch biquad with the prewarped capacitances C_{Dp}, C_{Bp}, C_{Ep}, C_{Kp} and with gain variation $A_1 = A_2 = A = 100 \pm 8$.

A	f_{za} [Hz]	$\Delta f_z/f_z$ [%]	Attenuation [dB] at f_{za}	/ 60 [Hz]
92	59.944	-0.093	-92.88	-75.74
100	60.001	0.0017	-91.07	-91.06
108	60.049	0.082	-90.05	-76.83

Table 2: Performance parameters of the notch biquad with prewarped capacitances and gain variation

4 Conclusions

The gain errors of the multi-input Nagaraj-89 inverting and noninverting integrators are reduced by modifying the integrating capacitances and the capacitances in the inverting gain branches. The feasibility of this prewarping technique is demonstrated by designing a 60 Hz notch biquad. The minimization of the gain errors significantly reduces the notch frequency shift of the biquad and increases the attenuation at 60 Hz.

Acknowledgments

This work is supported by TU-Sofia project 542-8/2005 "Analysis and design of circuits and systems for signal processing".

References:

[1] K. Nagaraj, "A parasitic-insensitive area-efficient approach to realizing very-large-time constants in switched-capacitor circuits", *IEEE Trans. Circuits Syst.*, vol. 36, N9, 1989, pp. 1210-1216.

[2] W.-H. Ki and G. C. Temes, "Offset-compensated switched-capacitor integrators", *in Proc. IEEE Int. Symp. Circuits Syst.*, 1991, pp. 2829-2832.

[3] J. Lin, W.-H. Ki, K Thompson, and S. Shamma, "Realization of cochlear filter by VLT switched capacitor biquads", *in Proc. IEEE Int. Conf. of Automatics, Speech & Signal Processing*, vol.2, 1992, pp. 245-248.

[4] W.-H. Ki and G. C. Temes, "Area-efficient gain and offset-compensated very-large-time constant SC biquads", *in Proc. IEEE Int. Symp. Circuits Syst.*, 1992, pp. 1187-1190.

[5] J. Lin, W.-H. Ki, T. Edwards, and S. Shamma, "Analog VLSI implementations of auditory wavelet transforms using switched-capacitor circuits", *IEEE Trans. Circuits Syst.*, vol.41, N9, 1994, pp. 572-583.

[6] N. A. Radev and K. P. Ivanov, "Area-efficient gain- and offset-compensated very-large-time constant SC integrator", *Electron. Lett.*, vol.36, N5, 2000, pp. 394-396.

[7] N. A. Radev and K. P. Ivanov, "Gain-and offset-compensated very-large-time constant SC integrator", *Journal of Electrical Engineering, Bratislava*, N3-4, 2000, pp. 109-112.

[8] N. A. Radev and K. P. Ivanov and K Stoykov, "Gain-and offset-compensated switched-capacitor integrators", i*n Proc. XI International Symposium on Theoretical Electrical Engineering*, 2001, Linz, Austria, pp. 125-132.

[9] K. Haug, F. Maloberti, and G. C. Temes, "Switched-capacitor integrators with low finite-gain sensitivity", *Electron. Lett.*, vol.21, N24, 1985, pp. 1156-1157.

[10] N. A. Radev and K. P. Ivanov, "Comparative analysis of two gain and offset-compensated very-large-time constant switched-capacitor integrators", *in Proc. XII International Conference on Microelectronics*, 2000, Tehran, Iran, pp. 51-54.

[11] A Baschirotto, R. Alini, and R Castelo, "BiCMOS operational amplifier with precise and stable DC gain for high-frequency switched-capacitor circuits", *Electron. Lett.*, vol.27, N15, 1991, pp. 1338-1340.