

Duty Cycle Adjusting Circuit for Clock Signals

HWANG-CHERNG CHOW

Department of Electronics Engineering, Chang Gung University
259 Wen-Hwa 1st Road, Kwei-Shan, Tao-Yuan 333
TAIWAN, REPUBLIC OF CHINA

Abstract: - A duty cycle control circuit for clock signals is presented. The proposed circuit uses a rising edge detector to generate one shot output signals which have the same frequency of the input clock signal. A pulse width controllable monostable multivibrator converts the one shot signals into rectangular pulses. By the feedback control voltage from an operational amplifier, the pulse width of generated rectangular pulses is automatically adjusted to a pre-set duty cycle. As compared to prior arts, features of this proposed circuit include simple design, low cost and less power.

Key-Words: - Duty cycle, Clock, Edge detector, Pulse width control, Monostable, One shot

1 Introduction

The characteristics of an electrical signal can be described by a number of parameters such as frequency, period, duty cycle, on-time and off-time. For an periodical signal its period refers to the time interval of a single cycle while its frequency is inverse of its period. Digital signals alternate their voltage levels between high and low. The amount of time spent at the high level is called "on-time" and the amount of time spent at the low level is therefore called "off-time". As for duty cycle, it means the ratio of on-time to period, so it is generally specified as a percentage.

For general IC design, a system clock signal is often required. However, in some cases the duty cycle of a clock signal from an oscillator is unpredictable. To make the characteristics of the clock signal from any clock generator more predictable the duty cycle has to be a known value, for example, 50 percent [1]-[6]. A conventional clock duty cycle controller used for 50 percent duty cycle adjustment directly doubles the frequency of the clock signal by an oscillator and then divides the resulted signal. However, this is disadvantageous since the current consumption is increased due to the oscillator operating at a higher frequency.

In other applications a phase locked loop is used for clock signal generation [1]. For a 50

percent duty cycle output by a phase locked loop, this approach is shown in Fig. 1.

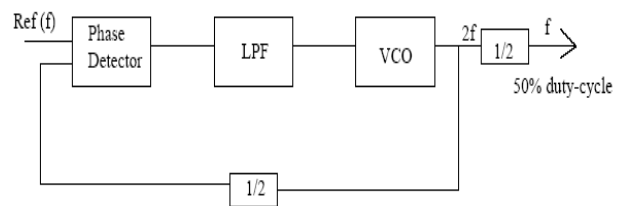


Fig. 1 Phase locked loop

As mentioned before, this phase locked loop first doubles the incoming clock frequency and then divides its output with a divider, such as a D flip-flop. Although the resulted output has a symmetrical waveform, two drawbacks of this approach have to be summarized.

First, the total power consumption is increased because the voltage controlled oscillator(VCO) operates at 2X frequency of the input clock signal. Second, the VCO design is actually difficult and so costly to fabricate as an integrated circuit. Therefore, this approach is expensive in terms of costs of implementation.

In the literature, many prior arts are devoted to improving the VCO design to obtain 50 percent duty cycle output signal directly [2]--[4]. As a consequence, the power consumption is effectively reduced since the VCO abates the

need of operating at 2X frequency. However, such analog VCO design becomes more complicated and so leads to very expensive cost.

Other methods used for controlling the duty cycle of a signal are described in the literature [5]--[7]. Krambeck describes a circuit, as shown in Fig. 2, in which the average voltage of a clock out pulse(at node t7) is compared to a reference voltage($V_{DD}/2$) in an operational amplifier. The OPAMP output(V_{fb}) is fed back to transistors MP2 and MN1 to alter the timing of the clock pulses inputted to pullup transistor MP1 and pulldown transistor MN2, thereby controlling the rise time and fall time of the output clock signal at node t2. Since the operating frequency of the whole circuit is the same as that of the input clock signal, the circuit consumes less power as compared to the described-above PLL approach.

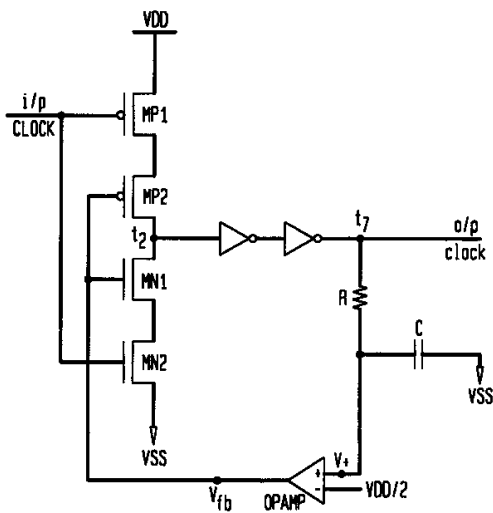


Fig. 2 Prior art circuit for duty cycle control

However, this circuit tends to have a loop stability problem under certain conditions. As the duty cycle of the input clock signal is sometimes unpredictable, its duty cycle, for example, may vary from 20 percent to 80 percent. Although the duty cycle may change, its frequency remains the same. Therefore, for a pre-determined operating frequency the RC time constant of the low pass filter usually keeps the same. As a result, for an input clock signal with duty cycle greater than 50 percent the disclosed circuit tends to have an unstable loop function. The instability occurs because

the NMOS transistor of the input stage (MN2) may be turned on for a longer time period than the feedback signal V_{fb} is able to control via transistor MN1.

Therefore, an improved method for adjusting the duty cycle of a clock signal is desired, which should provide two advantages of less power than PLL and better stable loop function at the same time. Thus, a low cost duty cycle control circuit will be proposed in this paper to overcome mentioned-above disadvantages. The presented circuit directly deals with duty cycle adjustment without any further frequency multiplication. In the next Section, circuit operations are described along with simulation results given in Section 3.

2 Proposed Circuit

Fig. 3 shows the proposed duty cycle control circuit. The circuit structure is described first.

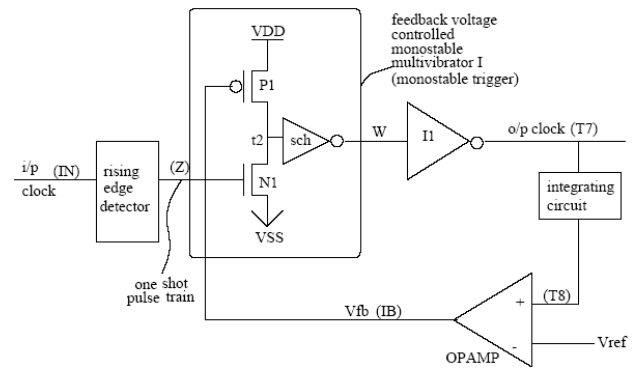


Fig. 3 Duty cycle control circuit

- (1)rising edge detector: This functional block is a rising edge detector to detect the transition of the input clock signal. To implement this edge detector only simple NOR gate, inverters and delay elements are needed. After the edge detection of the input clock signal a one shot pulse train is generated. Importantly, the one shot pulse train is at the same frequency as the input clock, but its duty cycle is much less than 50%.
- (2)feedback voltage controlled monostable multivibrator (monostable trigger): This functional block generates an output signal W whenever it is triggered by the one shot pulse input, as illustrated in Fig. 4. The pulse

width of the output rectangular signal is controlled by the feedback voltage V_{fb} ,

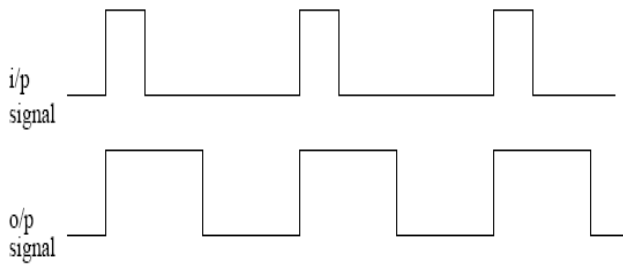


Fig. 4 Operation of monostable trigger

in conjunction with PMOS P1 and the Schmitt trigger circuit. Alternately, an inverter can be used in place of the Schmitt trigger.

- (3)inverter: This functional block inverts the monostable output signal in order to output a clock signal whose duty cycle is the complement of the duty cycle of the monostable output signal.
- (4)integrating circuit: This functional block integrates the final output clock signal and outputs this average voltage to the positive input of the operational amplifier, OPAMP. Note that when the final output clock signal has 50 percent duty cycle this average voltage is equal to $V_{DD}/2$. In fact, an integrating circuit has the effect of a low pass filter. So, a simple RC low pass filter can be used in circuit implementation.
- (5)OPAMP: This functional block may be a high gain operational amplifier or differential amplifier. The negative input receives a reference voltage, V_{ref} . The output of this OPAMP is a control voltage, V_{fb} , fed back to the monostable trigger to adjust the turn-on strength of PMOS device P1.

The described-above functional blocks 1, 2, 3, 4 and 5 comprise a duty cycle control circuit. In brief, this duty cycle control buffer automatically adjusts the duty cycle of an input clock signal via a closed loop function. The desired duty cycle value is determined by the reference voltage V_{ref} . Detailed circuit operations of this duty cycle control circuit are described below.

Consider two cases to illustrate the operation of the duty cycle control circuit: (1) the duty cycle is greater than desired, and (2) the duty cycle is less than desired.

- (1)If the duty cycle is greater than desired, the average voltage derived from the output clock signal by the integrating circuit will be larger than V_{ref} . When the average voltage from the integrating circuit is larger than V_{ref} , the OPAMP will output a feedback control voltage V_{fb} with increased amplitude. The increase in V_{fb} at the gate of PMOS P1 will have the effect of decreasing the turn-on strength of PMOS P1. Therefore, the voltage level at node t2 (P1's drain) will be pulled up to V_{DD} more slowly. As a result, the output signal from the monostable trigger will have an increased pulse width. This signal is then inverted, so that the resultant output signal at node t7 has a narrowed pulse width. Therefore, the average voltage, which is derived from the output clock signal by the integrating circuit, will decrease until the desired duty cycle is achieved (steady-state) as determined by the value of the reference voltage V_{ref} .
- (2)If the duty cycle is less than desired, the average voltage derived from the output clock signal by the integrating circuit will be less than V_{ref} . When the average voltage from the integrating circuit is less than V_{ref} , the output control voltage V_{fb} will decrease in amplitude. The decrease in V_{fb} at the gate of PMOS P1 will have the effect of increasing the turn-on strength of PMOS P1. Therefore, the voltage level at node t2 (P1's drain) will be pulled up to V_{DD} more quickly. As a result, the output signal from the monostable trigger will have a decreased pulse width. This signal is then inverted, so that the resultant output signal at node t7 has an increased pulse width. Thus, the average voltage derived from the output clock signal by the integrating circuit, will increase until the desired duty cycle is achieved, as determined by the value of the reference voltage V_{ref} .

Since the closed loop has negative feedback in its function, the loop function will finally become stable under the steady-state condition. Once the closed loop is under the steady-state condition, the desired duty cycle pre-set by V_{ref} is obtained. Moreover, due to the action of the edge detector, the feedback loop stability of the proposed circuit is not affected by the pulse width/duty cycle of the input clock signal.

For general applications of IC design or digital signal processing it is desirable that the clock signal is a symmetrical square wave with 50 percent duty cycle. To shape an incoming non-symmetrical clock signal to 50 percent duty cycle the disclosed circuit with $V_{ref}=V_{DD}/2$ can meet this requirement.

3 Results and Discussions

Both Fig. 5 and Fig. 6 are simulation results according to Fig. 3 circuit for an input clock signal of 50MHz with duty cycle 20 percent and 80 percent, respectively.

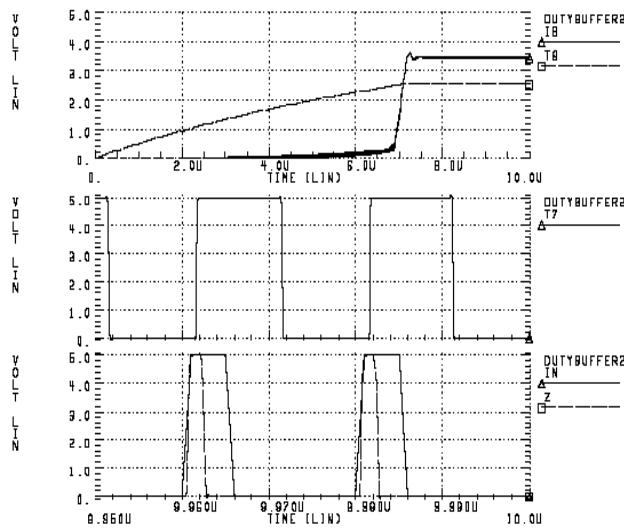


Fig. 5 Simulation results I (50MHz, 20% duty cycle input)

These simulation results are based on 0.6um process parameters. In both figures, the input clock signal is IN, edge-detected output Z, feedback voltage IB, average voltage T8 and the final output clock signal T7.

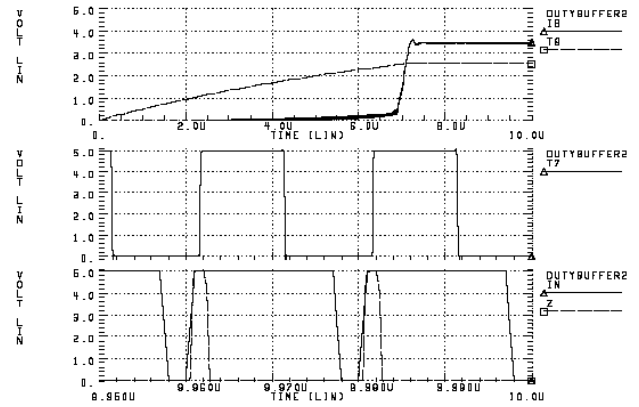


Fig. 6 Simulation results II (50MHz, 80% duty cycle input)

Judging from these simulation results, the output clock signal is well controlled with 50 percent duty cycle. To illustrate the operational advantage of the proposed circuit with respect to the prior art circuit of Fig. 2, a number of simulation tests were conducted. Fig. 7 and Fig. 8 show simulation results for the prior art circuit(Fig. 2) with 10 percent and 80 percent duty cycle. While the simulation test results of the proposed circuit are shown in Fig. 9 and Fig. 10, respectively. While the output clock signal $v(t7)$ in Fig. 7 is a proper representation of the input clock signal $v(in)$, this is not the case in Fig. 8. That is, despite the fact that the closed loop of the prior art circuit has reached a steady state condition, the resultant output clock signal is periodically in error, as shown in Fig. 8.

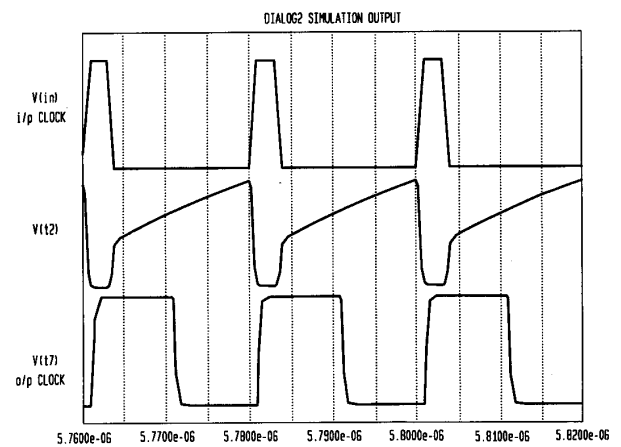


Fig. 7 Simulation results of prior art (10% duty cycle input)

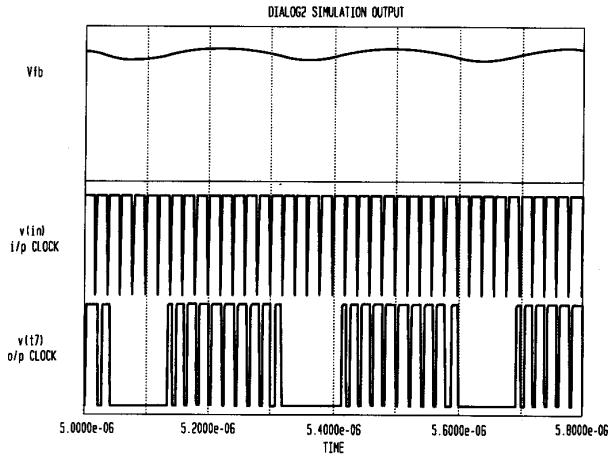


Fig. 8 Simulation results of prior art (80% duty cycle input)

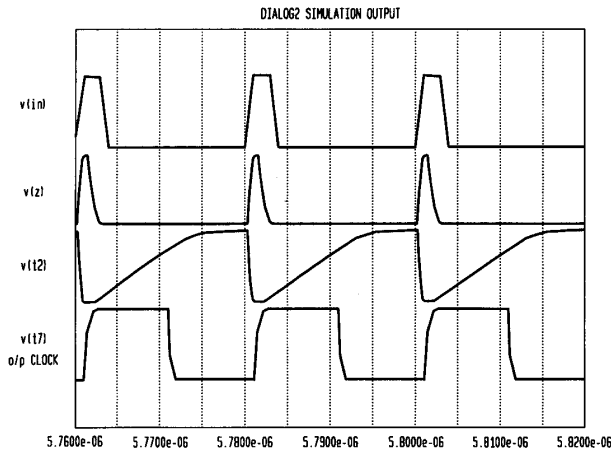


Fig. 9 Simulation results of proposed circuit (10% duty cycle input)

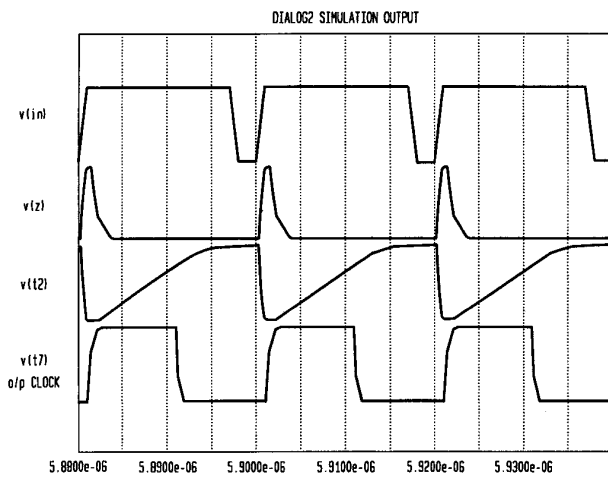


Fig. 10 Simulation results of proposed circuit (80% duty cycle input)

Due to the effect of the edge detector, the loop stability of the proposed circuit is very

satisfactory without regard to the original duty cycle of the input clock signal, as shown in Fig. 9 and Fig. 10.

For an input clock of higher frequency such as 100MHz the simulation results are presented in Fig. 11.

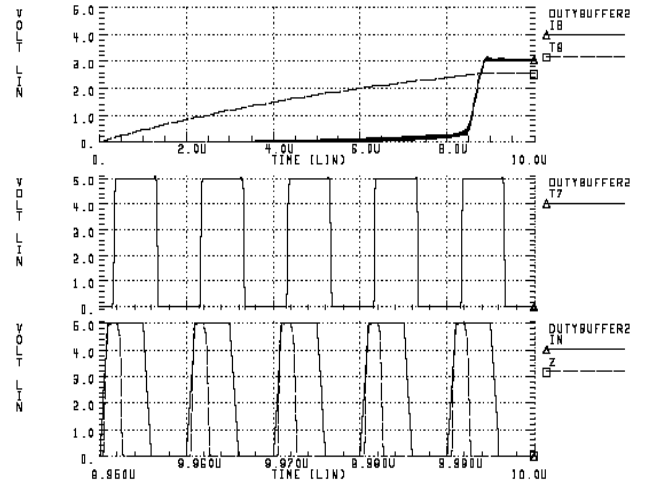


Fig. 11 Simulation results III (100MHz input)

The output clock signal t7 is also adjusted to a symmetrical square wave through proper loop function.

In fact, in a real design example only 32 MOS transistors are required to implement the proposed duty cycle control circuit. As compared to the conventional duty cycle controller such as a PLL (over 150 MOS transistors) the design complexity is greatly reduced. In addition, only an operational amplifier has to be incorporated in the loop circuit instead of a high cost VCO. Furthermore, the proposed whole loop circuit operates at the same frequency as the input clock signal so power consumption can be effectively reduced.

4 Conclusion

In this paper, a duty cycle adjusting circuit for clock signals has been demonstrated, which features simple design, low cost and reduced power. According to simulation results the proposed circuit is effective in adjusting the duty cycle of an input clock signal with frequency up to 100MHz. Besides, the whole

loop function shows much better stability than that of the prior art circuit. Due to simplicity of the proposed design it is very suitable for applications of duty cycle adjustment in combination with clock signal generators such as crystal oscillators or phase locked loop circuits.

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