Development of a Wavelet Encoder in FPGA

Felipe Gama, Rodrigo Semente, Luiz Silveira
Universidade Federal do Rio Grande do Norte
Department of Computer Engineering and Automation
Senador Salgado Filho Av, 3000
CEP: 59078-970, Natal, RN
Brazil
felipe.sgama@hotmail.com, rsemente@yahoo.com.br, lfelipeqs@gmail.com

Abstract: The performance of wireless communications systems is mainly limited by fading produced by multipath propagation. In order to minimize the destructive effects of fading, several techniques have been proposed recently, among them, diversity techniques and channel coding. The classical techniques of channel coding use controlled addition of redundancy to the information. Among the known coding techniques in the literature, the wavelet coding presents an alternative in which the robustness achieved against the effects of multipath fading occurs because of a temporal diversity on the transmitted information. This paper presents architectures for wavelet encoder and decoder on Field Programmable Gate Array (FPGA). The proposed architectures are analysed in terms of computational complexity. The obtained results demonstrate the low cost for hardware implementation, as well as attest the efficiency of the technique in combating the destructive effects of wireless communication systems. The implementation was validated by means of platforms MATLAB-SIMLINK e Xilinx-system generator.

Key–Words: Fading, FPGA, wavelet encoding.

1 Introduction

In wireless communication systems, the signal usually spreads in multiple paths. Due to factors such as scattering and refraction atmospheric or sea. In this environment of communication, the signals that arrive at the receiving antenna will have mitigations and different delays and may affect severely the performance of these systems. In order minimize the destructive interference of these channels, several strategies have been proposed.

In this sense, it is increasing the number of coding and diversity techniques to combat the degenerative effects of these channels. In particular, the techniques of diversity consists basically in generate redundancy (replicas) of the transmitted signal at the receiver. These replicas are transmitted on independent channels, and therefore, are affected differently, uncorrelated way by the channel. With the generation of replicas there is a spreading of information in time which usually decreases considerably the spectral efficiency of the system. However, there is a strategy to generate diversity without compromising the spectral efficiency of the system known as wavelet coding.

The wavelet coding was initially proposed in [2], as a new alternative to combat the effects of fading. The wavelet coding is based on the properties of orthogonality between the rows of the wavelet coefficients matrix (WCM). In the wavelet encoding process, each bit of data entering the encoder is multiplied successively by the coefficients of a line of WCM, disseminating information of each bit in multiple coded symbols. The result of this encoding is a not equiprobable and multilevel wavelet set of symbols that carry information from various bits, which are transmitted in different time intervals.

Due to the orthogonality property of WCM, the sequence of information bits is retrieved from a correlatores bank. This mechanism for the spreading of information in time, before the transmission and gathering it at the receiver, contributes to improve the robustness of the communication system to the combination of time-variant plant fading and located noise effects.

In previous studies, the wavelet coding was evaluated, as well as the properties of transmission errors correction in, [1, 2, 4, 6, 7, 8]. The results show the efficiency of this technique and provides subsidies for a future use of the technique in communication standards. But evaluation related to the complexity of hardware has not been made so far.

The implementation hardware cost of communication systems is a determinant factor in the design of embedded systems. In this aspect, several architectures was investigated [9, 10, 11]. This study aims to verify the implementation cost of the wavelet en-

coder and decoder in reconfigurable hardware FPGA. It is believed that the performance evaluation and the hardware cost can proof the viability for the use of the wavelet coding in embedded systems. We present simulation results to validate the implementation and computational cost.

The remainder of this article is organized as follows. Section 2 presents a review of the technique of wavelet coding. In Section 3 is presented the model of the system that will be implemented. Section 4 is devoted to the details of the project for implementation of wavelet coding. The numerical results obtained with the simulation of the proposed scheme are shown and discussed in Section 5. Finally, Section 6 presents the conclusions of this paper.

2 Fundamentals of Wavelet Coding

Wavelet coding uses the rows of a wavelet coefficient matrix (WCM) in order to encode information bits. As presented in [5], a WCM of order m and genus g has dimension $m \times mg$, denoted by

$$\mathbf{A} = \begin{pmatrix} a_0^0, & \ldots, & a_{mg-1}^0 \\ a_0^1, & \ldots, & a_{mg-1}^1 \\ \vdots & & \vdots \\ a_0^{m-1}, & \ldots, & a_{mg-1}^{m-1} \end{pmatrix}, \qquad (1)$$

whose entries can belong to the field of complex or real numbers.

In particular, the WCM matrix is planar and integer when it is coefficients are integer numbers chosen from the set $[-1, 1]$ and satisfy the wavelet scaling conditions:

$$\sum_{k=0}^{mg-1} a_k^j = m\sqrt{g}\delta_{0,j}, \quad 0 \le j \le m-1 \qquad (2)$$

$$\sum_k a_{k+ml}^j a_{k+ml'}^{j'} = mg\delta_{j,j'}\delta_{l,l'}, \; 0 \le j, j' \le m-1$$
$$0 \le l, l' \le g-1 \qquad (3)$$

in which $\delta_{j,j'}$ is the Kronecker delta.

The fundamental property of WCM's for channel coding purposes is given by Equation (3). This equation states that the rows of a order m WCM are mutually orthogonal at shifts of length lm, where $0 \le l \le g-1$. It also states that each row is orthogonal to a copy of itself shifted by lm, where $0 < l \le g-1$. In the theory of digital filter-banks, the rows $\{a^j\}$ represent bandpass filters of a filter-bank with m-bands.

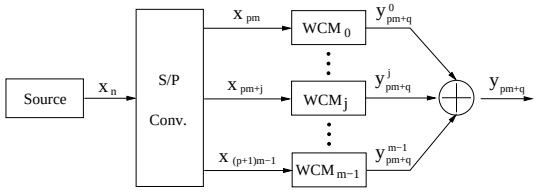
2.1 Algorithm of Wavelet Encoding

Consider a discrete source that generates bits $x_n \epsilon [-1, 1]$ statistically independent of each other. In the encryption process, the sequence of information bits x_n is initially divided into m parallel sequences, defined by

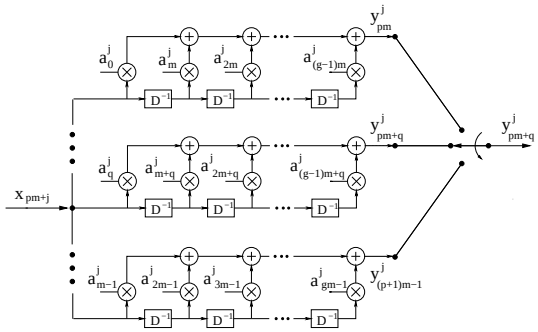
$$X_{pm+j} := \{x_{pm+j}\}_{p \in \mathbb{Z}}, 0 \le j < m,$$

as can be observed in Figure 1(a). The jth parallel sequence X_{pm+j} is then coded by a bank of registers of displacement, denoted by block WCM_j detailed in Figure 1(b).

The symbols y_n can also be obtained from a matrix product simple, expressed by $y = x \times C_{WCM}$ where y is the vector of symbols wavelet generated and C_{WCM} is a matrix of codification, constructed from successive repetitions and displacements (in m positions) of the WCM until the matrix number of rows of C_{WCM} is equal to the dimension of the vector of bits of information that you want to encode.



(a) Encoder overview.



(b) Wavelet encoder based on $m \times mg$ WCM. The WCM_j block is defined by the jth row of the WCM.

Figure 1: Wavelet encoder based on $m \times mg$ WCM. The WCM_j block is defined by the jth row of the WCM.

The symbol wavelet generated in time interval $n = pm + q$, can be given by:

$$y_{pm+q} = \sum_{j=0}^{m-1} \sum_{l=0}^{g-1} a_{lm+q}^j x_{(p-l)m+j}, \qquad (4)$$

and takes values in the alphabet of symbols defined in wavelet set $\mathcal{Y} =$

$\{-mg, -mg+2, \ldots, -2k, \ldots, 0, \ldots, 2k, \ldots, mg\}$, with cardinality, $\|\mathcal{Y}\|$, equal to $mg+1$. Consequently, the wavelet multilevel symbols are different and depend on bits of information.

2.2 Algorithm of Wavelet Decoding

At the reception the sequence of information bits x_n can be recovered from the sequence of symbols y_n received using a bank of m correlators length mg, related to the m lines of MCW used in wavelet coding. Assuming absence of noise, the output of the correlator z^j, $j \in \{0, 1, \ldots, m-1\}$, related to the line a^j of MCW, at the moment of time $i = m(g+p)-1$, $p \in \mathbb{Z}$, is given by:

$$\begin{aligned} z_i^j &= \sum_{k=0}^{mg-1} a_{mg-1}^j y_{i-k} \\ &= \sum_{k=0}^{mg-1} \sum_{j'=0}^{m-1} \sum_{l=0}^{g-1} a_k^j (a_{k-lm}^{j'} x_{j'+lm+i-(mg-1)}) \\ &= x_{j+i-(mg-1)}) \sum_{k=0}^{mg-1} a_k^j a_k^j \\ &= mg x_{j+i-(mg-1)} \end{aligned} \tag{5}$$

In general, taking into account the interference caused by the channel of communication on the symbols wavelet transmitted, it is assumed estimates of the bits provided by $\hat{x}_{j+i-(mg-1)} = \text{sgn}(z_i^j)$.

3 Model System

Figure 2 illustrates the system model with wavelet encoding used in this paper. In this system, the information source generates a bit sequence x_n statistically independent. This sequence of bits is then coded by a planar and integer WCM with dimensions of $m \times mg$. In implementation was used a WCM planar of dimension 2×8.

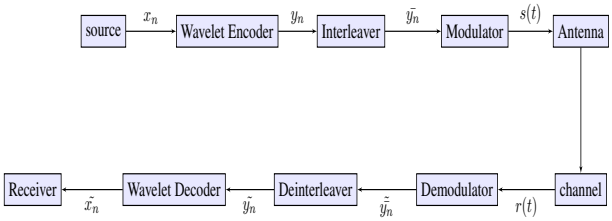


Figure 2: Model of the communication system based on wavelet coding.

The system based on WCM, each symbol value generated, $\bar{y_n}$, must be mapped to a point in a PSK constellation of unit radius with $mg+1$ points in accordance with the Equation (4). It uses a single antenna to transmit signals PSK. The received signal is denoted by $r(t)$ is given by:

$$r(t) = \alpha(t) \cdot s(t) + n(t), \quad iT_s \leqslant t \leqslant (i+1)T_s, i \geqslant 2.mg \tag{6}$$

Where $s(t)$ is the transmitted signal, $\alpha(t)$ is the channel with planar fading and $n(t)$ is the complex white Gaussian noise with zero mean and spectral energy density of $N_0/2$. The signal $\alpha(t)$ can be modeled by a stationary process Gaussian. It is considered a perfect interleaving fading channel, ie, the process $\alpha(t)$ is uncorrelated in time.

At the receiver, the m signals received in each range of signalling T_s are converted into their vector representations by a bank of correlators. The received vector r_i in the range of signals i, is given by:

$$r_i = \alpha_i \cdot s_i + n_i \tag{7}$$

Where s_i is the vector representation of the transmitted signal in time. The elements of vector n_i belong to the set of complex numbers, are random variables Gaussian, statistically independent and identically distributed with mean zero and variance $N_0/2$. After using the estimates of α_i to compensate for the multipath fading effects, a rule of decision MAP is applied in order to obtain the estimates of PSK symbols transmitted.

At the reception, we assume a perfect estimation of the channel state, ie, the receiver knows the exact value of the fading at each instant of time. It is considered that the receiver is able to obtain estimates of the PSK signal transmitted by metric decision Euclidean and MAP. The estimates are mapped into Wavelets symbols $\tilde{y}(n)$.

4 Design on FPGA

This section presents an architecture of wavelet encoder and decoder on a hardware platform like FPGA. It is defined that all the variables and constants are in fixed point and use a resolution of n bits of which b bits are for the part in floating point and $(n-b)$ bits represent the integer part.

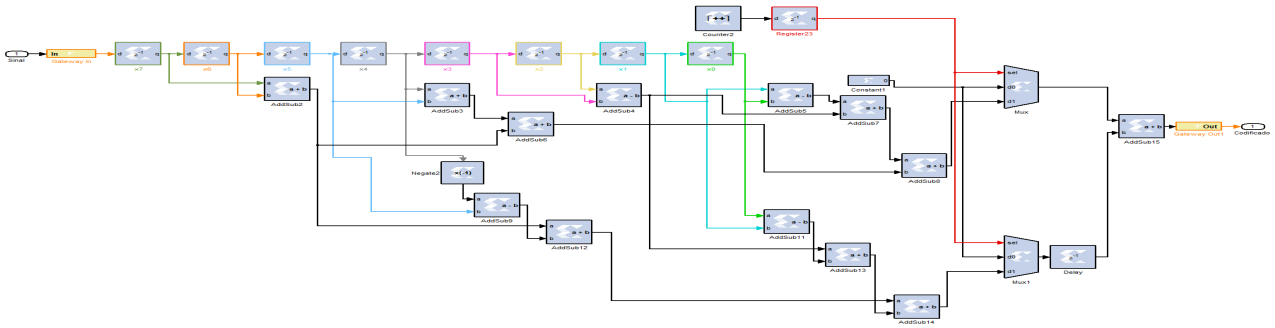


Figure 3: Implementation of wavelet encoder in Xilinx Platform.

4.1 Architecture of Wavelet Encoder

In the wavelet encoder architecture implementation was adopted a resolution of 5 bits on integer part and 0 bits on fractional part. This resolution has been analyzed previously to minimize the use of components of the FPGA. The implementation of the encoder adopted an architecture consists of three major modules, characterized as storage module, calculation module and output module of the encoder, as shown in Figure 4.

1. Storage Module (SM): This module is responsible for storing the bits generated by the source in a database comprised of eight registers in series. Initially the register values are null.

2. Calculation Module (CM):This module is responsible for performing mathematical operations required for wavelet coding, described below: Multiplication of the values stored in registers with their wavelet matrix equivalent weights, followed by the sum of these multiplications results. Calculations are performed in parallel and simultaneously sent to the next module. The matrix encoding used is based on a WCM dimensions with 2×8, defined by:

$$\mathbf{A} = \begin{pmatrix} a_0^0 & a_1^0 & a_2^0 & a_3^0 & a_4^0 & a_5^0 & a_6^0 & a_7^0 \\ a_0^1 & a_1^1 & a_2^1 & a_3^1 & a_4^1 & a_5^1 & a_6^1 & a_7^1 \end{pmatrix} \tag{8}$$

The calculations performed in this module are expressed in equations:

$$\begin{aligned} y_{n+1-m} = a_6^0 \cdot x_{n-7} + a_6^1 \cdot x_{n-6} + a_4^0 \cdot x_{n-5} \\ + a_4^1 \cdot x_{n-4} + a_2^0 \cdot x_{n-3} + a_2^1 \cdot x_{n-2} \\ + a_0^0 \cdot x_{n-1} + a_0^1 \cdot x_n \end{aligned} \tag{9}$$

$$\begin{aligned} y_{n+2-m} = a_7^0 \cdot x_{n-7} + a_7^1 \cdot x_{n-6} + a_5^0 \cdot x_{n-5} \\ + a_5^1 \cdot x_{n-4} + a_3^0 \cdot x_{n-3} + a_3^1 \cdot x_{n-2} \\ + a_1^0 \cdot x_{n-1} + a_1^1 \cdot x_n \end{aligned} \tag{10}$$

Functions defined for all n odd and may also be listed in Table I:

Table 1: Relationship in time between incoming bits and symbols wavelet encoded.

	1	2	3	...	$2g-1$	$2g$	...
x_0	$x_0 a_0^0$	$x_0 a_1^0$	$x_0 a_2^0$	...	$x_0 a_{2g-1}^0$		
x_1	$x_1 a_0^1$	$x_1 a_1^1$	$x_1 a_2^1$	...	$x_1 a_{2g-1}^1$		
x_2			$x_2 a_0^0$	$x_2 a_1^0$	$x_2 a_2^0$	...	$x_2 a_{2g-1}^0$
x_3			$x_3 a_0^1$	$x_3 a_1^1$	$x_3 a_2^1$	...	$x_3 a_{2g-1}^1$
$\vdots$					$\vdots$	$\vdots$	$\ddots$
	y_0	y_1	y_2	...	y_{2g-1}	y_{2g}	...

3. Output Module Encoder (OME): This module is responsible for implementing a port with selector function to select symbols received from CM when n is odd and discard when n is even. The module is also responsible for transmitting instantly the symbol y_{n+1-m} received from CM and delaying a clock unit symbol y_{n+2-m} to transmit it when n is even.

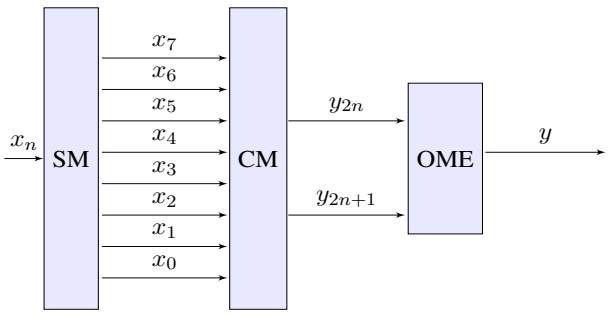


Figure 4: Model used for the wavelet encoder.

The encoder used in this paper will generate a delay of $m = 2$ units in the clock system. In Figure 3 is detailed the wavelet encoder platform implementation in Xilinx.

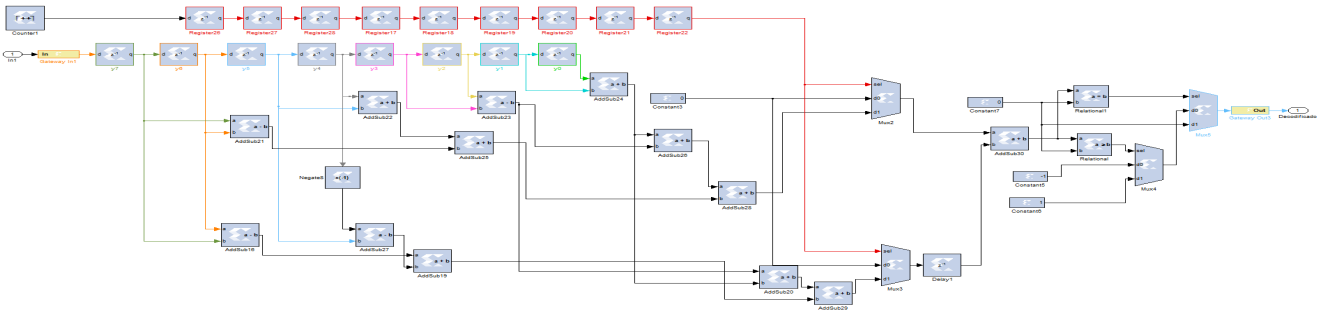


Figure 6: Implementation of the decoder on Xilinx platform wavelet.

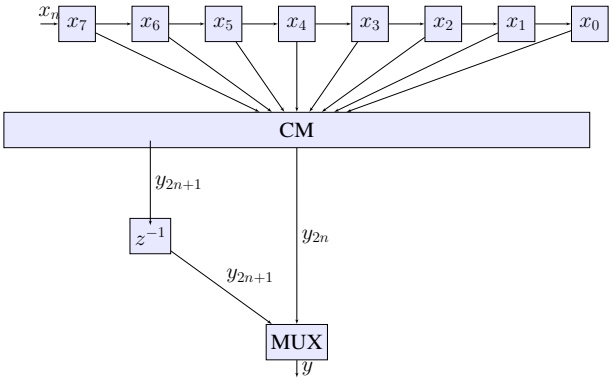


Figure 5: Details of SM and OME modules.

4.2 Wavelet Decoder Architecture

In the wavelet decoder implementation all variables and constants are using 7 bits in the integer part and 0 bits in the fractional part. This resolution was analyzed to minimize the use of FPGA components. The decoder implementation has adopted an architecture consisting of three major modules called: Module storage, calculation module and decoder output module.

1. Storage Module (SM): This module is responsible for storing the received symbols of the demodulator on a bench with eight registers in series. Initially the register values are null.

2. Calculation Module (CM): This module is responsible for performing mathematical operations required in wavelet decoding. The calculations performed are represented by the following functions:

$$\begin{aligned} x_{n-\tilde{m}+1} = a_7^0 \cdot y_n + a_6^0 \cdot y_{n-1} + a_5^0 \cdot y_{n-2} \\ + a_4^0 \cdot y_{n-3} + a_3^0 \cdot y_{n-4} + a_2^0 \cdot y_{n-5} \\ + a_1^0 \cdot y_{n-6} + a_0^0 \cdot y_{n-7} \quad (11) \end{aligned}$$

$$\begin{aligned} x_{n-\tilde{m}+2} = a_7^1 \cdot y_n + a_6^1 \cdot y_{n-1} + a_5^1 \cdot y_{n-2} \\ + a_4^1 \cdot y_{n-3} + a_3^1 \cdot y_{n-4} + a_2^1 \cdot y_{n-5} \\ + a_1^1 \cdot y_{n-6} + a_0^1 \cdot y_{n-7} \quad (12) \end{aligned}$$

Functions defined for all n odd.

These calculations are performed in parallel and are sent instantly to the next module.

3. Output Module Decoder (OMD): This module is responsible for implementing a port with selector function to select symbols received from CM when n is odd and discard when n is even. The module is also responsible for examining whether the symbol received is greater than zero, in this case with that $\tilde{x_n}$ is equal to 1. Otherwise, $\tilde{x_n} = -1$. This module requires a delay of 10 unit of clocks due delay coding.

5 Results

5.1 Methodology

In this work we used a methodology of co-simulation, with simulations performed simultaneously on platform Xilinx-System Generator and the platform MATLAB/SIMULINK. The wavelet system was investigated with two distinct demodulation metrics, that is, Euclidian and MMAP. It was used the constellation proposal in [3], is illustrated in Figure 7.

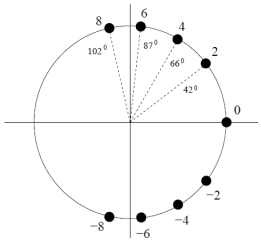


Figure 7: Constellation 9-PSK for WCM 2×8.

5.2 Validation of Results

In order to validate the proposed implementation of FPGA wavelet encoding two scenarios were analyzed. In the first scenario, the performance of the wavelet encoding is evaluated based on architectures implemented in platform Xilinx-System Generator with FPGA kintex7-xc7k325t. In the second scenario, the architecture of wavelet encoder and decoder were evaluated by simulation in MATLAB / SIMULINK. The two scenarios have the same input with $1.2 \cdot 10^6$ bits.

In both scenarios, the system was evaluated in terms of their bit error rate (BER). In this type of evaluation, it is expected that those systems with best performances show a lower bit error rate for a given rate of the signal to noise ratio. The Figures 8 and 9 illustrate the performance curves of the system with 2×8 and WCM Euclidean and MAP demodulation schemes. From these figures, we observe that the implementations performed on platforms SIMULINK and Xilinx reproduced similar performance curves, validating the wavelet encoder developed in FPGA. In addition, you can check that these performance results similar to the results already published in the literature for this system [3].

In Figure 9, we can also see that the system with wavelet coding and rule of demodulation MAP has superior performance to the system with Euclidean metric, illustrated in Figure 8. In particular, for a BER approximately equal to 10^{-3}, it can be seen that the system with rule MAP achieves a gain of approximately 5 dB in relation to system with decision Euclidean.

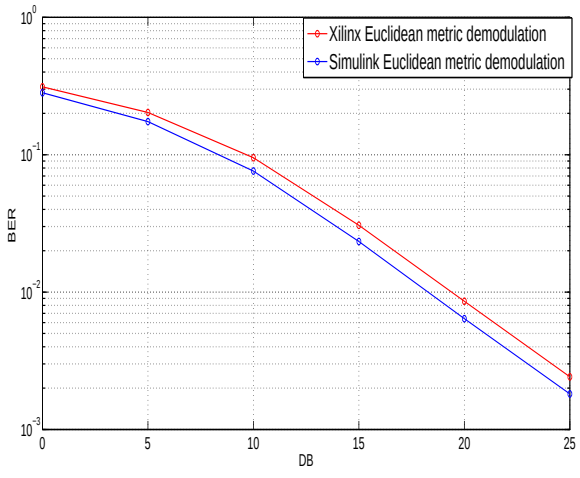


Figure 8: Performance curve with the Euclidean metric demodulation.

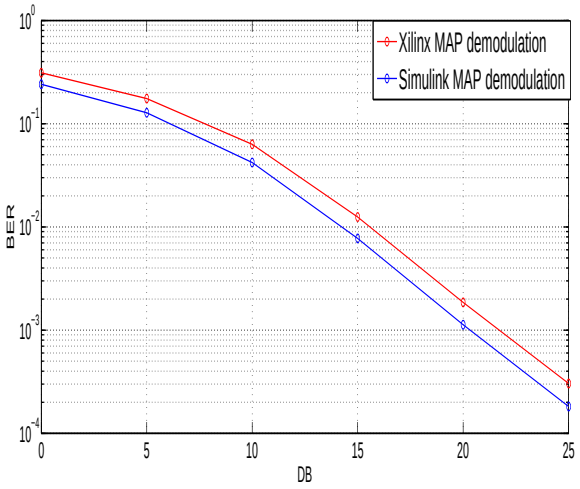


Figure 9: Performance curve with MAP demodulation.

5.3 Parameters of Hardware

After synthesizing the blocks for co-simulation in FPGA Kintex7, it was performed a resource estimate used in the implementation of the encoder and decoder wavelet. The result of this estimation and the total quantity of hardware resources used is illustrated Table 2.

Table 2: FPGA occupation for implementation of the wavelet coding.

	Encoder	Decoder	FPGA kintex7
Slices	78(0.15%)	125(0.25%)	50950
Flip-flops	47(0.01%)	73(0.02%)	407600
LUTs	86(0.03%)	139(0.04%)	326080
IOB	10(1.19%)	14(1.67%)	840

With the data shown in Table 2 we can perceive the low-cost hardware implementation of the system proposed in this paper. The encoder and decoder implemented used a clock with frequency of 1 MHZ. Finally, you can see that the hardware decoder cost is greater than the cost of the encoder, in function of the different resolutions of bits adopted in these architectures.

6 Conclusions

This study evaluated the implementation cost in hardware FPGA reconfigurable architectures for the encoder and decoder wavelet, in terms of occupation, resolution in bits and processing delay. The results indicate that this coding technique has a low implementation cost in terms of area occupation on the FPGA

board. It is also important to note that this encoding technique proved robust to the effects caused by the fading and additive white noise, even when implemented with low bit resolution. This robustness against fading wavelet coding, together with the low complexity in hardware, enables the use of the technique in different communication scenarios.

Acknowledgements: The author Felipe O. S. Gama thanks the ANP, MCT, FINEP and Petrobras for financial support through project PFRH-PB220.

References:

[1] CAVALCANTI, L. C. P. ; Fontes, A. I. R. ; Fernandes, M. A. C. ; SILVEIRA, L. F. Q.,"Performance Analysis of Wavelet Encoding in Frequency Selective Channels (in Portuguese),". In: XXXI Simpsio Brasileiro de Telecomunicaes-SBrT2013, 2013, Fortaleza - CE. Anais do XXXI Simpsio Brasileiro de Telecomunicaes, 2013.

[2] M. A. Tzannes and M. C. Tzannes, "Bit-by-bit channel coding using wavelets," *Proceedings of IEEE GLOBECOM'92*, pp. 684–688, Abril, 1992.

[3] SILVEIRA JUNIOR, L. G. Q. ; SILVEIRA, L. F. Q.,"Analysis of Bit Error Probability Systems with Wavelet Coding and Soft demodulation (in Portuguese)". In: 15 SBMO Simpsio Brasileiro de Micro-ondas e Optoeletrnica/MOMAG'2012, 2012, Joo Pessoa. Anais do MOMAG'2012, 2012.

[4] L. G. Silveira, L. F. Q. Silveira, F. Assis, and E. L. Pinto, "Soft-Decision Demodulation of Wavelet-Coded PSK Signals over Flat Rayleigh Fading Channels," in *ITS'2006 – VI International Telecommunications Symposium*, Setembro, 2006, Fortaleza-CE.

[5] H.Resnikoff and R.Wells, *Wavelet analysis: the scalable structure of information*, 1st ed., ser. ISBN 0-387-98383-X, Verlag, Ed. Springer, 1998.

[6] Fontes, A. I. R. ; CAVALCANTI, L. C. P. ; SILVEIRA, L. F. Q. "Novel Automatic Modulation Classification using Correntropy Coefficient,". In: XXX Simpsio Brasileiro de Telecomunicaes (SBrT'12), 2012, Braslia. Anais do XXX Simpsio Brasileiro de Telecomunicaes, 2012.

[7] SILVEIRA, L. F. Q. ; SILVEIRA JUNIOR, L. G. Q. ; ASSIS, F. M. ; PINTO, E. L., "Iterative Decoding for Serial Concatenation With Wavelet Encoding,". In: International Microwave and Optoelectronics Conference, 2007, Salvador. Proceedings of International Microwave and Optoelectronics Conference, 2007.

[8] L. F. Q. Silveira, L. G. de Q Silveira Jnior, F. M. Assis e E. L. Pinto, "Genetic Algorithm Applied in Obtaining Signal Constellations for Coding with Wavelet Coding for Rayleigh Fading Channels with (in Portuguese)" VIII Congresso Brasileiro de Redes Neurais - CBRN 2007, 2007.

[9] Ndzi, David L., et al. "An FPGA-based adaptable 200 MHz bandwidth channel sounder for wireless communication channel characterisation." International Journal of Reconfigurable Computing 2011 (2011).

[10] Hatai, Indranil, and Indrajit Chakrabarti. "A new high-performance digital FM modulator and demodulator for software-defined radio and its FPGA implementation." International Journal of Reconfigurable Computing 2011 (2011): 2.

[11] Jaquenod, Guillermo A., Javier Valls, and Javier Siman. "Efficient FPGA Hardware Reuse in a Multiplierless Decimation Chain." International Journal of Reconfigurable Computing 2014 (2014).

[12] Xilinx. Xilinx System Generator User's Guide. [Online]. Available: www.xilinx.com