Design of On-line Clock Jitter Fault Detection Circuit for Time-Error-Tolerant System

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Abstract: - One of the major obstacles encountered in design of a system on chip (SoC) arises from the high fault rate of clock distribution network in embedded intellectual property (IP) cores. With technology scaling, the geometries of devices approach its physical limits of operation, SoCs will be susceptible to various noise sources such as crosstalk, coupling noise, process variations, etc. Designing such a system under uncertainty becomes a challenge, as it is difficult to predict the time behavior of the system. Conservative design methodologies that consider all possible faults due to the noise sources, targeting safe system operation under all conditions will cause poor system performance. By contraries, aggressive design approach that can provide resilience against such timing faults without much additional hardware, is toughly required for maximizing system performance.

In this paper we present an aggressive method to on-line detect the jitter faults on the clock signal that are due to defects caused by noise for high speed SoCs. Only fourteen MOS transistors and two minor capacitors are used for the circuit. The technique of time-to-voltage conversion is employed for transforming the time jitter error to variable voltage, which is more convenient in contrast with the conservative clock fault tolerance structure methodology. The circuit proposed can detect the jitter error of the digital clock signal faults with different applications. We have formally evaluated the meta-stability of our technique, which shows that our technique reliably meets the timing requirements. The simulation-based results show that the proposed circuit can be integrated into the nano-electronic SoCs applications to achieve the on-line clock jitter fault detection, and its maximal frequency can reach 800MHz. Furthermore, fault injection experiments show that our technique can tolerate all single faults on clock sources that lead to permanent stuck-at fault and masks almost 49 percents of intermittent faults.

Key-Words: - Clock fault, On-line detection, Time-to-voltage conversion

1 Introduction

As shrinking feature sizes and increasing transistor density, the number of functional cores on a chip and their operational speed are increasing [1]. In future SoCs, communication between the functional cores and processes will become main bottleneck in system performance, as the current bus-based communication architecture is inefficient throughput, latency and power consumption [2-4]. Scaling of transistors is accompanied by a decrease in supply voltage and an increase in clock rate makes wires unreliable as the effect of various noise sources (such as crosstalk, process variations and coupling noise, etc.) increases [5][6]. In particular, clock signals have to maintain correct duty-cycle, limited skew, jitter, and sharp edges. It is becoming progressively more difficult to achieve this.

In SoCs, the transaction and communication of information is controlled critically by a periodic clock. Due to the uncertainty of the clock wires in future SoCs, the reliability of the clock is becoming more important. As shown in Fig.1, a typical SoC consists of bus devices (such as switches, links), computational elements (such as CPU or DSP cores), logic elements (LEs) and other in-system-devices (IDEVs). Data for DSP/CPU are read in from the memory or the other module (such as LEs or IDEVs) under the driving of system clock [7]. When the data are processed, they will be sent to the destination with clock synchronization. If faults occur in clock signal, the whole system will be in disorder.

To make the clock signal operate reliably in the conditions of permanent manufacture defects and transient signal faults many new fault-tolerant hardware clock synchronization methods were proposed in literature. The most notable in these studies includes Von Neumann [8]. Techniques such

as N-tuple modular redundancy (NMR) [8], Triple Modular Redundancy (TMR) [9], NAND multiplexing [10] and others based on reconfigurable hardware [11], error-correction coding techniques [12] have also been proposed in the literature.

Recently, generalized likelihood ratio test (GLRT) [13] becomes new points to resolve the faulty in atomic clock signal which can reveal frequency jumps and variance changes in clock signal. Phase locked loop (PLL) [14] and delay locked loop (DLL) [15] are also employed for clock fault detection in nano-system, which duplicates the aimed clock signal with fixed latency of one clock cycle. With phase selection circuits and a start-controlled circuits, these two technology can enlarge the operating frequency range and eliminate harmonic locking problems while detect fault in clock signal. Concatenating broadside tests [16] is used to deal with delay faults and some transition fault in time error systems. Paper [17] employs testability evaluation method to detect crosstalk faults in digital circuits which can also detect the crosstalk in clock signal.

Nevertheless, these methodologies described in literature use extensive hardware redundant circuit, and sometimes employ software to resynchronize the clock periodically, so these clock fault detection techniques waste much chip area. Furthermore, these fault tolerant designs are mainly for combinatorial circuits but not little sequential logic circuits. Therefore, an effective of clock signal fault detection methodology is critical for designing both combinatorial and sequential SoC circuits.

In this paper, we propose a novel on-line clock jitter fault detection topological structure which consist fourteen MOS transistors and two minor capacitors. We emphasize on time-to-voltage conversion, which transforms clock jitter error to deviation of voltage. The proposed circuit can detect the jitter error of the digital clock signal for different applications within operation frequency 800MHz.

This paper is organized as follows: Section 2, model for synchronous operation with a common clock in SoCs is reviewed. Section 3, the novel on-line clock jitter fault detection architecture of synchronous system is presented and the clock fault detection circuit based on 0.18μm standard CMOS technology is demonstrated. Section 4, the detection capacity of proposed circuit is shown by simulation. Finally, conclusions are made in the end of this paper.

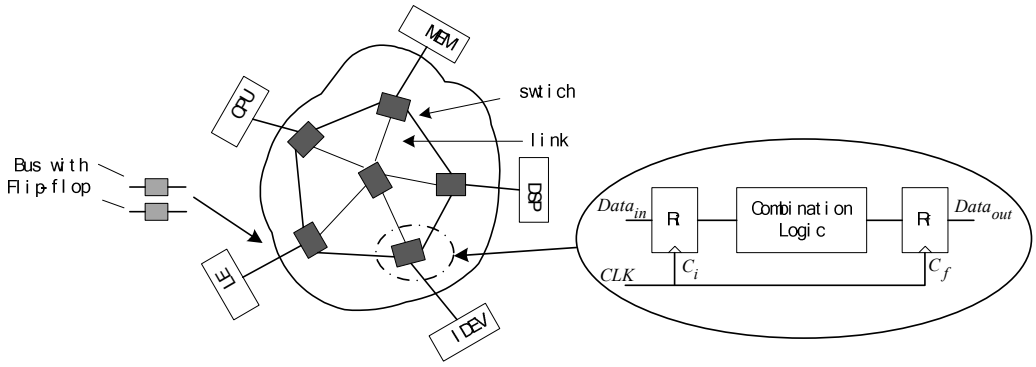


Fig.1 A typical SoC architecture and data flow

2 Model for synchronous operation with a common clock in SoC

2.1 Notations and Statement of Problem

There are many different defects with practical clock signal in high performance SoCs for real-time applications such as continuous clock with temporary stoppage, clock slowing down, temporary short or long pulse, long traveling path and so on. Generally these clock faults are divided into two major types: clock jitter and clock skew.

In SoCs, data are driven by the clock signal within system. Synchronization errors caused by clock fault can be classified in three categories, as illustrated in Fig. 2. In these cases where a common clock feeds all subsystems under consideration, only cases (b) (but with the condition that when clock jitter error rate within error tolerance threshold as described next part) and (c) are applicable. Case (c) in Fig. 2 illustrates the fully synchronous case for two subsystems, where both subsystems switch simultaneously. Case (b) shows the situation of two subsystems with identical clocks, where clock signal reaches the two subsystems at different times caused by clock jitter. Case (a) shows the switching sequence that resulted from clock jitter [18].

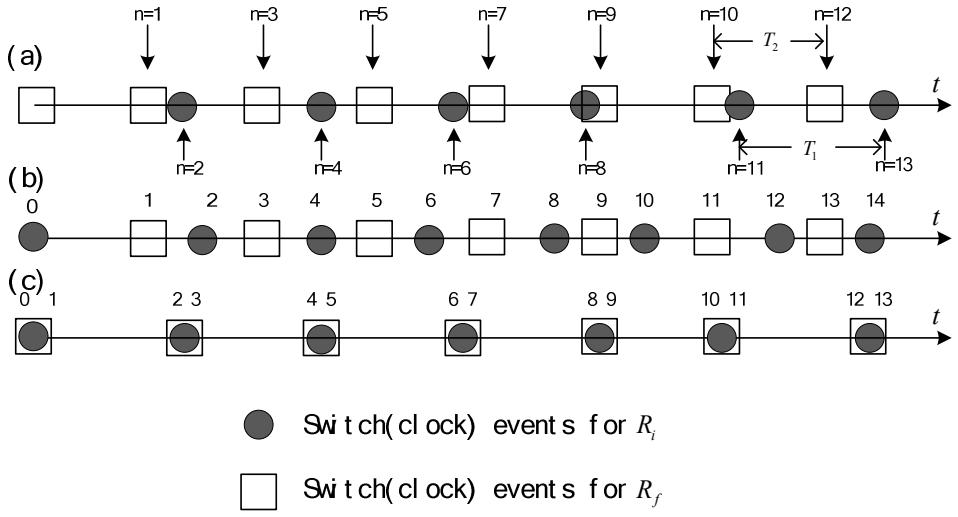


Figure 2. Time index and switching events for the three cases: (a) $T_1 > T_2$, (b) $T_1 = T_2$ with phase error in clock signal (jitter or skew), (c) $T_1 = T_2$ without phase error

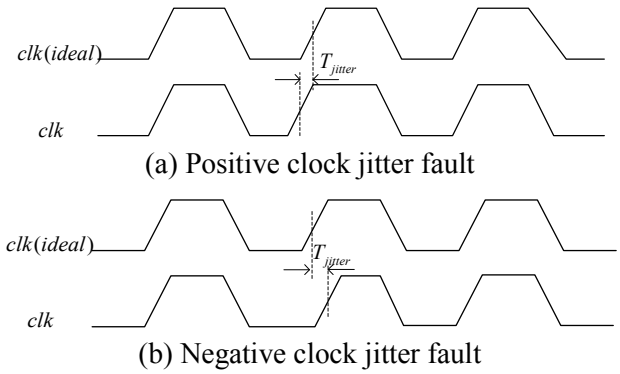
2.2 Mechanisms of clock faults

When there are different loads or distances on the clock distribution roadway, the time of each clock arriving to the trigger is different and the clock will drift apart from the other clock after some time. This clock drift and error sometimes can be avoided by circuit optimization and design. Clock jitter is always caused by the uncertain factor of PLL and clock deviation. Certainly the clock jitter can not be avoided because the uncertain effects are not predicted accurately. As the power supply voltage becomes lower and lower, especially in the complex clock distribution system, the noise and cross-talks affect the clock jitters more and more obviously. The clock fault tolerance through redundancy must be applied in the synchronous system to reduce the affect of clock jitter.

As mentioned before, in SoC, a synchronize system, when clock jitter happens and propagates, the system will be in disturb and operation in abnormal state, in next part we will analysis the fault caused by clock jitter.

2.3 Evaluation of clock jitter probability

An ideal clock waveform has positive pulse width W_p and pulse period W ($W = 2W_p$, when duty cycle is 50%). If clock pulse width deviates from the predetermined value for uncertain reason which referred previous part then these kinks of clock signal can be labeled as faulty clock signal with jitter. Use Fig. 3 as example, the clock waveform can be regarded as "positive clock jitter" if the negative clock pulse width is $0 < w_n < \alpha W$ ($0 < \alpha < 0.5$), where α is the preset positive threshold value of faulty clock. Vice versa, the clock waveform is regarded as "negative clock jitter" if the negative clock pulse width is $0.5 < w_n < \beta W$ ($0.5 < \beta < 1$), where β is the preset negative threshold value of fault clock.



(a) Positive clock jitter fault

(b) Negative clock jitter fault

Fig. 3 Example of clock jitter faults

We construct our clock jitter fault model using a clock with stable frequency but with a pulse width that varies with a normal (ideal) distribution with mean w_s and standard deviation σ. The probability distribution function (PDF) of the distribution can then be described as:

$$f(w)=\frac{1}{\sigma\sqrt{2\pi}}\exp\left(-\frac{(w-w_s)^2}{2\sigma^2}\right) \quad (1)$$

Thus, the cumulative distribution function (CDF) can be derived to be:

$$P(W\le w)=\frac{1}{2}\left(1+erf\left(\frac{w-w_s}{\sigma\sqrt{2}}\right)\right) \quad (2)$$

where w is a random variable of pulse width.

When the positive clock jitter happens, the probability of a clock error P_{error_p} can then be expressed using the following formulate:

$$P_{error\_p}=P(0<w<\alpha w_s)=\frac{1}{2}\left(erf\left(\frac{\alpha w_s-w_s}{\sigma\sqrt{2}}\right)-erf\left(\frac{-w_s}{\sigma\sqrt{2}}\right)\right) \quad (3)$$

Corresponding, when the negative clock jitter happens, the probability of a clock error P_{error_n} can then be expressed using the following formulate:

$$P_{error\_n}=P(0.5<w<\beta w_s)=\frac{1}{2}\left(erf\left(\frac{\beta w_s-w_s}{\sigma\sqrt{2}}\right)-erf\left(\frac{0.5w_s-w_s}{\sigma\sqrt{2}}\right)\right) \quad (4)$$

Having established a methodology to distinguish between faulty and non-faulty clock signals, and to map clock distribution to clock error probabilities, we set out to make out our proposed architecture.

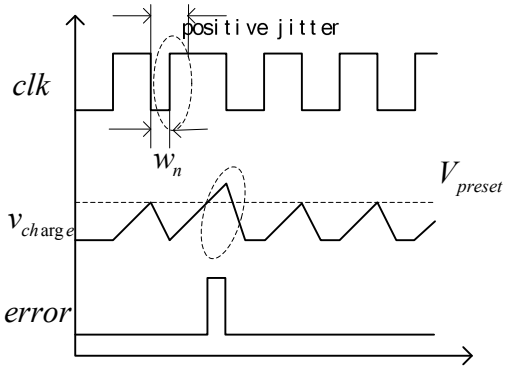
3 Design of the proposed on-line clock jitter fault detection circuit

3.1 Design of the proposed on-line clock jitter fault detection circuit

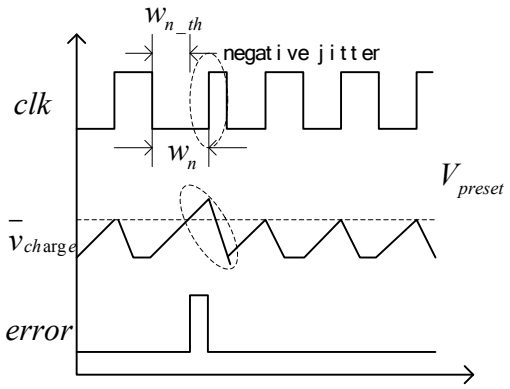
Under normal operation, it is difficult to detect the clock jitter without reference (ideal) clock signal, so it is important to form a reference electronic parameter for expressing the clock time variety. In this methodology, the clock signal is transformed to the variable voltage by using the clock signal to control the charge or discharge of corresponding capacitor. The distribution of clock is changed to distribution of voltage value on the corresponding capacitor which is more convenient to be distinguished and detected.

Fig. 4 shows the voltage variety of the capacitor with normalized practical clock. If negative clock pulse is too short that $0<w_n<w_{p\_th}$, then clock jitter will cause a type of error which we call it as "positive clock jitter error" (shown in Fig. 4(a)). In this case the duration of positive pulse is too long that charge the capacitor more time than normal clock signal, as a result, the voltage of the capacitor will be higher than V_{th_preset} and a positive clock jitter error signal will be triggered. On the other hand, If the negative clock pulse is too long that $w_{n\_th}<w_n<W$, the clock jitter will cause an type of error which we call it as "negative clock jitter error" (shown in Fig. 4(b)). In this case the duration of negative pulse is too long that charge the capacitor more time than normal clock signal, as a result the voltage of the capacitor will be higher than V_{th_preset} and a negative clock jitter error signal will be triggered

In this paper, the discharge current is larger than the charge current to make discharge time enough to set the capacitor voltage to zero at the beginning of each clock cycle. The detection circuit compares the voltage of the capacitor with the preset value, if the voltage of the capacitor is higher than preset value, a clock jitter error will be detected. The preset value can be set to the threshold voltage of MOSFET, which can simplify the detection circuit. To adjust the charge current or the capacitor, we can also change the trigger voltage of the detection circuit.



(a) Positive clock jitter error



(b) Negative clock jitter error

Fig. 4 The voltage variety of the capacitor under the condition of the clock jitter faults

To make our methodology more adaptive, the best values of the charge current and the capacitor should be modified when the clock frequency changes. Equation (5) gives the relations of the voltage, the charge current and the capacitor. For example, when the preset value of the threshold voltage is 0.5V $\alpha = 0.45$ (or $\beta = 0.55$) the clock frequency is 500MHz, the best parameter of I/C from the calculation is 5.0×109(A/F).

$$V(t) = (V(0) + \frac{I(t) * t}{C})(\frac{\alpha}{0.5})$$
$$(\text{or } V(t) = (V(0) + \frac{I(t) * t}{C})(\frac{1-\beta}{0.5}) \text{ }) \qquad (5)$$

3.2 Block diagram of proposed circuit

The key point of the proposed clock jitter detection topology is the time-to-voltage converter and the detection for range of voltage which stands for clock signal. Fig. 5 shows the block diagram of the clock jitter fault detection circuit.

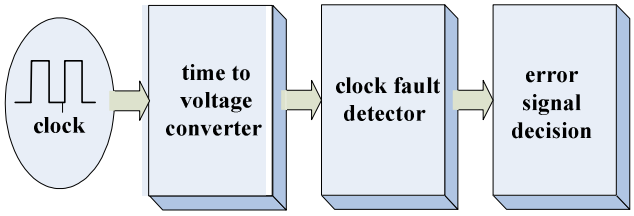


Fig. 5 Block diagram of the on-line clock jitter fault detection circuit

This circuit consists of three parts: time-to-voltage converter; clock jitter fault detection and the error signal decision circuit. Under normal operation, the time-to-voltage converter keeps its voltage level less than preset values and it will not trigger the clock jitter fault detector. If the periodic clock signal behaves abnormally (clock jitter error happens), the voltage of the time-to-voltage converter will exceed the threshold voltage of the clock fault level detector, and then the clock-fault detector sends out a signal to clock error decision block. The decision part with a simple OR gate then sends a warning signal to following part of SoC.

3.3 Circuit Implementation

The clock jitter fault detection circuit in 0.18μm CMOS technology is shown in Fig. 6. For clock signal contains positive jitter error and negative jitter error, the clock fault detection circuit must handle these two kinds of errors respectively. The time-to-voltage converter part only consists of three inverters and two minor capacitors. The inverters M1 and M2 supply the charge and discharge current to the capacitor C1 and C2 respectively. The clock fault detection and error signal decision logic only consists of two inverters and one OR gate. The whole circuit is simple but it can detect the clock jitter error of the high speed digital clock signal.

When the clock signal is at positive half cycle, capacitor C1 charges through the inverter M1, meanwhile, C2 discharges through the inverter M2. If the positive half cycle time of the clock signal is longer than the normal range (which is the condition that positive clock jitter happens, as shown in Fig. 4(a)), the voltage of C1 will higher than the threshold voltage of M3, and then the error signal will become high which means that the clock fault occurs.

When the clock signal is at negative half cycle, capacitor C2 charges through the inverter M2, at the same time C1 discharges through the inverter M1. If the negative half cycle time of the clock signal is longer than the normal range (which is the condition that negative clock jitter happens, as shown in Fig. 4(b), the voltage of C2 will higher than the threshold voltage of M4, and then the error signal will be high which means that the clock fault occurs.

4 Experimental results and analyses

To show the performance of our proposed design, we have implemented the whole circuit in TSMC 0.18um CMOS process technology and simulated by Hspice software. The simulation based results can demonstrate on-line clock-jitter fault detection capability.

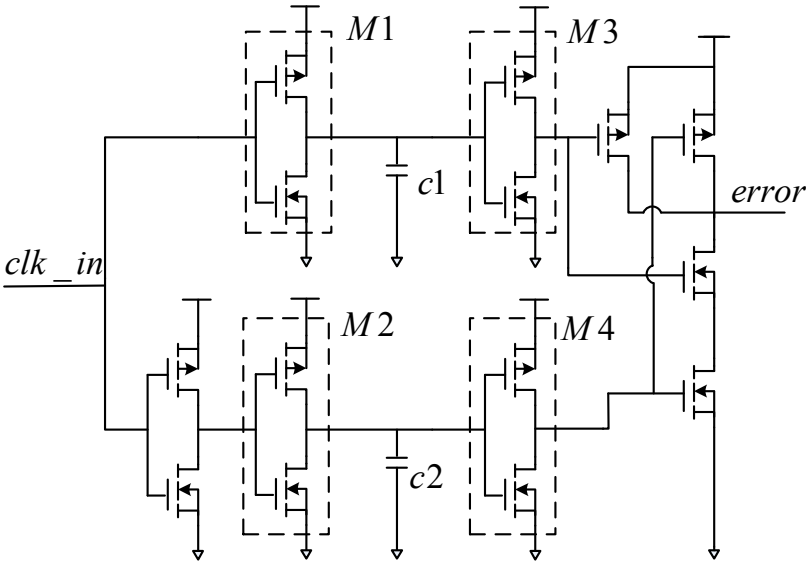
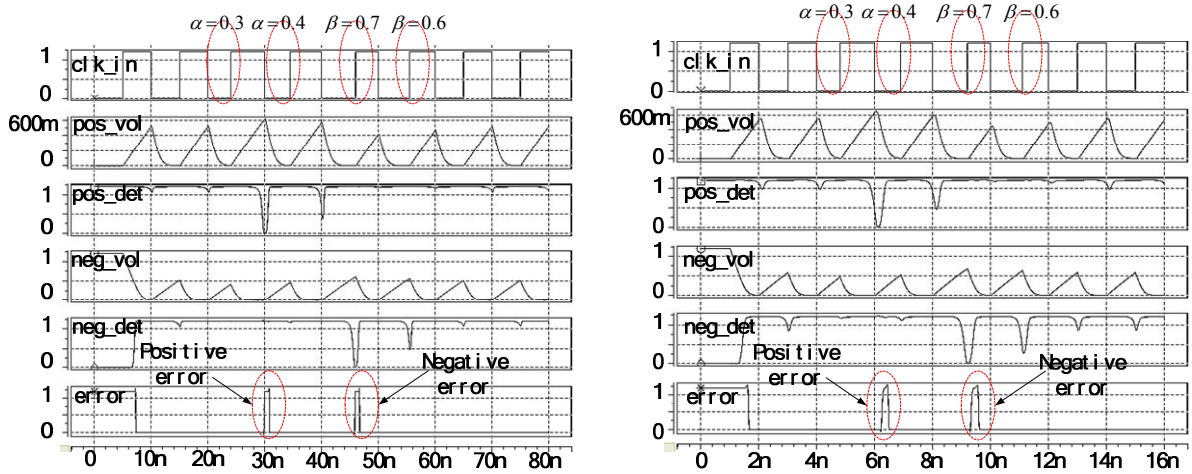


Fig. 6 Implementation of clock jitter fault detection circuit in 0.18μm CMOS technology

4.1 Experiments on operation frequency

We firstly test the operation frequency of the proposed clock jitter fault detection circuit. The maximum operation frequency can as high as 800MHz, as shown in Fig. 7 and Fig. 8.When the clock signal has jitter error, the waveform of circuit work status is shown in Fig. 7 ($f = 100MHz$ and $f = 500MHz$, error tolerance threshold is 15%). Suppose that we regard when jitter time is more 15% ($\alpha < 0.35$ or $\beta > 0.65$) as an error clock signal, so when $\alpha = 0.3$ or $\beta = 0.7$ the positive error signal or negative error signal would occur. And when $\alpha = 0.4$ or $\beta = 0.6$, the detect circuit regards clock signal with jitter as a normal signal.

When the circuit works under operation frequency 500MHz, the detect delay time is about 0.2ns.



(a) Operation frequency is 100MHz (b) Operation frequency is 500MHz

Fig. 7 Waveforms of the proposed circuit when detect error threshold is 15%

Fig. 8 shows the waveform that operation frequency is 1GHz. The proposed circuit fails to detect positive jitter error when $\alpha = 0.3$.

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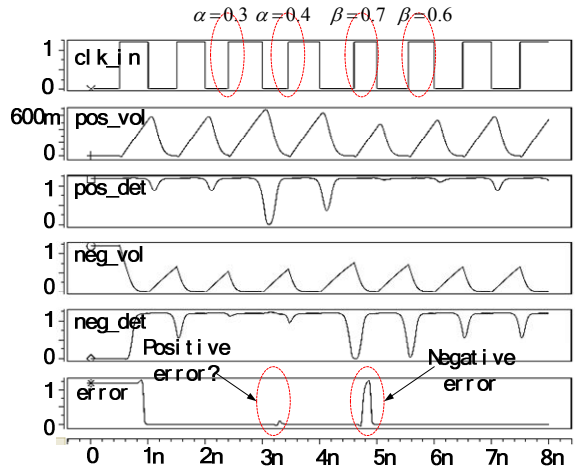


Fig. 8. Waveforms of the proposed circuit when operation frequency is1GHz and detect error threshold is 15%

The circuit work status with different frequency ($\alpha = 0.3$ and $\alpha = 0.7$) is shown in Fig. 9. The circuit can detect clock jitter error when the frequency is below 820MHz with minor error rate. However when operation frequency is higher than 850MHz the error rate become unacceptable.

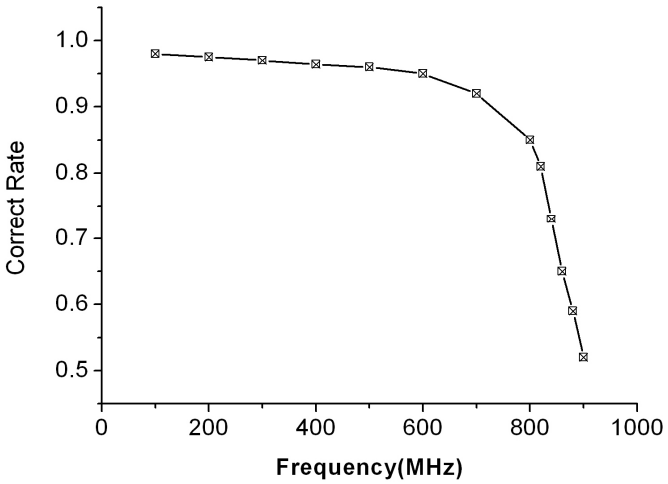


Fig. 9 Work status with different frequency

4.2 Experiments on error threshold

Fault tolerance of SoC with clock jitter varies in different applications, so it is necessary to make our design adoptive to corresponding requirements. In this part we use the operation frequency 500MHz for instance to illustrate adaptability of proposed circuit.

With equation (5), we can get:

$$f = \frac{i(t)}{(v'(t) - V(0)) * C} \quad (6)$$

where $v'(t) = \frac{0.5 * v(t)}{\alpha}$ or $v'(t) = \frac{0.5 * v(t)}{(1-\beta)}$.

Equation (6) can be rewritten as $f = \frac{i(t)}{v'(t) * C}$ if $V(0) = 0$. When the voltage of capacitor is higher than V_{th} (threshold voltage of the inverter) thus an error signal triggers, and a clock jitter error detects. It can be changed the value of charged and discharged capacitors to make our design adaptive to different operation frequency.

Fig. 10 shows the cases that we change value of capacitors to get different fault tolerance of clock jitter.

In Fig. 10, when the clock jitter time is more then preset value such as 5% (shown in (a)), the clock error occurs. On the other hand, when the clock jitter time is less then preset value, the detect circuit consider this kind of clock jitter as an acceptable fault.

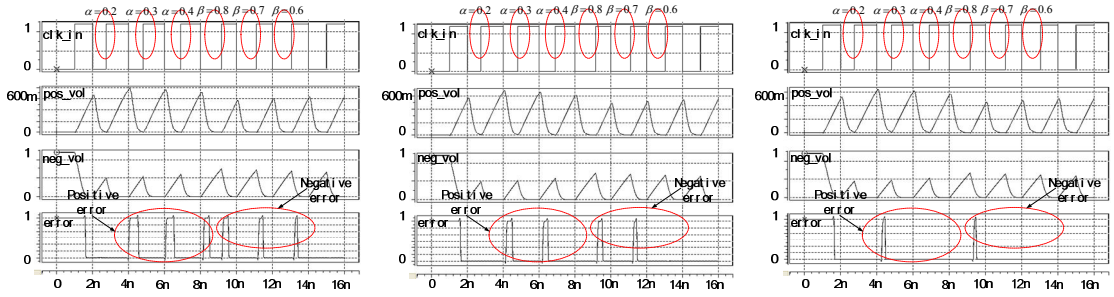
Fig. 11 shows the relationship between error tolerance threshold and capacitor value when the operation frequency is 100MHz, 500MHz and 800MHz. The curve of capacitors and operation frequency is mainly in accordance with

$$c = \frac{i(t)}{f * v_{th}} = \frac{I_{fixed}}{f_{500MHz} * V_{TH} * (1-\alpha)} \left(or \frac{I_{fixed}}{f_{500MHz} * V_{TH} * (1-\beta)}\right)$$

.

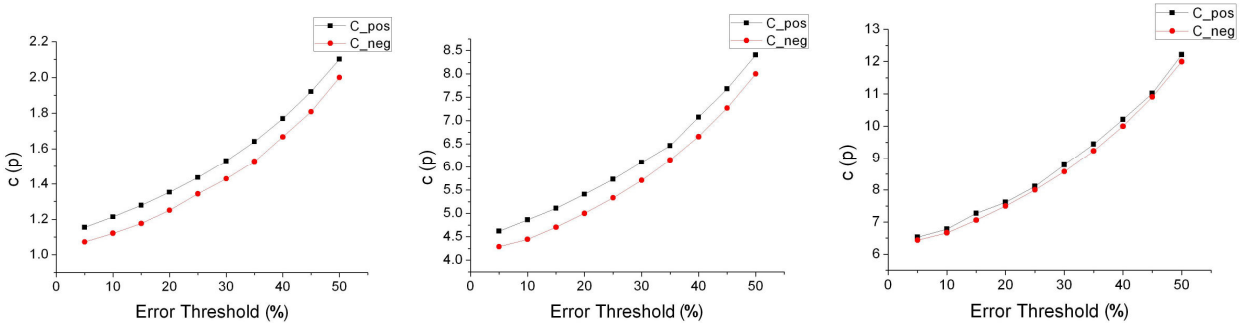
5 Conclusion and discussion

Clock integrality and regularity have been affected deeply with the development of IC manufacture technology and complicated SoCs. To improve the clock signal performance and detect the clock jitter fault on-line, which will increase the reliability of high speed nano-electronic digital ICs or SoCs, a novel on-line clock jitter fault detection circuit is



(a) Error threshold is 5% (b) Error threshold is 15% (c) Error threshold is 25%

Fig. 10. Waveforms of the proposed circuit when operation frequency is 500MHz with different detect error threshold



(a) $f = 100MHz$ (b) $f = 500MHz$ (c) $f = 800MHz$

Fig. 11 Relationship between capacitors and detect error threshold with different operation frequency

presented on the principle of the time-to-voltage conversion. The simulation-based results show that this circuit can effectively detect the clock jitter errors for different SoC applications. The maximal clock frequency of the circuit can be 800MHz and it is appropriate for high speed SoCs

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Appendix

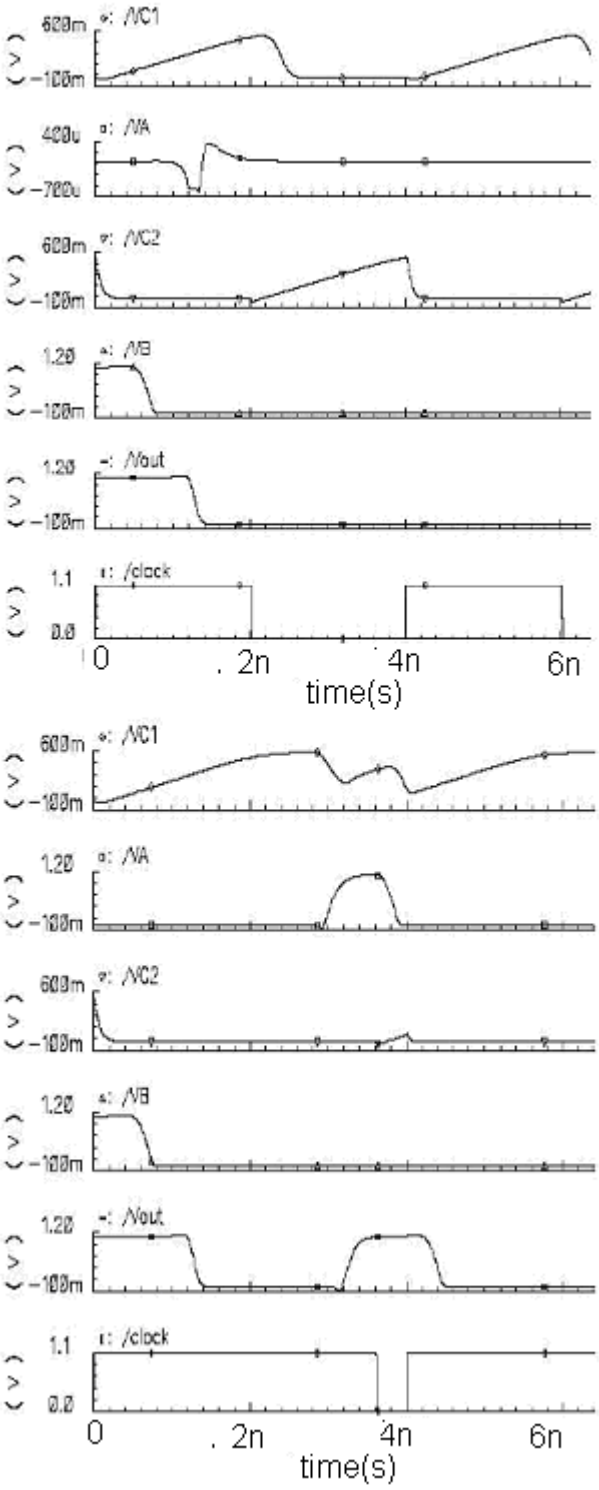

Fig. 12 Full waveforms of the proposed circuit when operation frequency is 500MHz and detect error threshold is 20% (positive jitter error)

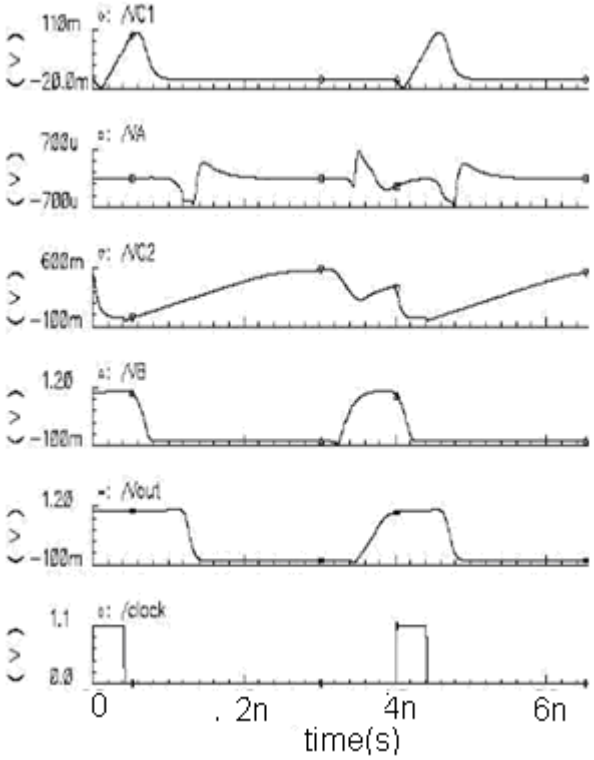

Fig. 13 Full waveforms of the proposed circuit when operation frequency is 500MHz and detect error threshold is 20% (negative jitter error)