A Novel CMOS 1-bit 8T Full Adder Cell

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Abstract: The 1-bit full adder is a very important component in the design of application specific integrated circuits. Demands for the low power VLSI have been pushing the development of design methodologies aggressively to reduce the power consumption drastically. In most of the digital systems adder lies in the critical path that affects the overall speed of the system. So enhancing the performance of the 1-bit full adder cell is the main design aspect. The present study proposes a novel CMOS 1-bit full adder cell with least MOS transistor count that reduces the serious problem of threshold loss. It considerably increases the speed and also proves best for high frequency applications. Result shows 45% improvement in threshold loss problem and considerable reduction in power consumption over the other types of adders with comparable performance. The simulation has been carried out on Tanner EDA tool on BSIM3v3 90nm and 130nm technologies.

Key words: Full adder, high speed, low power, power-delay product, XOR gate, VLSI.

1 Introduction

The full adders form the basic building blocks of all digital VLSI circuits. The considerable improvement have undergone at very high pace. The main motto behind such blinding pace are being motivated by three basic design goals, viz. minimizing the transistor count and the power consumption and increasing the speed of operation. The full adder performance affects the system as a whole. A variety of full adders using static or dynamic logic styles have been reported in the literature [1]-[8]. To meet the growing demand, we propose the new high speed and energy efficient full adder cell using 8 transistors (least number of transistors) that yielded very encouraging results, so to say, the best in speed, power and threshold loss in comparison to other adders using transistor count of 10, 14 and 16 [1],[3],[4],[5].

The adder has been designed using 90nm and 130nm technologies to establish the technology independence. Simulation results indicate that the proposed 8T full adder cell operates at high speed and has low power dissipation than its peer designs.

The rest of the paper is organized as follows: In Section II, we briefly describe the previous work reported in the literature. In Section III, we propose the new 8T full adder cell. In Section IV, we present the simulation results and we draw the conclusions in Section V.

2 Previous Work

The survey of the contemporary literature reveals very wide spectrum availability of adder designs over the past few decades. Several designs of low power and high speed adder cells can be found in the literature. The full adder cell realization of the circuit using 28T (conventional full adder) [7] is shown in Fig.1.The CMOS structure combines PMOS pull-up and NMOS pull-down network to produce considered output. It has the advantage of full output voltage swing i.e.; it does not suffer from the threshold loss problem. The drawback of this circuit is that it acquires large silicon area and also consumes much power. Therefore it is not suitable for low power and area efficient applications

Using lower number of transistors to implement a logic function is beneficial in reducing the number of components and interconnect parasitic and reducing the chip area, resulting in lower time delay and potentially lower power consumption. There is wide spectrum of such adder designs available in the literature. The full adder cell realization of the circuit using 16 transistors [1] is shown in Fig.2.

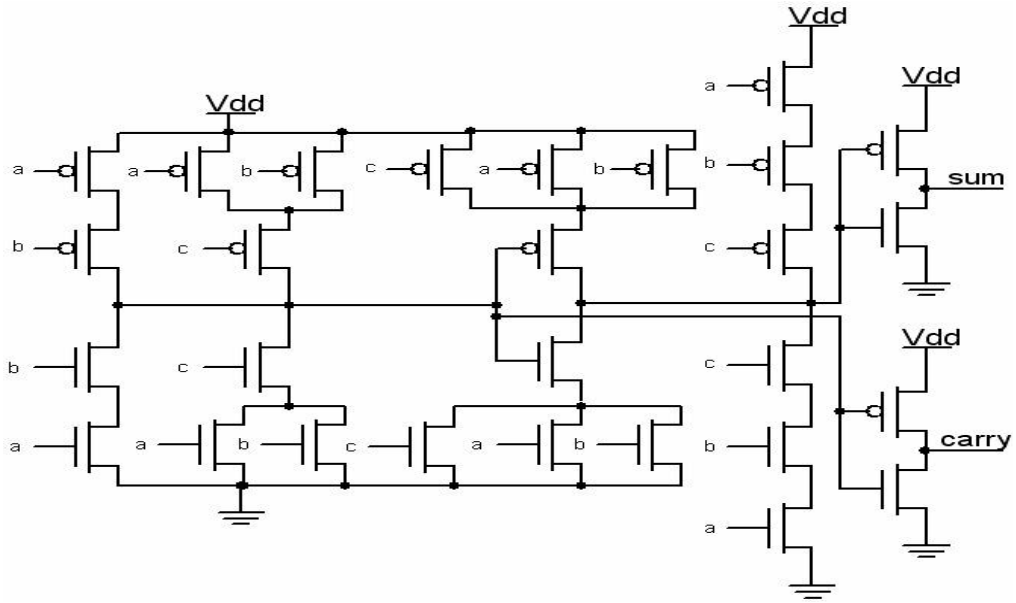
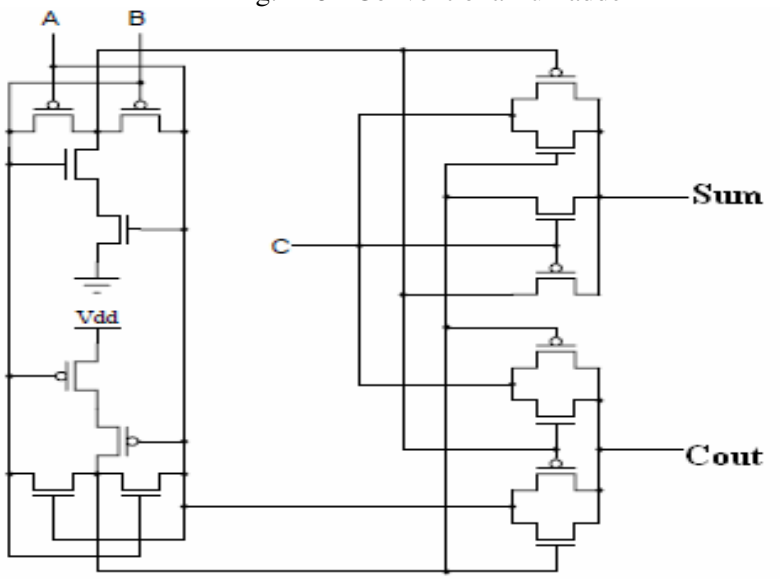


Fig.1 28T Conventional full adder

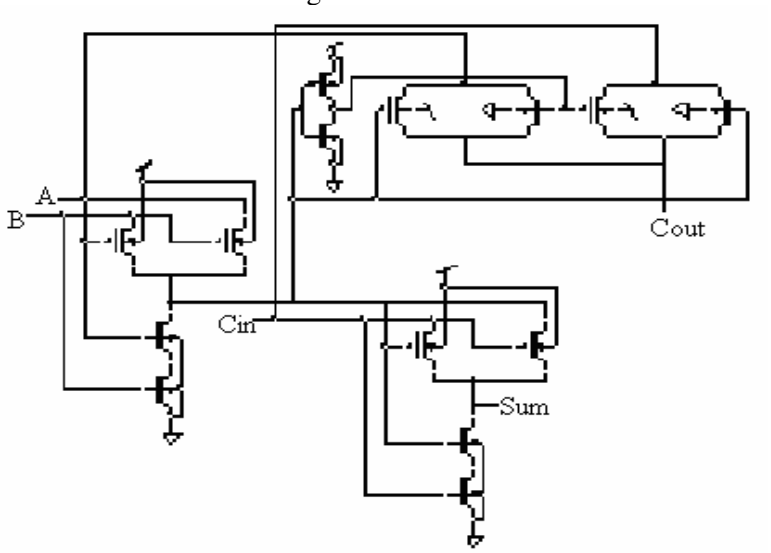


(W/L)n=1/1 and (W/L)p=2.5/1

Fig.2 16T full adder

This circuit can operate with full output voltage swing but consumes significant amount of power and have more delay compared to other adders having less transistor count. It uses 4-transistor powerless XOR gates and XOR gate implemented by transmission gates. It is reported in literature that this circuit shows better performance in comparison to 16T TFA. It has high speed and low power than 16T TFA circuit. A 16-transistor full adder was proposed to minimize the short circuit power dissipation of 14-transistor full adder but it acquires more area than 14T full adder. With the aim of further minimizing the number of transistors, pass transistor logic based XOR and XNOR circuits [2] were used and as a result the 14T full adder circuit of Fig.3 was designed. The Sum is implemented by inverter-based 4T XOR gates and Cout is implemented by XOR gate using transmission gates. . It shows the better performance in speed and power dissipation as compared to the other 14T full adder circuits stated in the literature. Also this circuit among all 14T full adder circuits [3],[4] shows the better

results for delay as compared to 16T full adder but it suffers from the threshold loss problem of approximately 0.4v. It works well in high performance multipliers with low power consumption.



(W/L)n=1/1 and (W/L)p=2.5/1
Fig.3 14T full adder

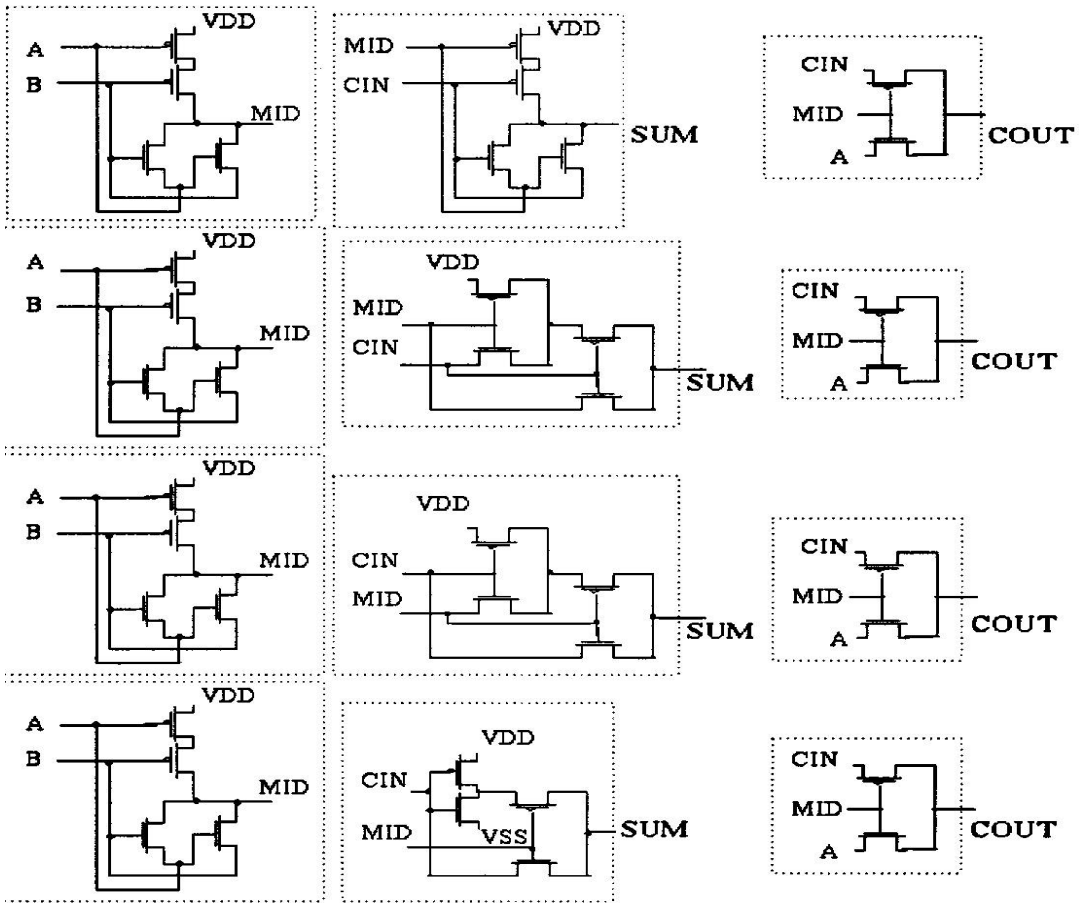


Fig.4 Construction Modules to Build Various Adders

The further reduction in transistor count while designing the full adder circuit results in a 10-transistor full adder cell. The literature reveals that in total we can construct 42 different types of 10-transistor full adder circuits. The construction modules to build various 10T full adders are depicted in Fig.4.

The further designed 10T full adder cell [5] of Fig.5 uses Inverter-based 4T XOR gates in their design and shows remarkable improvements in power and delay. It also reduces the silicon area. This reveals better performance than the other 10T adder cells [5]. The drawback of this circuit is that it also suffers from threshold loss problem of 0.35v approximately equal to 14T adder circuit.

3 Proposed 8T Full Adder

This design of proposed full adder is based on three transistor XOR gates. It acquires least silicon area. The power dissipation of the 3T XOR gate is slightly more than that of the 4T XOR gate. 3T XOR gate has much less delay than 4T XOR gate so that it has a much less power-delay product. The noise margin of the 3T XOR gate is also better than the 4T XOR gate.

The design of 3T XOR gate is shown in Fig.5. The heart of the design is based on a modified version of a CMOS inverter and a PMOS pass transistor. When the input B is at logic high, the inverter functions like a normal CMOS inverter. Therefore the output A XOR B is the complement of input A. When the input B is at logic low, the CMOS inverter output is at high impedance. However, the PMOS pass transistor is enabled and the output A XOR B gets the same logic value as input A.

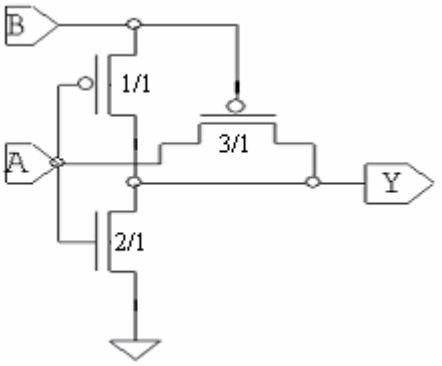


Fig.5 Design of 3T XOR gate

The operation of the circuit shown in Fig.5 is thus like a 2 input XOR gate. However, when A = 1 and B = 0, voltage degradation due to threshold drop occurs across PMOS pass transistor and consequently the output A XOR B is degraded with respect to the input. The voltage degradation due to threshold drop can be considerably minimized by increasing the W/L ratio of pass transistor.

The basic architecture of the 8-T full adder, consisting of 3 modules, is shown in Fig.6. If the module-1 and module-2 are XOR or XNOR gates, then the choices of module-Cout are shown in Fig.7 (a) and Fig. 7(b) respectively. Hence, we get a total of 6 new 8-T full adder cells as shown in Table I, all having a delay of 2T. However, in this work, only adder 3 shown in the table is considered for the purpose of comparison.

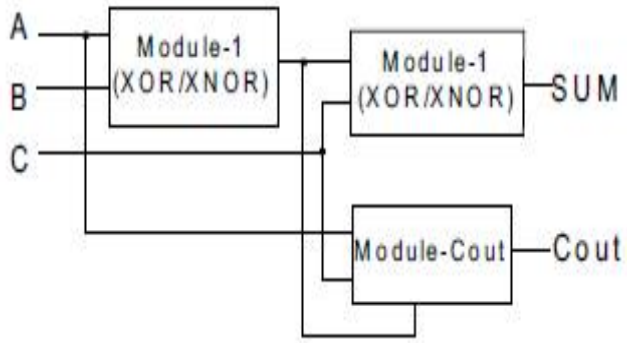


Fig.6 Architecture for 8T full adder

Adder	Module-1	Module-2	Module-Cout
1	3-T XOR	3-T XOR	Multiplexer
2	3-T XOR	3-T XOR	Double PMOS
3	3-T XOR	3-T XOR	Double NMOS
4	3-T XNOR	3-T XNOR	Multiplexer
5	3-T XNOR	3-T XNOR	Double PMOS
6	3-T XNOR	3-T XNOR	Double NMOS

Table I. Description of various 8T adders

The design of 8T full adder cell having the least number of transistors using 3T XOR gates is shown in Fig.8. The Boolean equations for the design of the 8T full adder are as follows:

$Sum = A \oplus B \oplus Cin$

$Cout = Cin\,(A \oplus B) + AB$

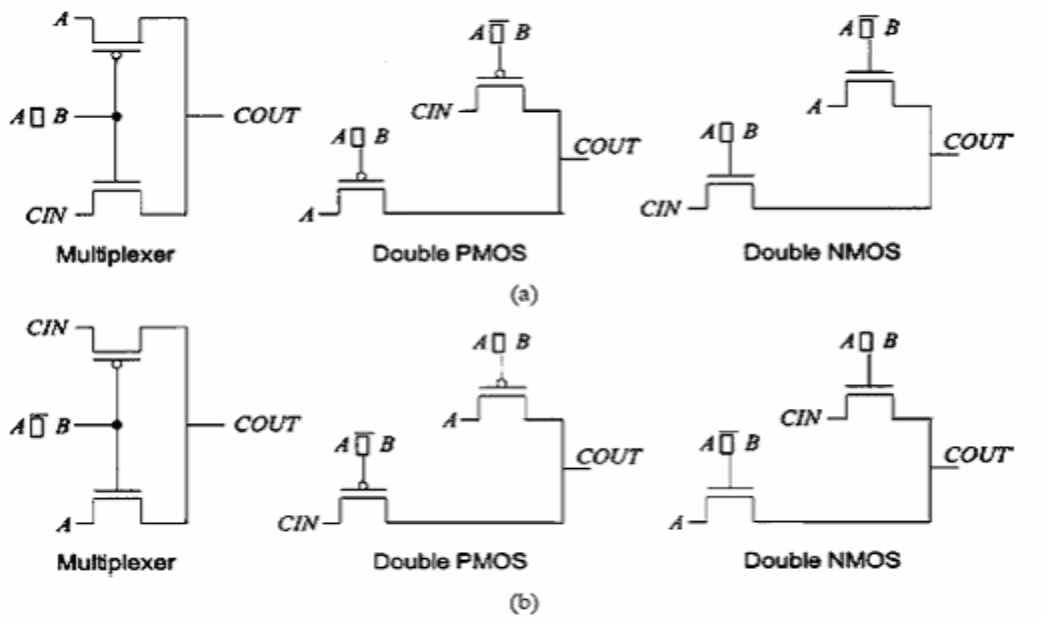


Fig.7 Choices for Module-Cout

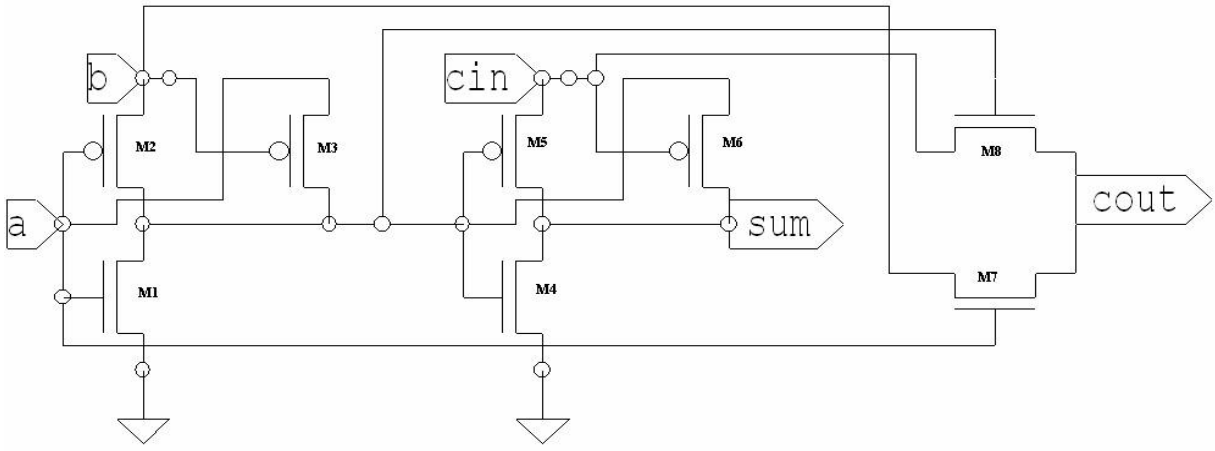


Fig.8 Proposed 8T full adder

The sum output is basically obtained by a cascaded exclusive ORing of the three inputs. The carry output is obtained in accordance with the Boolean equation. The final sum of the products is obtained using a wired OR logic. It is quite evident that two stage delays are required to obtain the sum output and at most two stage delays are required to obtain the carry output.

The voltage drop due to the threshold drop in transistors M3 and M6 in Fig.8 can be minimized by suitably increasing the aspect ratios of the two transistors. However, the threshold voltage drop of |VT,p| provided by the PMOS pass transistor M3 when a=0 and b=0 is used to turn on the NMOS pass transistor M8 and therefore we get an output voltage equal to |VT,p|-VT,n , where VT,p is the threshold voltage of the PMOS transistor and VT,n is the threshold voltage of the NMOS transistor. The difference value is very close to 0V. Similarly, the threshold drop of the transistors M7 and M8 can be minimized by suitably increasing the aspect ratios of transistors M7 and M8.

This circuit shows approximately 45% improvement in threshold loss (0.2v) as compared to other adders stated above. It is the fastest and consumes least power. Therefore we report it to be the best on

account of power consumption, delay and threshold loss.

4 Simulation and Comparison

4.1 Simulation Environment

We have performed simulations using Tanner EDA tool in 90nm and 130nm technologies; with supply voltage ranging from 1v to 2.6v in steps of 0.2v.

Circuits are also simulated on different operating frequencies with Vdd=1.8v at 90nm technology in order to prove that the proposed 8T adder is the fastest among all other adders over the range of operating frequency.

To establish an impartial testing environment each circuit have been tested on the same input patterns shown in Fig.9, which covers every possible combination of A, B and Cin.

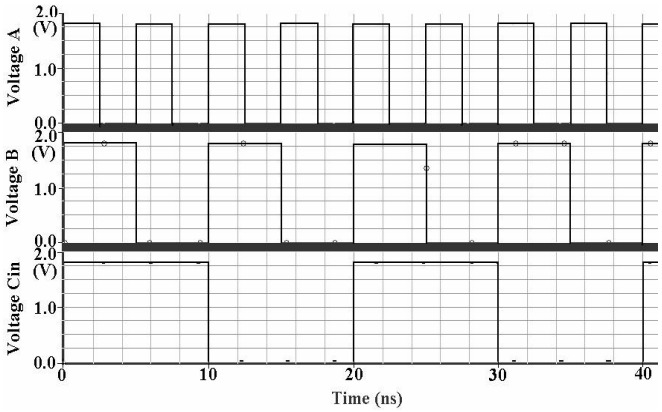


Fig.9 Simulation input patterns

4.2 Comparison

Power consumption and working speed (frequency and delay) are yardsticks for the performance of CMOS circuits. Another important standard for CMOS circuits is Power-Delay product (P×*D)*. This parameter is applied often in testing characteristics of CMOS circuits. Since, in many cases, requirements of low power and high speed cannot be accomplished simultaneously, comparisons only using these two metrics may become problematical.

Comparative studies on the different adders discussed above have been done using 90nm and 130nm technologies. Studies have been done with 16T, 14T, 10T and the proposed 8T full adder cells.

The result of the comparative analysis states that the performance of the proposed 8T full adder cell is the best among all. The 8T full adder cell also occupies the minimum silicon area on chip amongst all the full adders reported so far in the literature. The small silicon area of the proposed full adder cell makes it potentially useful for building compact VLSI circuits on a small area of chips. The threshold loss, delay and power dissipation of the proposed full adder cell is much less compared to any other adder. The net effect is that our proposed 8T full adder cell shows a much better performance compared to any other adders available in the literature.

Fig.10-Fig.27 shows the comparative analysis of the circuits stated above at 90nm and 130nm technology.

The comparisons of 16T and 14T full adder cells are shown in Fig.10-Fig.15.

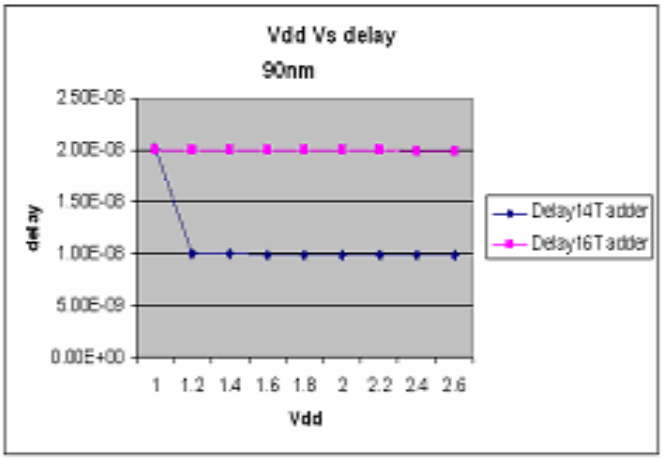


Fig.10 Vdd Vs Delay for 14T and 16T full adder at 90nm technology

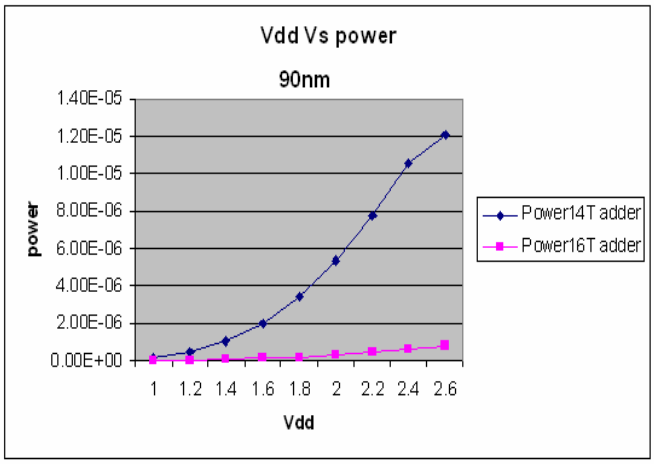


Fig.11 Vdd Vs Power Dissipation for 14T and 16T full adder at 90nm technology

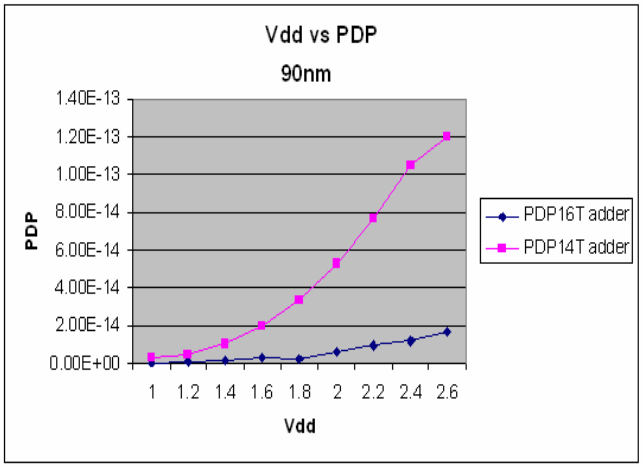


Fig.12 Vdd Vs Power-Delay Product for 14T and 16T full adder at 90nm technology

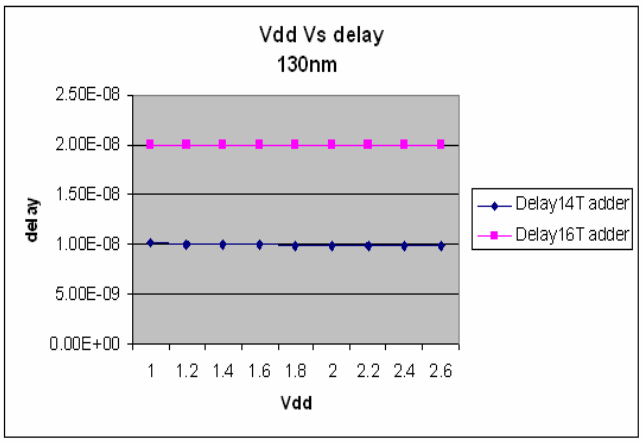


Fig.13 Vdd Vs Delay for 14T and 16T full adder at 130nm technology

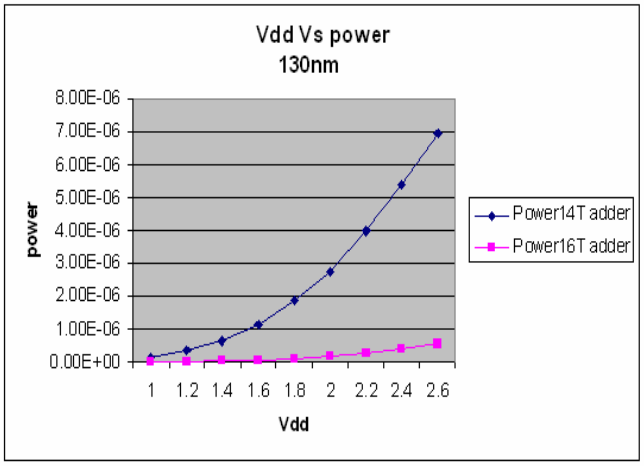


Fig.14 Vdd Vs Power Dissipation for 14T and 16T full adder at 130nm technology

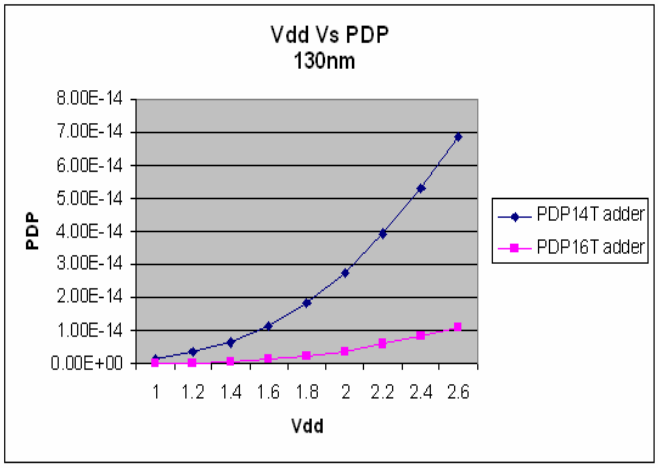


Fig.15 Vdd Vs Power-Delay Product for 14T and 16T full adder at 130nm technology

The above results show that the delay is more in the case of 16T adder as compared to 14T adder but the power dissipation of 16T adder is far superior to 14T adder having advantage of full output swing over 14T adder also. We have also compared the 16T full adder with 10T full adder to show the superiority of one over the other. The comparative graphs are shown in Fig.16-Fig.21.

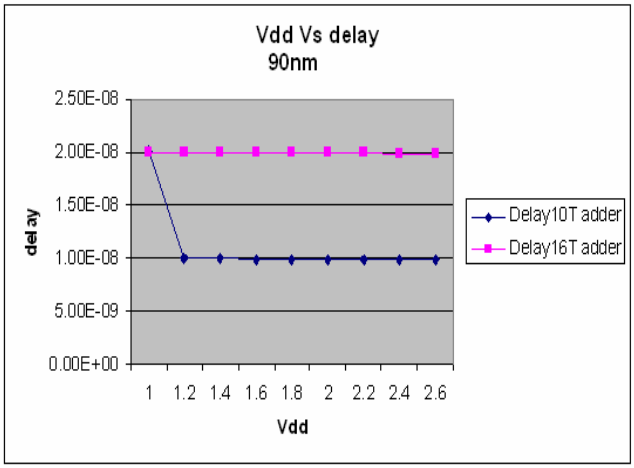


Fig.16 Vdd Vs Delay for 10T and 16T full adder at 90nm technology

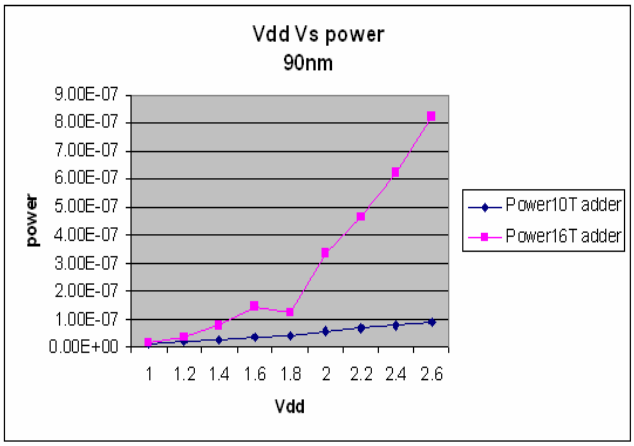


Fig.17 Vdd Vs Power Dissipation for 10T and 16T full adder at 90nm technology

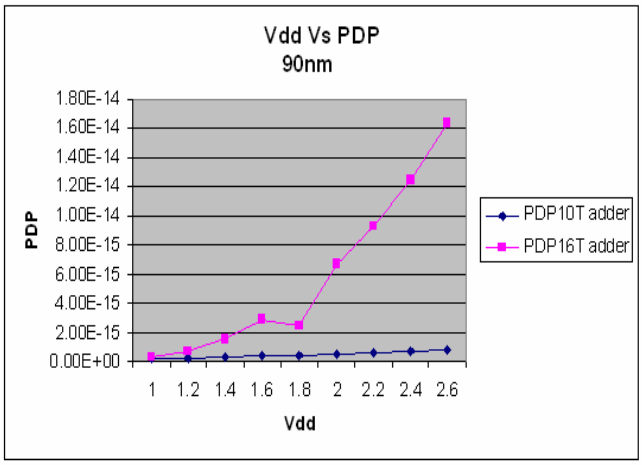


Fig.18 Vdd Vs Power-Delay Product for 10T and 16T full adder at 90nm technology

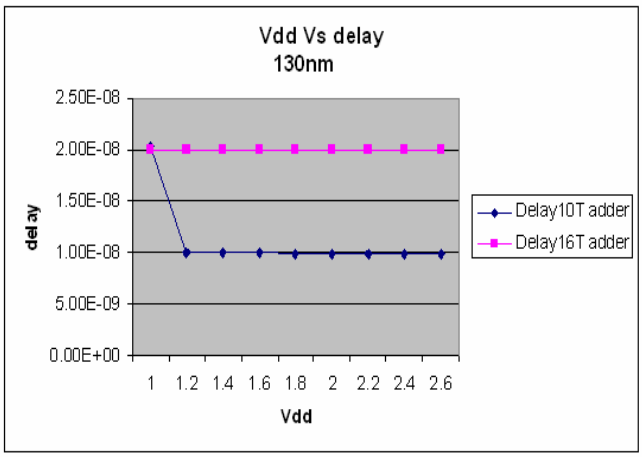


Fig.19 Vdd Vs Delay for 10T and 16T full adder at 130nm technology

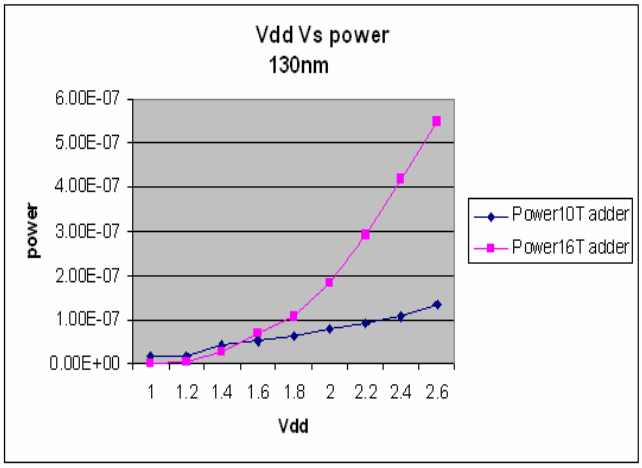


Fig.20 Vdd Vs Power Consumption for 10T and 16T full adder at 130nm technology

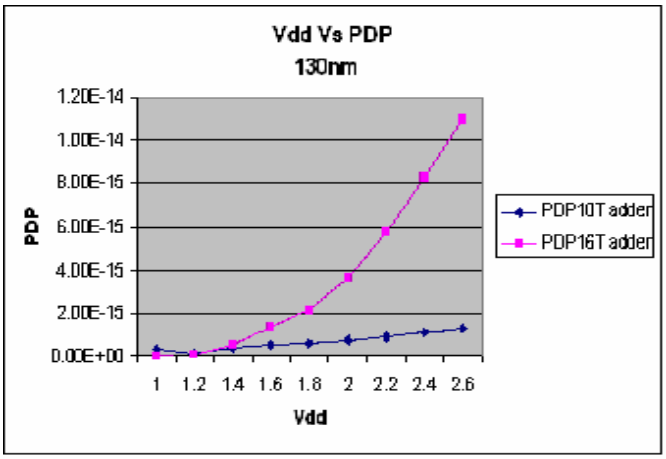


Fig.21 Vdd Vs Power-Delay Product for 10T and 16T full adder at 130nm technology

The above simulation results shows that the 10T full adder is giving better performance than 16T full adder in all perspectives such as area covered on chip, delay and power dissipation and hence it is more superior to 16T full adder cell. Now further we have compared this 10T full adder with the proposed design of 1-bit 8T full adder cell. The curves drawn in Fig.22-Fig.27 make it obvious that 8T full adder cell is having best performance than the other adder cells in terms of speed, power dissipation and power-delay product.

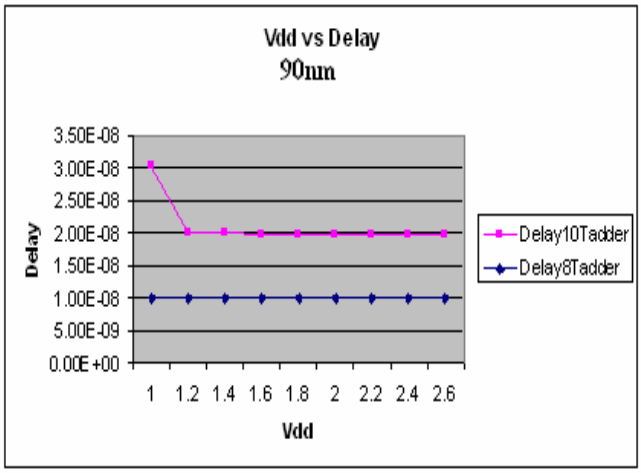


Fig.22 Vdd Vs Delay for 10T and proposed 8T full adder at 90nm technology

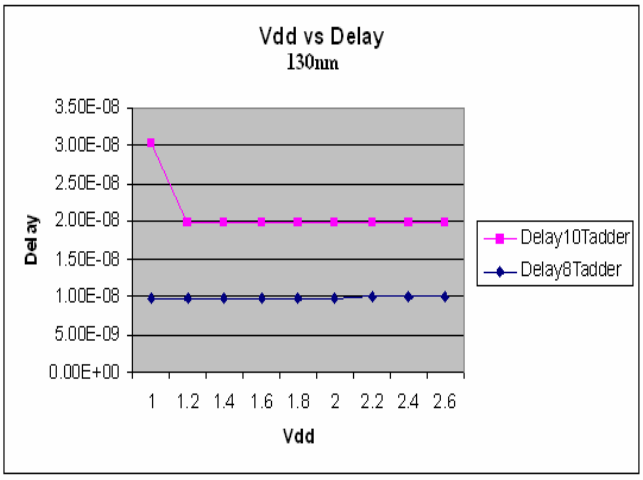


Fig.25 Vdd Vs Delay for 10T and proposed 8T full adder at 130nm technology

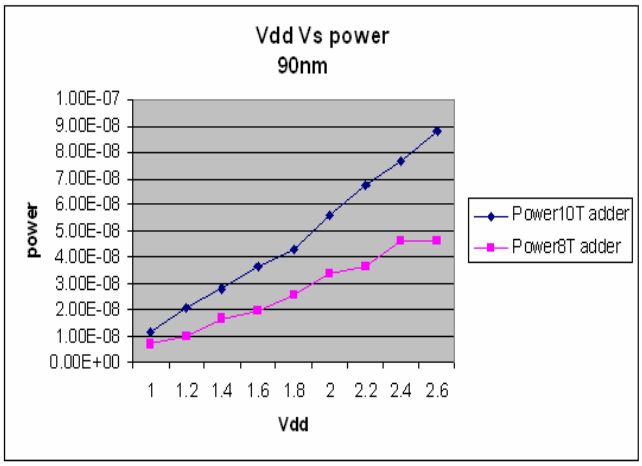


Fig.23 Vdd Vs Power Consumption for 10T and proposed 8T full adder at 90nm technology

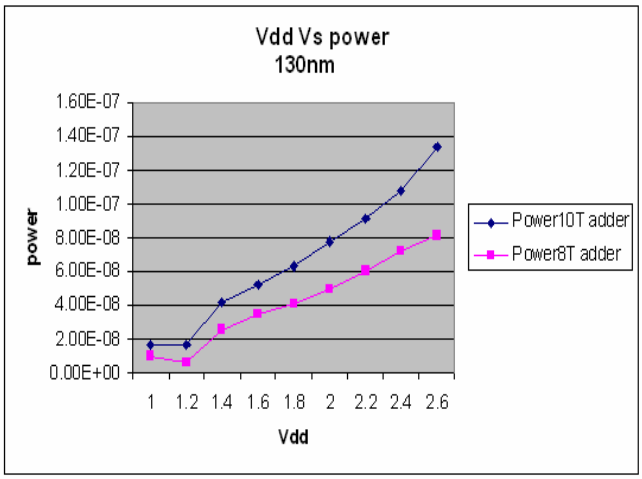


Fig.26 Vdd Vs Power Consumption for 10T and proposed 8T full adder at 130nm technology

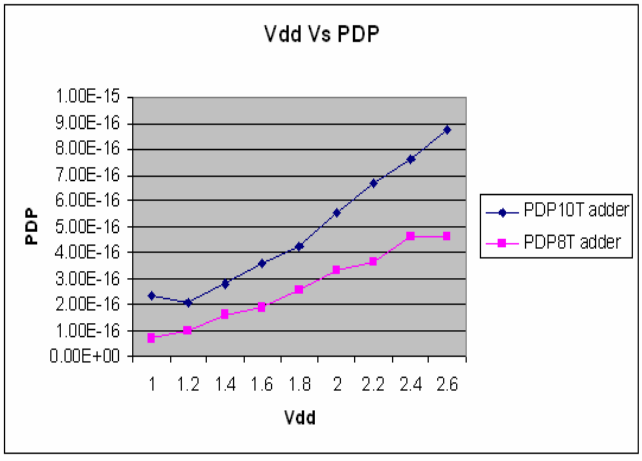


Fig.24 Vdd Vs Power-Delay Product for 10T and proposed 8T full adder at 90nm technology

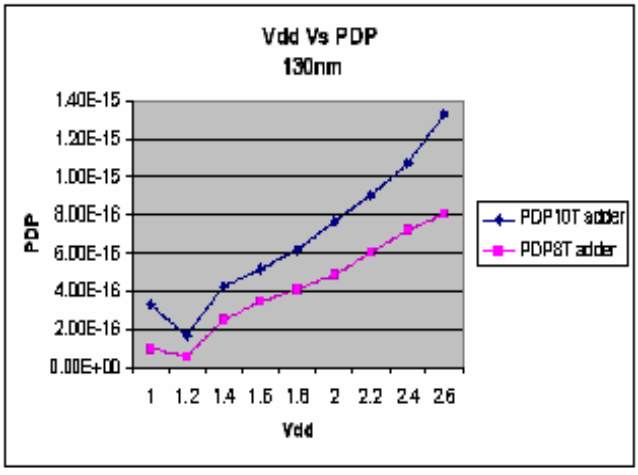


Fig.27 Vdd Vs Power-Delay Product for 10T and proposed 8T full adder at 130nm technology

The above results shows that the proposed adder circuit is better than the other adder circuits stated in the literature having low transistor count. The proposed 8T full adder circuit has threshold loss of approximately 0.2v which is nearly 45% less compared to the circuits available in the literature. Other full adder circuits explained in this paper have the threshold loss of nearly 0.35v except 16T full adder resulting into the full output swing.

The results shown in Table II depicts that the proposed 8T full adder cell has highest speed than other full adders at high operating frequencies. Hence it is the best choice for the high frequency applications.

Frequency (MHz)	Delay (nsec) @ Vdd=1.8volts			
	Proposed 8T adder	10T adder	14T adder	16T adder
100	4.84	4.86	4.88	5.06
200	2.33	2.36	2.37	2.56
300	1.48	1.50	1.52	1.71

Table II. Delay comparison of the full adders using 90nm technology

5 Conclusion

The current work proposes the design of the full adder cell using 8T which acquires least area. It also shows nearly 45% improvement in threshold loss problem compared to other circuits [1]-[8]. The designed full adder is found to give better performance than the adders mentioned in literature so far as the low power, high speed, power-delay product and threshold loss is concerned. It also proves its superiority as the fastest cell for high frequency applications. The proposed 8T adder has been designed and studied using 90nm and 130nm technologies, which establish the technology independence of the circuit.

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