An improved dc capacitor voltage detection technology and its FPGA implementation in the CHB-based STATCOM

Xingwu Yang , Jianfei Zhao, Jianguo Jiang
Department of Electrical Engineering
Shanghai Jiao Tong University
Shanghai 200240
P.R.CHINA
yxw790930@sjtu.edu.cn

Abstract: - In this paper, an improved single multiple-voltage (SMV) detection technology based on cascaded H-bridge(CHB) multilevel inverter-based static synchronous compensator (STATCOM) is introduced and it is realized using a Filed Programmable Gate Array(FPGA) by delay technology. The advantage of the improved SMV detector is that, it could save a lot of voltage sensors by using the inverter output voltage to detect the dc capacitor voltage of each H-bridge unit, meanwhile, it could get their mean value more accurately. Take into account delay time in detection circuit and control circuit, in order to transform this detection technology into practice, a novel delay technology is studied. Based on delay technology, an implementation method of the improved SMV detector using a FPGA is also introduced. The experimental results prove its feasibility and practicality.

Key-Words: - CHB inverter, static synchronous compensator (STATCOM), dc capacitor voltage detection, FPGA, delay technology

1 Introduction

Reactive power compensation is an essential part in a power system, since it could improve the energy transmission capability, stabilize the power system and maintain the supply voltage and so on[1]-[3]. Recent advances in high power electronic switches have enabled the development of new controllable fast reactive power compensators such as static-synchronous compensator (STATCOM) [4]. Conventionally , STATCOM is composed of one inverter with energy storing capacitor on its dc side, inductances and a coupling transformer on its ac side, which is connected in parallel with the system at the point of common coupling (PCC), as shown in Fig.1, the fundamental principle of STATCOM is the generation of a controllable ac voltage source by a voltage source inverter(VSI). The ac voltage source appears behind the transformer leakage reactance. So the active and reactive power transfer is caused by the voltage difference across this reactance[5].

In recent years, multilevel voltage source inverter has gained much attention. The inverter can use a number of techniques to construct high-quality ac waveforms from several switched dc sources, so it is possible to achieve high-voltage low-distortion ac waveforms, which result in lower harmonic generation[4], smaller reactor size[6], and eliminating bulky and costly transformer [7][8]. There are three well-established topologies of multilevel inverter: neutral point clamped[9], flying capacitor[10] and CHB converter configuration[11]-[13]. This paper deals with the CHB inverter which is deemed as one of the most promising topologies for STATCOM application[6][11].

A seven level single phase CHB multilevel converter is illustrated in Fig.2. One of the main disadvantages of the CHB-based STATCOM is the voltage imbalance between the multiple floating dc capacitors, unequal conducting and switching losses produced by power switching devices, as well as resolution issues inherent in the control circuit, may bring voltage imbalance to the dc capacitors. Several literature studied the problem and proposed different control strategies, such as using low-frequency modulation techniques[12] or taking adequate control strategy to change the active power absorbed by each H-bridge unit [8][13][14]. No matter what methods, in order to realize dc capacitor voltage balancing control, dc capacitor voltage of each unit has to be detected. It means that *M*-level CHB-based STATCOM need $3(M-1)/2$ voltage sensors. In order to reduce voltage sensors, literature[15] proposed a single multiple-voltage (SMV) detector to detect all dc capacitor voltages through detecting the output phase voltage of CHB

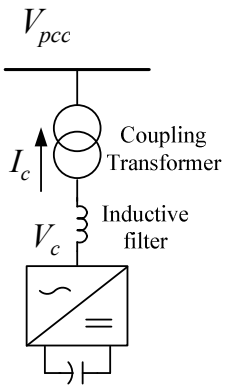


Fig.1- STATCOM basic structure

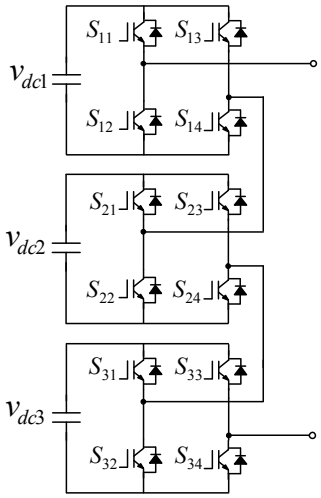


Fig.2- A seven level single phase CHB multilevel converter

inverter. Where, SMV detection method is tested based on the dSPACE prototyping system, but it doesn't finish a depth-analysis of some issues which need to be paid attention in practical application.

In this paper, an improved SMV detector based on the CHB-based STATCOM is proposed, which can get more accuracy value of the dc mean capacitor voltage, in addition, an implementation method with a field programmable gate array (FPGA) is presented. Because the accuracy of SMV detector is affected by many factors, such as the detection circuit, the sampling frequency and so on, a novel delay technology is studied. The main factors which determine the delay time such as detection circuit, cascade number in each phase and switching frequency are analyzed emphatically. This strategy is experimentally validated. The proposed dc capacitor voltage detection method is combined with the carrier phase shift SPWM(CPS-SPWM) modulation strategy and individual balancing control technology, so the balancing control of dc capacitor voltages is easy to be implemented. Experimental results shows that the STATCOM system has excellent steady-state and dynamic performance.

2 System configuration and control scheme

As is shown in Fig.3, The CHB inverter is connected to the PCC at the ac system through a filter with inductance L_c, and the PCC is supplied power from the ac source. The objective of the STATCOM is to generate a proper output voltage to get a leading or lagging reactive current, thus, it can compensate reactive power generated by the load.

2.1 Configuration of CHB-based STATCOM

Fig.3 shows the system configuration of the CHB inverter based STATCOM, where u_s is the source voltage, i_s is the source current, i_L is the load current, i_c is the current drawn by the STATCOM, i_{cq}, i_{cq}^* is the reactive current and its reference, i_{cd}, i_{cd}^* is the active current and its reference, v_{dc}^* is the dc capacitor voltage reference of each H-bridge, and θ is the phase angle of the public point of voltage.

2.2 Control Scheme

The STATCOM control scheme contains output current control and voltage balancing control. In order to control active current and reactive currents independently and get good dynamic performance, output current control adopts decoupled current control strategy[1][3]. In order to ensure that STATCOM is stable, voltage balancing control comprises dc capacitor voltage control and an individual balancing control as shown in Fig.3.

2.1.1 Decoupled Currents Control Strategy

In d-q synchronous reference frame, the mathematical expression of the STATCOM is shown as follows:

$$L_c \frac{d}{dt}\begin{bmatrix} i_{cd} \\ i_{cq} \end{bmatrix} = \begin{bmatrix} v_{sd} \\ v_{sq} \end{bmatrix} - \begin{bmatrix} v_{cd} \\ v_{cq} \end{bmatrix} + \omega L_c \begin{bmatrix} i_{cq} \\ -i_{cd} \end{bmatrix} \quad (1)$$

In order to generate the desired active and reactive current components i_{cd}^* and i_{cq}^* for the STATCOM, the references of the STATCOM output voltages u_{cd}^* and u_{cq}^*, should be given as

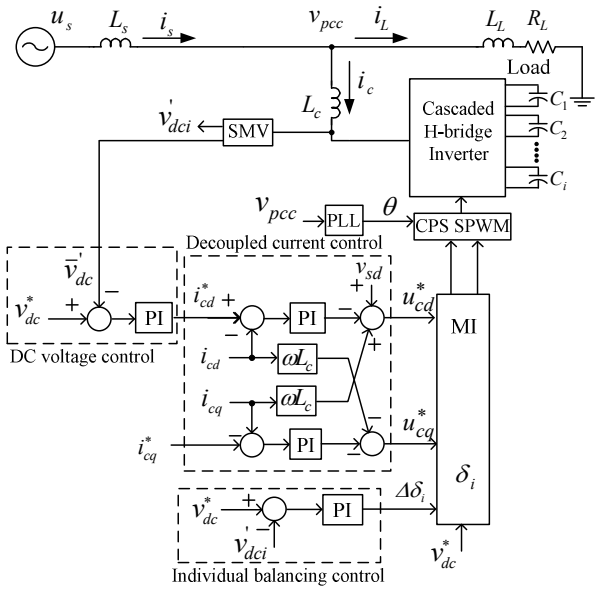


Fig. 3. System configuration and control block diagram of the CHB-based STATCOM

$$\begin{bmatrix} u_{cd}^* \\ u_{cq}^* \end{bmatrix} = \begin{bmatrix} v_{sd} \\ v_{sq} \end{bmatrix} + \omega L_c \begin{bmatrix} i_{cq} \\ -i_{cd} \end{bmatrix} - \begin{bmatrix} L_c \dfrac{d}{dt} i_{cd}^* \\ L_c \dfrac{d}{dt} i_{cq}^* \end{bmatrix} \tag{2}$$

and

$$u_c^* = \sqrt{(u_{cd}^*)^2 + (u_{cq}^*)^2} \tag{3}$$

$$\delta = \tan^{-1}(u_{cd}^* / u_{cq}^*) \tag{4}$$

Where, u_c^* can be used to obtain modulation index

$$MI = u_c^* / kn\bar{v}_{dc} \tag{5}$$

(k is a constant whose value depends on the modulation technique scheme used, n is the cascade number. in this paper, k is 0.5)

Based on (3) ~ (5), a decoupling feedforward control is obtained as shown in Fig.3. In this figure, the active current reference i_{cd}^* is used to regulate the dc voltage, and the reactive current reference i_{cq}^* is given according to different compensation aims[1].

2.1.2 Voltage balancing control

STATCOM should consume a small amount of energy due to switching losses, copper- and core-loss of reactor, so current controller should supply appropriate active power to compensate the power loss of STATCOM. The reference of the active current can be obtained by dc capacitor voltage control as shown in Fig.3, when the active current in d-axis i_{cd} reaches to it's reference , the dc mean capacitor voltage has been regulated to its desired value v_{dc}^*. However, dc capacitor voltage controller can only ensure that the power drawn from each dc side is equal, due to unequal conducting and switching losses, as well as resolution issues inherent in the control circuit, it will result in dc capacitor voltages imbalance. Dc capacitor voltages imbalance will affect the character of STATCOM and even damage the switch device. So for multilevel inverter based on STATCOM, dc voltage regulation is essential in normal operation. In order to compensate the power loss of STATCOM and maintain the dc capacitor voltage at desired value, appropriate active power should be absorbed by STATCOM. PI controller is applied to regulate individual dc capacitor voltage, the error between dc capacitor voltage reference and each actual dc capacitor voltage is fed to PI controller. The output is used to regulate the phase of output voltage which affects active power absorbed, so dc side of each unit can absorbed different and appropriate active power to make individual dc capacitor voltage balancing. As shown in Fig.3, each phase angle is determined by:

$$\delta_i = \delta + \Delta\delta_i \qquad i = 1,2,3...n \tag{6}$$

For 5-level CHB-based STATCOM, the modulation wave can be obtained

$$\begin{cases} u_{u1} = MI\cos(\theta + \delta_1) \\ u_{u2} = MI\cos(\theta + \delta_2) \\ u_{v1} = MI\cos(\theta + \delta_1 - 120^\circ) \\ u_{v2} = MI\cos(\theta + \delta_2 - 120^\circ) \\ u_{w1} = MI\cos(\theta + \delta_1 + 120^\circ) \\ u_{w2} = MI\cos(\theta + \delta_2 + 120^\circ) \end{cases} \tag{7}$$

3 Dc capacitor voltage detection technique

For traditional detection strategy used in CHB-based STATCOM, output voltage of each H-bridge unit need a voltage sensor to detect, in a M-level CHB-based STATCOM, there are $3(M-1)/2$ H-bridge to be detected, that is, $3(M-1)/2$ voltage sensors are required. Literature[15] proposed a new detecting technique, all individual dc capacitor voltage can be obtained through a SMV detector based on the inverter output voltages, thus, each phase of the

cascaded inverter only need one voltage sensor to detect dc capacitor voltage. Traditional dc capacitor voltage measurement method and SMV detection method shown in Fig.4.

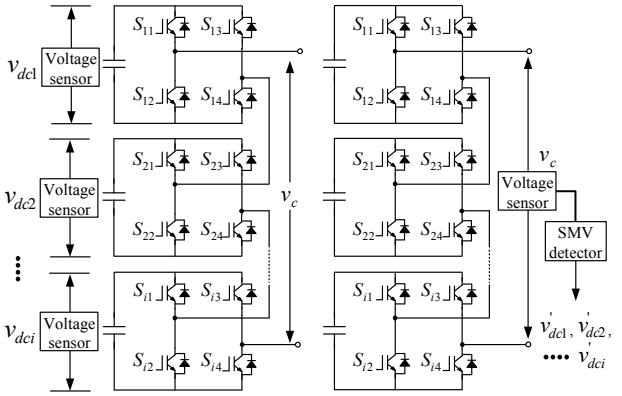


Fig.4- Two dc capacitor voltage detection methods in CHB multilevel inverter. (a)traditional method, (b) SMV detection method.

3.1 Principle of a new dc capacitor voltage detection

For CHB converter, all units are connected in series, so the converter instantaneous total output voltage is equal to the sum of the individual dc capacitor voltage, that is

$$v_c = \sum_{i=1}^{n} v_{Hi} \tag{8}$$

The converter used in STATCOM acts as an inverter, each H-bridge unit can generate three-level output, +Vdc, 0V, -Vdc by connecting dc voltage to ac side through different states of the four switches. Define a condition as follows: one H-bridge unit in one phase, such as H_i generates output voltage +Vdc or -Vdc, other units generate output voltage 0V. So the inverter phase voltage equals to the output voltage of unit H_i.

$$v_c = v_{Hi} = \pm v_{dci} \tag{9}$$

Therefore, the dc capacitor voltage of H-bridge unit H_i can be obtained from the inverter phase voltage as follows:

$$v'_{dci} = |v_c| . \tag{10}$$

The prime of v_{dci} denotes that the dc capacitor voltage is obtained by dc voltage detection method instead of measuring from the voltage sensor.

3.1 Improved single multiple-voltage detector

According to the principle of dc capacitor voltage detection above, a SMV detector can be designed. Owing to dc mean capacitor voltage $\bar{v}'_{dc}$ is also used in STATCOM control scheme, in order to improve the accuracy of $\bar{v}'_{dc}$, an improved SMV detector is proposed. Here, we take a seven-level inverter as an example, and the principle can be explained with the aid of Fig.5.

Waveforms in Fig.5(a) shows that a single modulating sine wave is compared with six phase shifted triangular carrier to decide the switching instants. Fig.5(b)-(d) are three H-bridge units output voltages and Fig.5(e)-(f) are all the inverter phase output voltage, Fig.5(e) is to show the principle of improved SMV detection strategy and another is to show the principle of traditional SMV detection strategy. Assuming each dc capacitor has the same dc voltage, defined to be E, it is clear that the output voltage of three H-bridge units cascaded inverter contains seven different level outputs (-3E, -2E, -1E, 0V, 1E, 2E, 3E). When v_c is one level voltage pulse, it corresponds to the output voltage of a certain H-bridge unit.

For traditional SMV detector as is shown in Fig.5(f), when the output voltage of u-phase v_{cu} is more than one level, v'_{dcu1}, v'_{dcu2} and v'_{dcu3} keep invariant, so the dc mean capacitor voltage in u-phase $\bar{v}'_{dcu}$ obtained by the following equation also keeps invariant.

$$\bar{v}'_{dcu} = (v'_{dcu1} + v'_{dcu2} + v'_{dcu3})/3 \tag{11}$$

In order to improve the accuracy of $\bar{v}'_{dcu}$, it also needs to update $\bar{v}'_{dcu}$ when the output phase voltage of inverter is the max level, as it is clear that v_{cu}

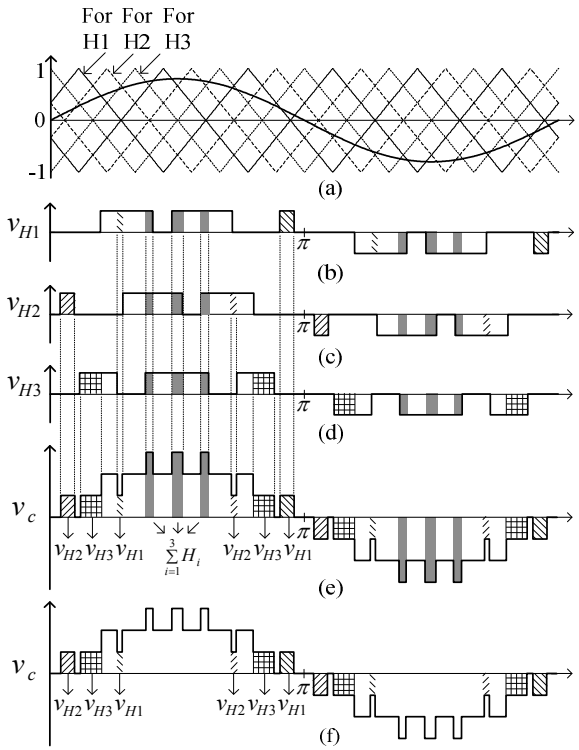


Fig.5- schematic diagram of improved SMV and traditional SMV detection strategy.

Table 1-Value assignment method in u-phase for improved SMV detector

Output voltage of each unit			Detected dc capacitor voltage	Detected dc mean capacitor voltage
H1	H2	H3		
±E	0	0	$v'_{dcu1} = \mid v_{cu} \mid$ v'_{dcu3}、v'_{dcu2} invariant	$\bar{v}'_{dcu} = \sum v'_{dcui} / 3$
0	±E	0	$v'_{dcu2} = \mid v_{cu} \mid$ v'_{dcu1}、v'_{dcu3} invariant	
0	0	±E	$v'_{dcu3} = \mid v_{cu} \mid$ v'_{dcu1}、v'_{dcu2} invariant	
E	E	E	$v'_{dcu1} \sim v'_{dcu3}$ invariant	$\bar{v}'_{dcu} = v_{cu} / 3$
-E	-E	-E	$v'_{dcu1} \sim v'_{dcu3}$ invariant	$\bar{v}'_{dcu} = -v_{cu} / 3$
other			v'_{dcu1}、v'_{dcu2}、v'_{dcu3} and $\bar{v}'_{dcu}$ invariant	

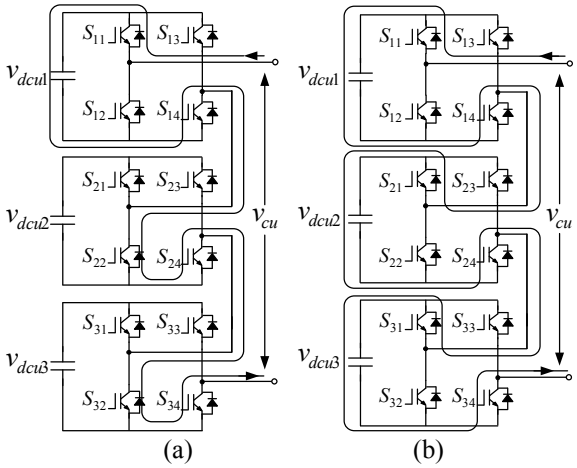


Fig.6- Two switching combination when v_{cu} is one and max level.

corresponds to the sum of dc capacitor voltages of u-phase directly as is shown in Fig.5.

$$\bar{v}'_{dcu} = \mid v_{cu} \mid / 3 \quad (12)$$

The dc mean capacitor voltage of three-phase system $\bar{v}'_{dc}$ is given by

$$\bar{v}'_{dc} = (\bar{v}'_{dcu} + \bar{v}'_{dcv} + \bar{v}'_{dcw}) / 3 \quad (13)$$

Table 1 shows value assignment method of dc capacitor voltage and dc mean capacitor voltage. When the inverter output voltage is one level, the dc capacitor voltage of one H-bridge unit H_i can be obtained from the inverter voltage of u-phase v_{cu}, so the detected dc capacitor voltage v'_{dcui} is updated with the inverter output voltage $|v_{cu}|$, at the same time the other dc capacitor voltage need to keeps the previous value. take one switching combination for example, S11=1, S13=0, S21=0, S23=0, S31=0, and S33=0, as is shown in Fig.6(a). The output voltage v_{cu} is just the dc capacitor voltage of H_1 unit, so the value of v_{cu} can be used to update the value of v'_{dcu1}. take another example, S11=1, S13=0, S21=1, S23=0, S31=1, and S33=0, as is shown in Fig.6(b). The output voltage v_{cu} is the sum of dc capacitor voltages of H_1, H_2 and H_3 unit. In this way, as v'_{dcu1} can be also updated when the output voltage is max level, its detection accuracy could be improved.

4 FPGA implementation of Improved SMV detector

The improved SMV detector is based on the switching state, so it is easily implemented if a

FPGA is used. Logic relationship of switching states for improved SMV detector is shown in Table 2. (where "&" denotes logic of AND, "^" denotes logic of XOR, "^~" denotes logic of XNOR, and "!" denotes logic of NOT). Table 1 combined with Table 2 illustrates the implementation method of improved SMV detection strategy using FPGA .

According to states of the switches, as shown in Table 2, the improved SMV detector can achieve the detection of each of dc capacitor voltage and dc mean capacitor voltage by detecting the output voltages of the CHB-based STATCOM. However, there are some factors that may affect the accuracy of SMV detector such as the response time of the sensors and amplifier in voltage detection circuit, etc. So, it is necessary to take effective measures to ensure that SMV detector works well in actual application. This paper proposes a novel delay technology during the assignment processes of SMV detection. Delay time will be discussed in detail below.

In general, delay time includes three parts. The first part is caused by the detection circuit, the reason is that sensor and operational amplifier in detection circuit have a response time. Voltage detection circuit, in this paper, uses voltage sensors LV28-p, and the sensor's response time is determined by the parameter $t_r = 40\mu s$ (90% $V_{P\max}$), so, for a M level CHB inverter, response time of the sensor between two adjacent levels can be expressed as follows(for CPS-SPWM, the output voltage level only jump a level once time) :

$$t_1 = \frac{t_r}{M} \tag{14}$$

Table 2-Logic relationship of switching states used for improved SMV detector

Logic of switching states	Output voltage of each unit		
	H1	H2	H3
$(S_{11}\hat{}S_{13})\&(S_{21}\hat{}\sim S_{23})\&(S_{81}\hat{}\sim S_{83})$	±E	0	0
$(S_{11}\hat{}\sim S_{13})\&(S_{21}\hat{}S_{23})\&(S_{81}\hat{}\sim S_{83})$	0	±E	0
$(S_{11}\hat{}\sim S_{13})\&(S_{21}\hat{}\sim S_{23})\&(S_{81}\hat{}S_{83})$	0	0	±E
$(S_{11}\&!S_{13})\&(S_{21}\&!S_{23})\&(S_{81}\&!S_{83})$	E	E	E
$(!S_{11}\&S_{13})\&(!S_{21}\&S_{23})\&(!S_{81}\&S_{83})$	-E	-E	-E

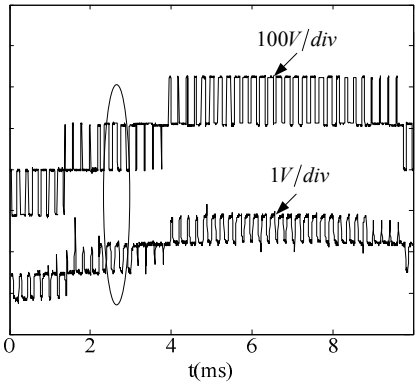


Fig.7- waveform of output voltage of inverter and its detected voltage.

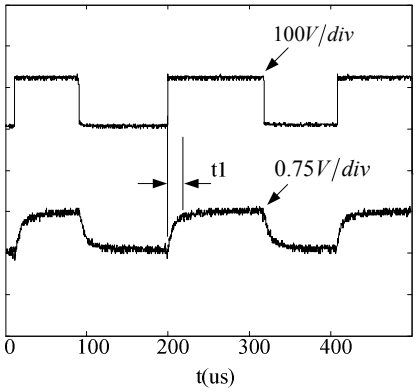


Fig.8- Closeup waveform of Fig.7.

As the response time of operational amplifier is always smaller than the sensor's, sensor's response time could represent the entire response time of detection circuit.

Waveforms of output voltage of 5-level cascade inverter and its detected voltage are shown in Fig.7. Top of Fig.7 is the waveform of output voltage of the CHB inverter, and bottom is waveform of output voltage of detection circuit. To make it clear, the closeup of Fig.7 is shown in Fig.8. It can be seen that the tested delay time is consistent with the analysis in equation (14) which is about 10 microseconds.

The second part is caused by the process of dealing with A/D sampling results in DSP and FPGA. Firstly, DSP sends its AD conversion results to FPGA, and then FPGA return the operation results of SMV. This process will produce a delay time t_2, which is about $20\mu s$ in this paper (If an external A/D chip combined with FPGA to complete sampling and operation of SMV, the second part of the delay time could be ignored).

The third part is a sampling period t_s. When the output voltage level of the detection circuit is stable, the value of output voltage of the CHB inverter just

can be used to update dc capacitor voltage values after a sampling period. At that time, the updated

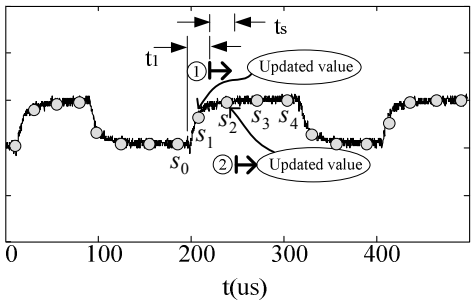


Fig.9- Detailed legend description of the third part of delay time.

value is really in steady state, that is, if the update is done at the beginning of the steady state, the updated value may be the last sampling value, which is not in stable as shown in Fig.9. The dots in Fig.9 denote sampling points. At time□, updated value is s_1 which is not in steady state. After a sampling time, at time□, updated value is s_2 just in steady state.

The overall delay time can be assigned by the following expression:

$$t_{\text{delay}} = t_1 + t_2 + t_s$$

(15)

For output voltage of the CHB inverter, maximum time one level voltage sustained is determined by the number of level and the carrier frequency f_c (using of carrier phase shift unipolar SPWM modulation strategy).

$$t_{\max} < \frac{1}{(M-1)f_c}$$

(16)

It is clear that the delay time must be less than the maximum time one level voltage sustained. Introduce a parameter k as margin, and k is more than one, so

$$t_{\text{delay}} \le \frac{t_{\max}}{k}$$

(17)

Equation (15) ~ (17) can be used to determine the limitation of the sampling frequency(reciprocal of t_s) , when the cascade number and the switching frequency are all fixed.

$$t_s < \frac{1}{k(M-1)f_c} - \frac{t_r}{M} - t_2$$

(18)

We can also obtain the limitation of cascade number n when the carrier frequency and sampling frequency are fixed

$$\frac{1}{k(M-1)f_c} - \frac{t_r}{M} - t_2 - t_s > 0$$

(19)

as M is 5,7, even more if SMV could be used, in order to facilitate the calculation, equation (19) could be expressed as:

$$\frac{1}{kMf_c} - \frac{t_r}{M} - t_2 - t_s > 0$$

(20)

After substitute $M = 2n+1$ into (20), restriction on n can be obtained

$$n < \frac{1 - kf_c(t_r + t_2 + t_s)}{2kf_c(t_2 + t_s)}$$

(21)

5 Experimental setup

In order to confirm the validity of the improved SMV detector and the performance of the CHB-based STATCOM, a 3kVA experimental prototype is built and tested. The block diagram is shown in Fig.10. The main parameters are given in table 3. The prototype model shown in this paper is a five-level CHB inverter with two series H-bridge connected to the grid through a LC filter. Each H-bridge unit consists of FAIRCHILD G80N60 IGBT and a driving circuit. TMS320F2812 and XC3S50AN FPGA based system are employed as the controller, where FPGA is used to realize the improved SMV detector as well as perform modulation strategy.

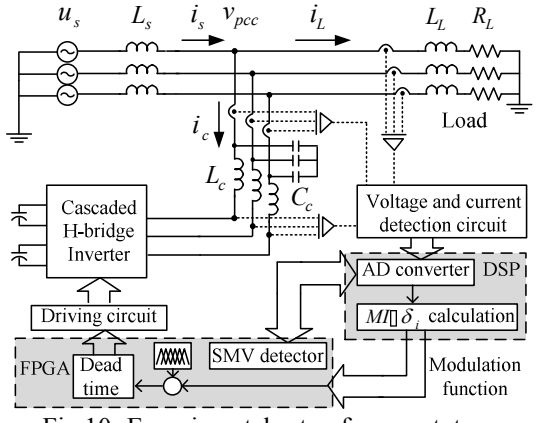


Fig.10- Experimental setup for a prototype CHB-based STATCOM

Table 3-Circuit parameters of the experimental setup

Source voltage rating	V_s	$110V$
Rated reactive power	Q	$3kVA$
System inductance	L_s	$100\mu H$
Inductive filter	L_c	$5mH$
	C_c	$1.2\mu F$
dc capacitor voltage reference	v_{dc}^*	$100V$
dc capacitor capacitance	C	$1880\mu F$
Dead time in each CHB		$2.5\mu s$
Carrier frequency		$2\ kHz$

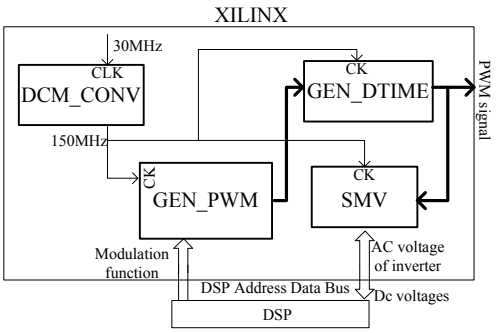


Fig.11- block diagram of modulation strategy and SMV detector implemented in FPGA

About FPGA, four main blocks are presented: Clock management block, PWM generation block, Dead time generation block and SMV detector block, as shown in Fig.11. The functional blocks presented in Fig.11 are fully implemented in this relatively inexpensive integrated circuit. All programming is done in verilog HDL circuit description language, and each functional block is an entity in verilog HDL.

The functional block operate as follows:

- Internal DCM_CONV block converts 30MHz clock to 150MHz to match the clock of DSP.
- GEN_PWM block generates phase shifted carrier signals which compared with a 16-b binary number sequence transmitted from DSP as defining a reference sinusoidal signal to generate switching state signals.
- GEN_DTIME block produces driving signals with deadtime.
- SMV block receives output voltage values of inverter transmitted from DSP to realize improved SMV detector according to different switching combination.

6 Experimental results

Based on the previously mentioned prototype system, an experiment has been carried out. We tested the performance of improved SMV detector, in addition, the performance of the CHB-based STATCOM was tested simultaneously.

6.1 Performance of improved SMV detector

Fig.12-13 shows the waveforms in Code Composer Studio (CCS) during the system operating. Owing to 20k sampling frequency and 2k carrier frequency used in five-level STATCOM in this paper, the range of overall delay time is determined. It is tested

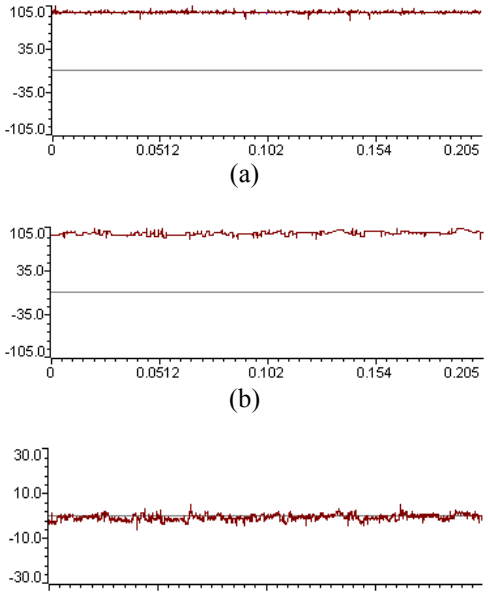


Fig.12- test results of the dc capacitor voltage of H_1 in u-phase.
(a) actual dc capacitor voltage v_{dcu1}.
(b) detected dc capacitor voltage $v_{dcu1}^{'}$.
(c) error between detected value and actual value.

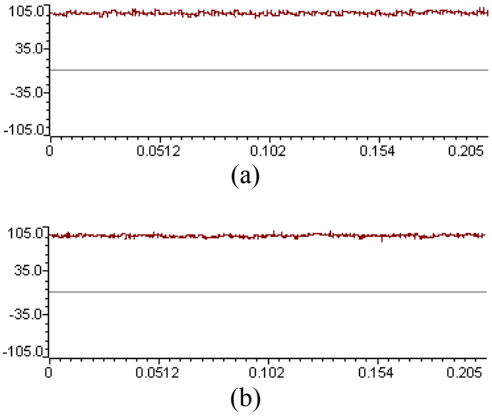
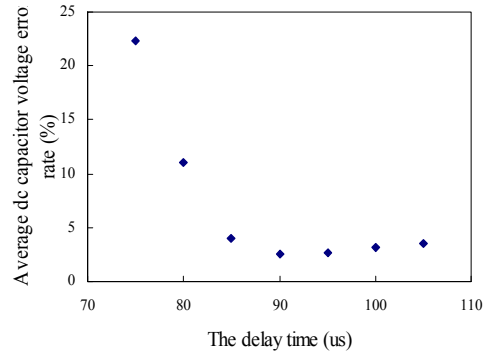


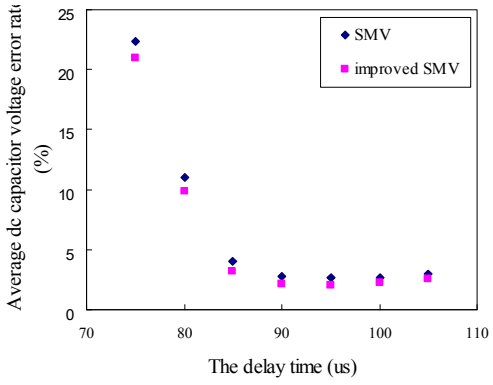
Fig.13- tested result of dc mean capacitor voltage.
(a)by traditional SMV detector
(b) by improved SMV detector

in the case of delay time chosen 90 μs . Waveform of actual dc capacitor voltage v_{dcu1} is shown in Fig.12(a). The detected dc capacitor voltage v'_{dcu1} by improved SMV detector is shown in Fig.12(b). The error between them is shown in Fig.12(c). Fig.13 shows the waveform of detected dc mean capacitor voltage by traditional SMV detector and improved SMV detector separately.

When the system sampling frequency and carrier frequency are fixed, delay time determines the accuracy of SMV detector. Delay time could be neither too long nor too short. In order to describe the accuracy of detection, we introduce an index average voltage error rate as $|v'_{dc} - v_{dc}|/v_{dc}$. Fig.14(a) demonstrates the relationship between the average voltage error rate and the delay time about v'_{dcu1} . Fig.14(b) shows comparison of the average voltage error rate test results of $\bar{v}'_{dc}$ using traditional SMV and improved SMV. It is observed from Fig.14(b) that the improved SMV detector gets more accuracy value than traditional SMV detector.



(a)



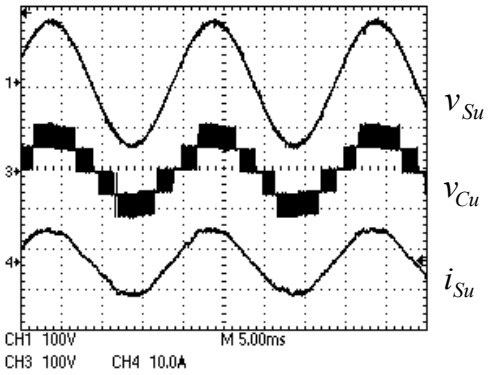
(b)

Fig.14- average error rate of detected voltage
(a) average dc capacitor voltage error rate of v'_{dcu1}
(b) comparison of the average voltage error rate test results of $\bar{v}'_{dc}$ using traditional SMV and improved SMV

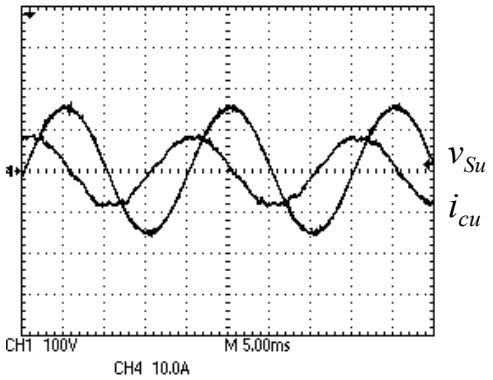
6.2 Performance of the CHB-based STATCOM

6.2.1 Steady state

System operation in steady state is tested, and some of the results are shown in Fig.15. Fig.15(a) shows that the system current i_{su} and voltage v_{su} are almost in same phase when STATCOM absorbs reactive power from the system.Fig.15(b) shows STATCOM u-phase output current.



(a)



(b)

Fig.15- Experimental waveforms in steady state.
(a) source voltage(line-neutral) v_{Su} , inverter output voltage (line-neutral) v_{Cu} , and the source current i_{Su} .
(b) source voltage(line-neutral) v_{Su} and STATCOM output current i_{Cu} .

6.2.2 Dynamic state

Fig.16 shows experimental results of dynamic response when STATCOM was started. It can be seen that, it has an excellent dynamic response with a step change from zero to 1800VA.

Fig.17 shows the dynamic response of the CHB-based STATCOM with a step change of the command from capacitive to inductive and vice

versa.

Fig.18 shows variation of dc capacitor voltages (four dc capacitor voltages in u-phase and v-phase) when individual balancing control is enabled. Initially, the dc capacitor voltages are unbalanced due to the different power losses of H-bridge units, but when the individual balancing control is activated, the voltage balance is achieved in 0.2s.

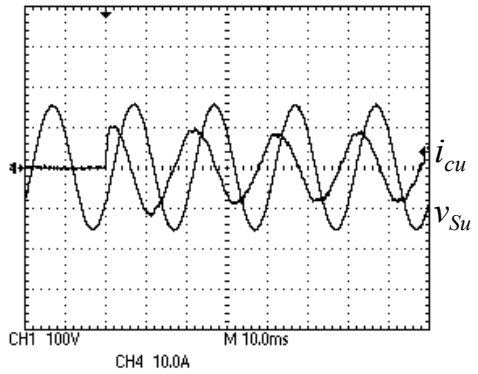


Fig.16- Experimental waveforms when STATCOM was started

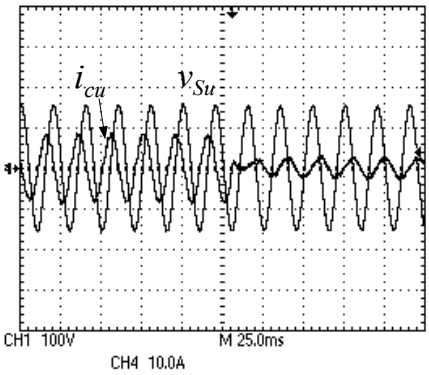


Fig.17- dynamic response for a step change in the command from capacitive to inductive

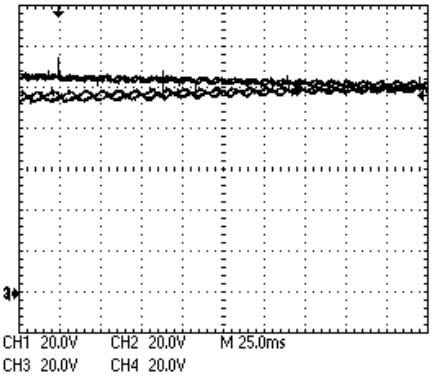


Fig.18- The variation of dc capacitor voltages when individual balancing control was enabled

7 Conclusion

In this paper, an improved single multilevel voltage (SMV) detector based on CHB-based STATCOM is proposed. For the CHB-based STATCOM, with the improved SMV detection technology, dc capacitor voltage detection only need three voltage sensors, all individual H-bridge dc capacitor voltage can be detected accurately, at the same time, more accurate dc mean capacitor voltage can be got In addition, the implement method is introduced, take into account delay time in detection circuit and control circuit, the delay time may produce a bad effect on the accuracy of detected value, the author propose a delay technology, which play an important role in promoting practical application of SMV detection technology. The validity of the improved SMV detector is proved by the experimental results, and excellent performance of the CHB-based STATCOM are obtained with decoupled current control and voltage balancing control strategies.

Acknowledgements

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