Dynamic Modeling and Robust Control of Multi-Module Parallel Soft-Switching-Mode Rectifiers

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Abstract: - In this paper, small-signal modeling and robust controller design for multi-module parallel soft-switching mode rectifiers (SSMRs) are presented. First, a single-phase boost-type SSMR is formed from the traditional boost-type switching mode rectifier (SMR) with auxiliary resonant branch to achieve zero-voltage-transition (ZVT) soft switching for the main and auxiliary switches. Based on the proposed single-phase SSMR, parallel operation of multi-module single-phase SSMR is made for increasing the total power capacity and the reliability of the SSMRs. The state-space averaging method is employed to derive the small signal model of the SSMR in current control loop for performing its current controller design. As for the voltage control loop, the dynamic model of the multi-module SSMR is derived at nominal case by averaging method for two-time-scale (AM-TTS) and averaged power method. Then, the quantitative and robust voltage regulation controls are proposed for multi-module SSMR to improve the control performance when the parameter variations caused by system configuration change and operating point shift have occurred. The accuracy of the derived SSMR dynamic model and the effectiveness of the proposed controller are demonstrated by some simulation and experimental results.

Key-Words: - Soft-Switching-Mode Rectifier, Small-Signal Model, Quantitative Controller Design, Parallel Operation, Robust Control.

1 Introduction

The conventional diode rectifiers possess the serious disadvantage of drawing pulse-type highly distorted line current from power source. Switching mode rectifier (SMR) with power factor correction (PFC) control can be employed to solve this problem [1]. The boost-type SMR is perhaps the most commonly used one owing to ease of making line current waveform shaping control. However, a boost-type SMR with hard switch exists in larger switching stresses, switching losses and electromagnetic interference (EMI). The soft-switching mode rectifiers (SSMRs) based on zero-voltage-transition (ZVT) technique is the easiest means in design and implementation aspects to lessen these problems [2].

The multi-module parallel SSMRs have the advantages of (i) providing more reliable power source; (ii) allowing the SSMR to be designed in modular fashion. A SSMR based on current-mode control possesses the equal current sharing or current programmable capability, so it is very suitable for multi-module parallel operation [3]. Before making the controller design, a mathematical model of SSMR is required for achieving output voltage regulation. However, the accurate plant transfer functions are difficult derived, particularly for multi-module parallel SSMRs. Although a dynamic model of a SSMR can be estimated from the command and load step response measurement, its correctness subjects to accuracy of the data measured at chosen operating point [4]. Moreover, as the constituted module change occurs, the small-signal model must be refreshed through the same procedure again. Unfortunately, for a multi-module parallel SSMR system, the number of paralleled SSMRs may change due to some SSMRs end or restart their operations. Hence the SSMR system model would be on the subject of the disturbances of load and system configuration variations. To let the SSMR possess good control performance, a lot of current and/or voltage control methods have been developed [5-8]. However, the adaptation of control for obtaining robust control performance is difficult to perform. It is well known that robust control is one of the most effective techniques for dealing with parameter variations. Although a robust control technique has been applied to many processes, it still seldom used for control of SSMRs [9-13]. Moreover, most of the existed robust control techniques are too complex in theoretic bases for practical engineers to completely understand. It follows that good control performances are general not able to be achieved.

In this paper, the dynamic modeling and quantitative controller design for the current and voltage control loops are made to achieve specified control performance at nominal case. The current controller is designed using frequency response method to let the current-controlled PWM scheme be normally operated [4]. As to the voltage control loop, the dynamic model is derived from system parameters and measurements at nominal operating point by averaging method [14]. Then it is employed to find the controller parameters systematically and quantitatively. Based on the designed voltage PI controller, a simple robust controller is proposed and augmented to reduce the performance degradations due to inaccurate plant modeling, the operating conditions and the system configuration changes. Some simulation and experimental results are provided to demonstrate the performance of the SSMR system and the effectiveness of the proposed control techniques.

2 The Proposed SSMR

Circuit configuration of the proposed SSMR is drawn in Fig. 1(a), which is formed from a boost-type SMR by augmenting with an auxiliary branch consisting of S_a, L_r, L_{r1}, C_r, D_a, and D_{r1}. The diode D_{r1} is employed to prevent undesired resonance forming by the resonant inductor and the parasitic capacitor of auxiliary switch, and saturable inductor L_{r1} is used to refrain the resonant current ripple caused by reverse recovery current of D_a and D_{r1}. The ZVT soft-switching is obtained by suitably delaying the turn-on instant of the PWM switching signal of the conventional SMR main switch, and within the delay period t_d the switching signal is applied to the auxiliary switch. The mechanism for generating the delayed switching signals for main PWM switches S and auxiliary switches S_a is shown in Fig. 1(b).

2.1 Circuit Operation and Governing Equations

The operation of this SSMR can be divided into seven modes; some key variables corresponding to these modes are list in Table 1. The waveforms of typical current and voltage waveforms are sketched in Fig. 2.

2.2 Circuit Design

The specifications of the proposed single-phase SSMR are given as follows:

- Input voltage: $v_{ac} = 110V_{rms} \pm 10\%$
- Power factor improved: $PF \geq 0.98$
- Input line frequency: $f = 60Hz$
- Maximum output power: $P_o = 600W$
- Output dc-link voltage: $V_o = 300V$
- Switching frequency: $f_s = 100kHz$ (Switching period： $T_s = 1/f_s = 10\,\mu s$)
- System efficiency at full load: $\eta \geq 85\%$

2.2.1 Power Circuit

A. Boosting inductor

The boost converter is designed to operate in continuous conduction mode, and the ramp-comparison current controlled PWM scheme is employed. Following the design procedure presented in [4], the boosting inductance L can be systematically found to be

$$L_m \geq 296.8(\mu H) \tag{1}$$

The measured inductance of the designed boosting inductor is $450\mu H$ at $100kHz$.

B. Output capacitor

Generally, the value of the output dc capacitor C_o depends on the hold-up time Δt_{hold}. Assume that $\Delta t_{hold} \geq 34ms$ and $V_{o(\min)} = 250V$, then

$$C_o \geq \frac{2P_o\Delta t_{hold}}{V_o^2 - V_{o(\min)}^2} = 1483\,(\mu F) \tag{2}$$

Accordingly, $C_o = 2000\mu F / 450V$ is chosen.

C. Power main switch components

According to the maximum current flowing through and voltage rating of the main switch S and the diode D, the power MOSFET IRFP460 (500V, 20A) and the fast diode RURP3060 (600V, 30A) are chosen for the main switch S and the diode D, respectively.

2.2.2 Auxiliary Resonant Branch

A. Resonant branch component and delay time

It follows from Fig.2 and Table 1, the determination of L_r and C_r can be made according to the following conditions [4]:

$$t_d > T_1 + T_2 = \frac{(\hat{I}_{Lm})_{\max}}{V_o} L_r + \frac{\pi}{2}\sqrt{L_r C_r} \tag{3}$$

$$\frac{V_o}{Z_o} = V_o\sqrt{\frac{C_r}{L_r}} < (\hat{I}_{Lm})_{\max} \tag{4}$$

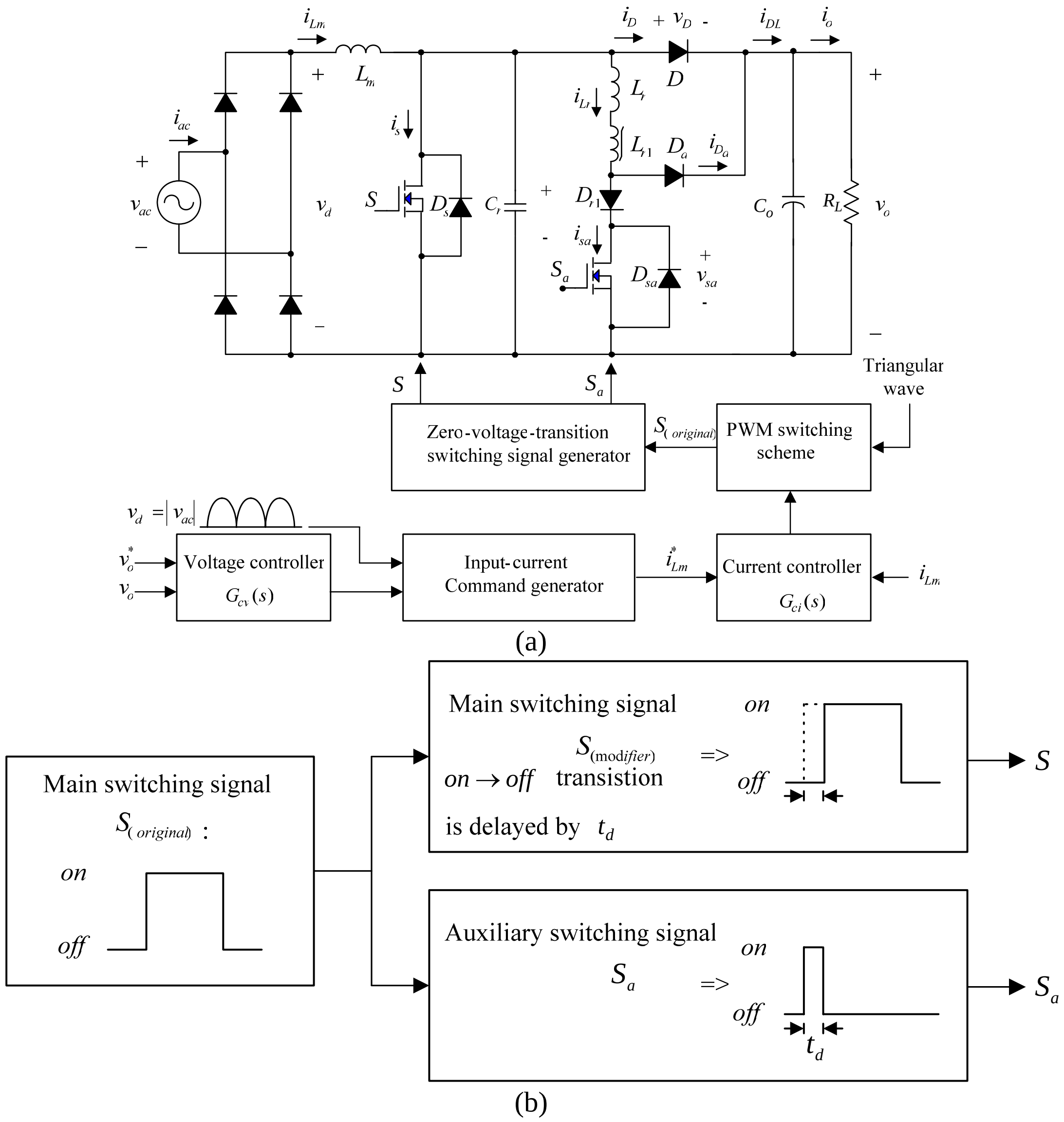


Fig. 1 (a) System configuration of the proposed SSMR; (b) the delayed switching signals for ZVT

Table 1 Some key variables at each operation mode of SSMR

Time period \ Variable	$v_{Cr}(t)$	$i_D(t)$	$i_{Da}(t)$
$T_1:[t_0 \sim t_1] = t_1 - t_0 = I_{Lm}L_r / V_o$	$v_{Co}(t)$	$i_{Lm}(t) + [v_{Co}(t)/L_r](t - t_0)$	0
$T_2:[t_1 \sim t_2] = t_2 - t_1 = \pi / 2(\sqrt{L_r C_r})$	$v_{Co}(t)\cos\omega_o(t - t_1)$	0	0
$T_3:[t_2 \sim t_3] = t_3 - t_2 = t_\varepsilon$	0	0	0
$T_4:[t_3 \sim t_4] = t_4 - t_3$ $= L_r / V_o(I_{Lm} + V_o / Z_o)$	0	0	$i_{Lm}(t) + v_{Co}(t)/Z_o$ $-[v_{Co}(t)/L_r](t - t_3)$
$T_5:[t_4 \sim t_5] = t_5 - t_4 = dT_s - \sum_i^4 T_i$	0	0	0
$T_6:[t_5 \sim t_6] = t_6 - t_5 = V_o C_r / I_{Lm}$	$[i_{Lm}(t)/C_r](t - t_5)$	0	0
$T_7:[t_6 \sim t_0] = (1-d)T_s - T_6$	$v_{Co}(t)$	$i_{Lm}(t)$	0

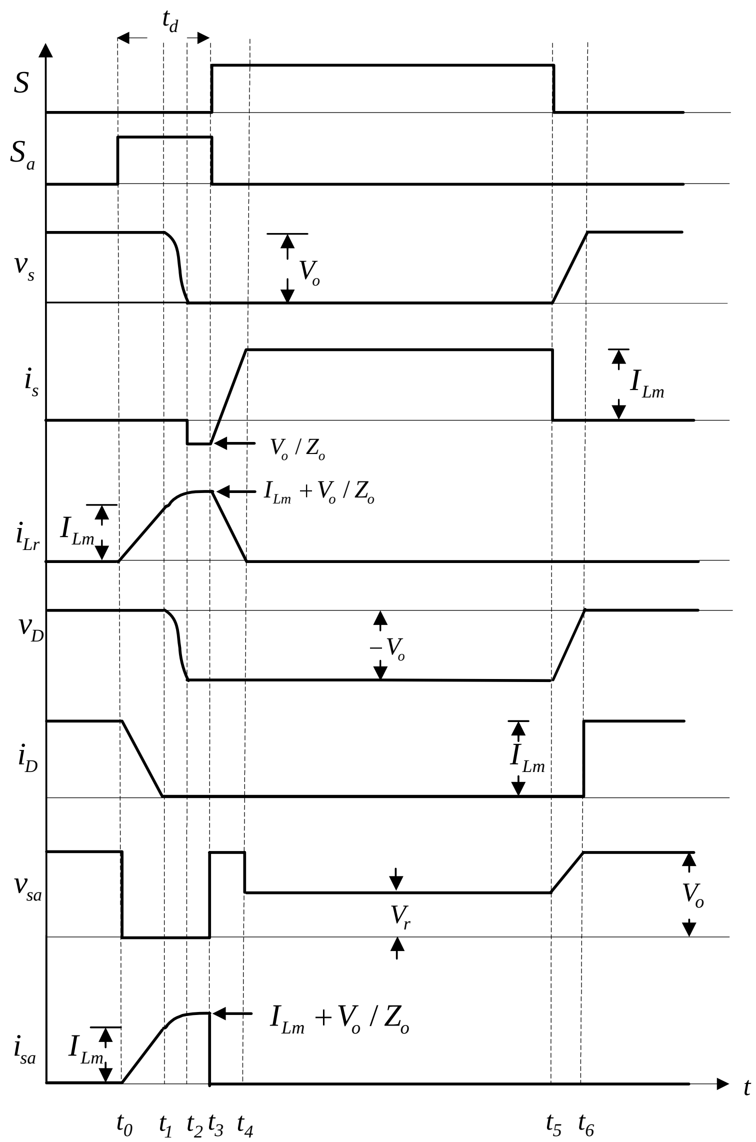


Fig. 2 Some key switching waveforms of the ZVT SSMR within one switching period

The parasitic capacitance of the main switch is measured (using HP4194) to be $870pF$ at $100kHz$. Then $C_r = 870pF$ is set for the zero external resonant capacitance. By specifying $t_d = 0.1T_s = 1\mu s$ and surplus amount $t_\varepsilon = 0.01T_s = 0.1\mu s$ within which D_s enters conduction state completely through the forward recovery process, the values of resonant inductor can be find from (3) $L_r = 52.66\mu H$, accordingly $L_r = 20\mu H$ is chosen.

B. Power auxiliary switch components

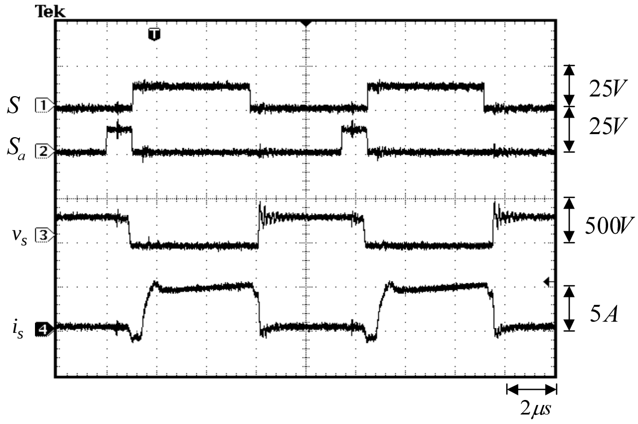
Since the maximum current and voltage rating of S_a are the same as those of the main switch S, the power MOSFET IRFP 460 and the fast diode RURP 3060 are also chosen for S_a, D_a and D_{r1}, respectively.

2.3 Measured Results

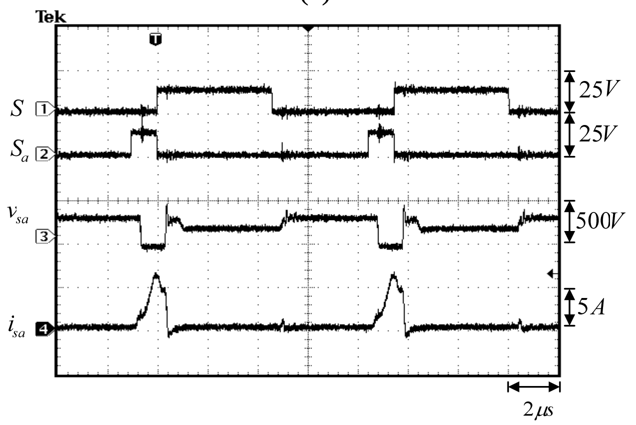
Some measured results of the main switch S and auxiliary switch S_a at output power $P_o = 300W$ are shown in Fig. 3. The results are all very close to the predicted ones shown in Fig. 2.

3 Multi-Module Parallel Configuration and Operation

To increase the total power capacity and the reliability of the SSMR system, the parallel connection configuration of multi-module is made in Fig. 4. Each of the single SSMR modules owns its current controller $G_{ci}(s)$, and the DC output voltages of all modules are connected in parallel. The control system is cascade arrangement and described in the following paragraph.



(a)



(b)

Fig. 3 Measured voltage and current waveforms of the designed ZVT SSMR at $v_{ac} = 110V_{rms}$, $V_o = 300V$ and $P_o = 300W$

A. Outer control loop

The outer control loop consists of a common voltage control scheme and a current distribution unit. The voltage control scheme yields a current magnitude command $\hat{i}_{Lm}$ through regulating the voltage tracking error. Then by multiplying $s(\omega t)$ with proper unit sine waves, the current command i^*_{Lm} for multi-module parallel SSMR is generated. The current command of each single-phase SSMR is made according to the following strategies:

$$i^*_{Lm} = \sum_{n=1}^{N} W_n i^*_{Ln} \tag{5}$$

The parameter W_n in (5) denotes a distribution factor of each single-phase SSMR. Its value depends on the capacity of each single-phase SSMR.

B. Inner control loop

The inner loop contains the current controlled PWM (CCPWM) scheme of all SSMR modules. Each of SSMR line current i'_{Ln} sensed from inductor is regulated to closely follow its command i^*_{Ln}. It leads to input current of each SSMR $i_{ac1} \sim i_{acN}$ in phase with v_{ac}.

4 Design of Current Control Loop

4.1 Dynamic Modeling

By neglecting the auxiliary branch of the SSMR power circuit shown in Fig. 1 and applying the well-known state space averaging method, one can derive the transfer function block diagram of the current control loop shown in Fig. 5. The transfer function from duty cycle Δd to inductor current $\Delta i'_{Lm}(s)$ in s-domain can be derived from Fig. 5 to be

$$G_{pi}(s) \overset{\Delta}{=} \left. \frac{\Delta i'_{Lm}(s)}{\Delta d(s)} \right|_{\Delta v_d(s)=0} = K_i \frac{R_L L_m V_o s + 2V_o}{R_L C_o L_m s^2 + L_m s + (1-D)^2 R_L} \tag{6}$$

Where D is the duty ratio of PWM, R_L is the load resistance and K_i is the current sensing factor ($K_i = 2V/A$ is set here).

4.2 Current Controller Design

The current-controlled ramp-comparison PWM scheme is realized in current control loop. For the ease of derivation and implementation, the current controller is chosen to be proportional-plus-integral (PI) type, which has the following transfer function:

$$G_{ci}(s) = \frac{K_{Pi}s + K_{Ii}}{s} \tag{7}$$

The simple rule of thumb $f_c \le 0.5 f_s$ is employed in performing the controller design [4], where f_c denotes the corner frequency of the closed-loop gain of the current loop.

The loop gain of the current loop can be derived to be:

$$LG(s) = \frac{G_{ci}(s)\frac{1}{\hat{V}_{tri}}K_i[R_L L_m V_o s + 2V_o]}{R_L C_o L_m s^2 + L_m s + (1-D)^2 R_L} \tag{8}$$

At the operation point ($V_o = 300V$, $P_o = 600W$, $V_d = 171V$), the load resistance and duty ratio can be founded as $R_o = 150\Omega$ and $D = 0.43$. The closed-loop corner frequency is chosen as $f_c = 0.5 f_s = 50kHz$, and through the help of computer-aided analysis, the proportional-integral current feedback controller is designed as:

$$G_{ci}(s) = \frac{K_{Pi}s + K_{Ii}}{s} = \frac{10s + 10000}{s} \tag{9}$$

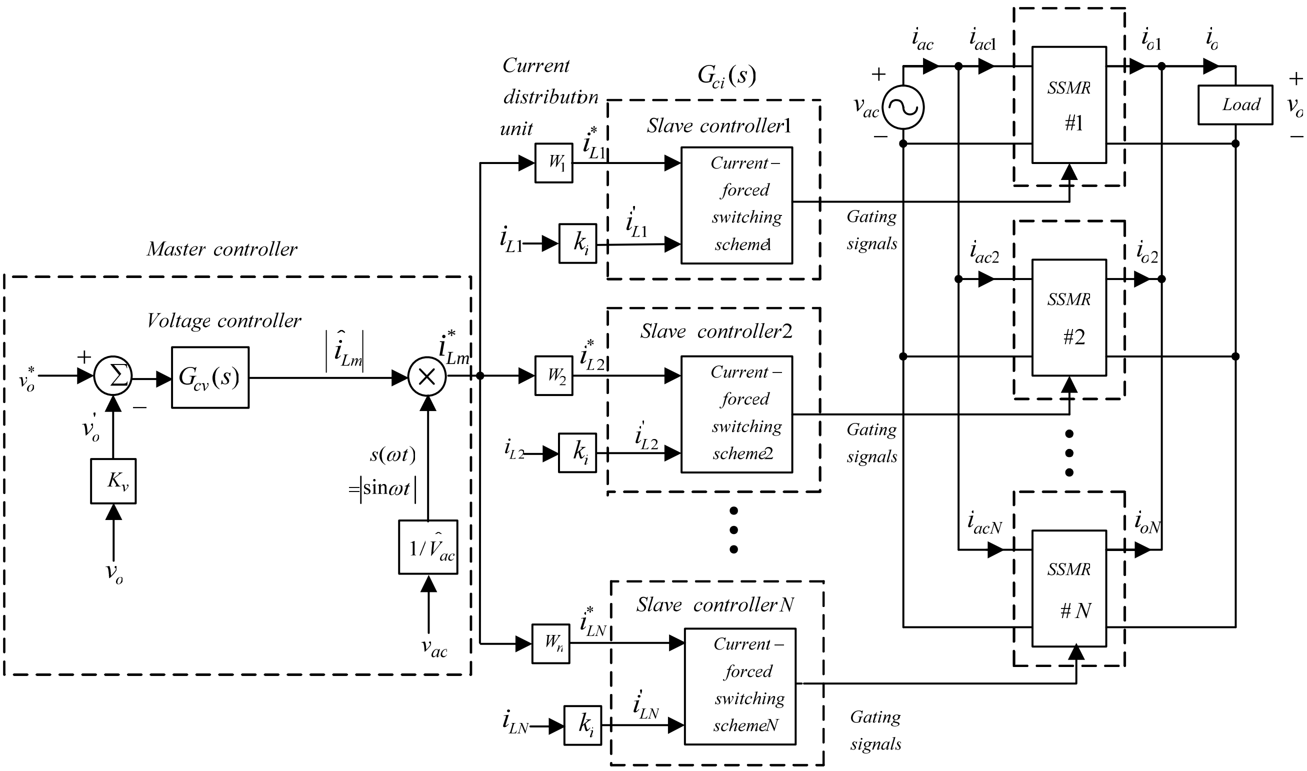


Fig. 4 Configuration of the proposed multi-module parallel SSMR system

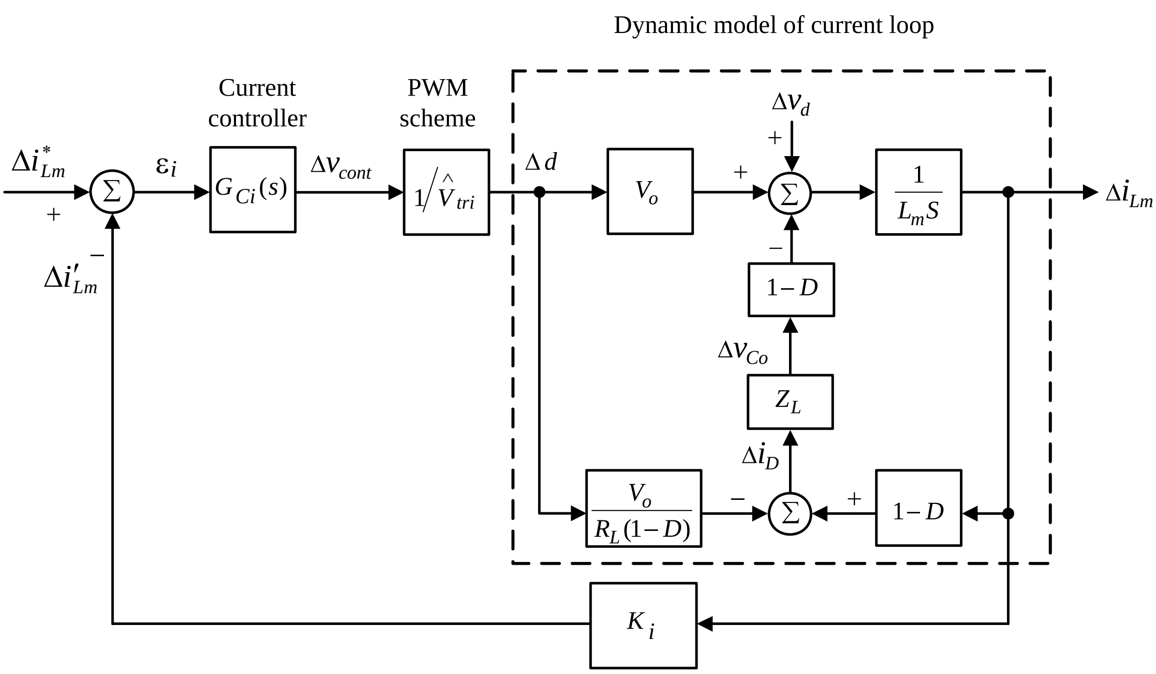


Fig. 5 The current loop control system block diagram of SSMR

5 Design of Voltage Loop

Assume that the input current i_{Lm} has tracked the command current i_{Lm}^* by using the well designed current controller, then the voltage loop dynamic behavior of the proposed parallel SSMR shown in Fig. 4 can be reasonably represented by the transfer function block diagram shown in Fig. 6, where $G_{cv}(s)$ is the PI type voltage controller, $G_p(s)$ is the plant transfer function, K_{pv} is the disturbance transfer ratio(K_{pv} =0.015V/W is measured here), and

K_v denotes the voltage sensing factor ($K_v = 0.02$ is set here).

5.1 Dynamic Modeling

Before making the controller design, the dynamic plant model of the proposed SSMR shown in Fig. 1 will be derived at nominal case. The proposed single-phase SSMR can be divided into two subcircuits, a fast response subcircuit and a slow response subcircuit. The former includes fast state variables $i_{Lr}(t)$ and $v_{Cr}(t)$. The latter includes slow state variables $i_{Lm}(t)$ and $v_{Co}(t)$. The equivalent circuit model of the SSMR is shown in Fig. 7(a) where the part enclosed by dotted line is the equivalent fast subcircuit. Current $i_{DL}(t)$ is the sum of diode currents $i_D(t)$ and $i_{Da}(t)$.

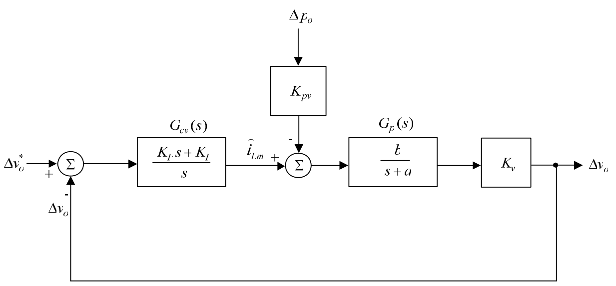


Fig. 6 Voltage loop control system block diagram of the multi-module parallel SSMR system

From a fast subcircuit point of view, the slow state variables in Fig.1 can be treated as constants. This leads to the results that $i_{Lm}(t) \approx I_{Lm}$ and $v_{Co}(t) \approx V_{Co} = V_o$. On the contrary, from a slow subcircuit point of view, only averaging behaviors of the fast state variables have effects on the slow state variables. As a result, substituting the fast variables by their moving averages, the averaged model of the slow subcircuit is then obtained. Viewing this, the state equation of the equivalent circuit model in Fig. 7(a) is given by

$$\begin{cases} \dfrac{di_{Lm}(t)}{dt} = \dfrac{v_d(t)}{L_m} - \dfrac{r_{Lm}}{L_m} i_{Lm}(t) - \dfrac{\bar{v}_{Cr}(t)}{L_m} \\ \dfrac{dv_{Co}(t)}{dt} = -\dfrac{v_{Co}(t)}{C_r R_L} + \dfrac{\bar{i}_{DL}(t)}{C_r} \end{cases} \quad (10)$$

Where $\bar{v}_{Cr}(t)$ and $\bar{i}_{DL}(t)$ are the moving average of $v_{Cr}(t)$ and $i_{DL}(t)$ within the switching period T_s, and from Table 1 which can be expressed as

$$\begin{aligned} \bar{v}_{Cr}(t) &= \left\langle v_{Cr}(t) \right\rangle_{T_s} = \frac{1}{T_s} \sum_{i=0}^{6} \int_{t_i}^{t_{i+1}} v_{Cr}(\tau) d\tau \\ &= v_{Co}(t)\left[d'(t) + \delta_1(t)\right] \end{aligned} \quad (11)$$

Where

$$\begin{cases} \delta_1(t) \overset{\Delta}{=} \dfrac{i_{Lm}(t) L_r}{T_s v_{Co}(t)} + \dfrac{1}{T_s \omega_o} + \dfrac{1}{2T_s} - \dfrac{v_{Co}(t) C_r}{T_s i_{Lm}(t)} \\ \omega_o \overset{\Delta}{=} \sqrt{\dfrac{1}{L_r C_r}} \end{cases} \quad (12)$$

$$\begin{cases} d(t) = \dfrac{T_1(t) + T_2(t) + T_3(t) + T_4(t) + T_5(t)}{T_s} \\ d'(t) = 1 - d(t) = \dfrac{T_6(t) + T_7(t)}{T_s} \end{cases} \quad (13)$$

$T_1(t) \sim T_7(t)$ denote the time of each mode operation of SSMR, and the switching period is defined as $T_s = \sum_{i=1}^{7} T_i$.

And

$$\begin{aligned} \bar{i}_{DL}(t) &= \left\langle i_{DL}(t) \right\rangle_{T_s} = \frac{1}{T_s} \sum_{i=0}^{6} \int_{t_i}^{t_{i+1}} [i_D(t) + i_{Da}(t)] d\tau \\ &= i_{LM}(t)[\delta_2(t) + d'(t)] \end{aligned} \quad (14)$$

where

$$\begin{cases} \delta_2(t) \overset{\Delta}{=} \dfrac{i_{Lm}(t) L_r}{T_s v_{Co}(t)} + \dfrac{L_r}{T_s Z_o} - \dfrac{v_{Co}(t) C_r}{2 T_s i_{Lm}(t)} \\ Z_o \overset{\Delta}{=} \sqrt{\dfrac{C_r}{L_r}} \end{cases} \quad (15)$$

It is interesting to see that the system in Fig. 1 is lossless, and thus, the average output power $\left\langle P_{out}(t) \right\rangle_{T_L}$ must be equal to the average input power $\left\langle P_{in}(t) \right\rangle_{T_L}$ over the line period $T_L = 1/120$ sec from an energy conservation point of view. From this viewpoint, the averaged model depicted in Fig. 7(a) can be transformed to the averaged model over the line period T_L, as shown in Fig. 7(b).

Assume that the input current $i_{Lm}^*(t)$ has tracked the command current $i_{Lm}^*(t)$ by using the well-designed inner-loop current controller and the shape of $i_{Lm}^*(t)$ is determined by $Kv_d(t)$, then

$$i_{Lm}(t) = i_{Lm}^*(t) = K v_d(t)\, \hat{i}_{Lm}(t) \quad (16)$$

And since, the amplitude of $i_{Lm}^*(t)$ is determined by $\hat{i}_{Lm}(t)$ which is more slowly varying than $Kv_d(t)$, the $\hat{i}_{Lm}(t)$ can be regarded as constant over the line period T_L. Therefore, the average of $i_{Lm}(t)$ within the line period can be found as

$$\begin{aligned}\left\langle i_{Lm}(t)\right\rangle_{T_L} &= K\hat{i}_{Lm}\left\langle v_d(t)\right\rangle_{T_L} = K\hat{i}_{Lm}v_{d(avg)} \\ &= \frac{2\sqrt{2}K}{\pi}\hat{i}_{Lm}v_{d(rms)} \overset{\Delta}{=} K_1\hat{i}_{Lm}v_{d(rms)}\end{aligned} \qquad (17)$$

Where $K_1 = \dfrac{2\sqrt{2}K}{\pi}$ and $v_{d(avg)}$, $v_{d(rms)}$ are the average and root-mean-square values of $v_d\,(t)$ over the line period T_L, respectively.

Substitution of $i^*_{Lm}(t)$ in (16) into $i_{Lm}(t)$ in (14) and tracking moving average over the line period T_L gives that

$$\begin{aligned}\left\langle \bar{i}_{DL}(t)\right\rangle_{TL} \overset{\Delta}{=} \left\langle\left\langle i_{DL}(t)\right\rangle_{T_s}\right\rangle_{T_L} &= \frac{K_1^2\pi^2 L_r\hat{i}_{Lm}^2 v_{d(rms)}^2}{8T_s v_o} + \frac{K_1 L_r\hat{i}_{Lm}v_{d(rms)}}{T_s Z_o} \\ &+ \frac{K_1\pi\,\hat{i}_{Lm}v_{d(rms)}^2}{2\sqrt{2}v_o} - \frac{C_r v_o}{2T_s}\end{aligned} \qquad (18)$$

To derive a small-signal model linearized around the operating point, the small perturbations are defined as follows:

$$\begin{aligned}
&\left\langle i_{Lm}(t)\right\rangle_{T_L} = I_{Lm} + \Delta i_{Lm}(t) && \text{with } \left|\Delta i_{Lm}(t)\right| << I_{Lm} \\
&v_{d(rms)}(t) = V_{d(rms)} + \Delta v_{d(rms)}(t) && \text{with } \left|\Delta v_{d(rms)}(t)\right| << V_{d(rms)} \\
&\hat{i}_{Lm}(t) = \hat{I}_{Lm} + \Delta\hat{i}_{Lm}(t) && \text{with } \left|\Delta\hat{i}_{Lm}(t)\right| << \hat{I}_{Lm} \\
&v_o(t) = V_o + \Delta v_o(t) && \text{with } \left|\Delta v_o(t)\right| << V_o \\
&\left\langle \bar{i}_{DL}(t)\right\rangle_{T_L} = I_{DL} + \Delta i_{DL}(t) && \text{with } \left|\Delta i_{DL}(t)\right| << I_{DL}
\end{aligned} \qquad (19)$$

Linearizing the voltage controller output $\hat{i}_{Lm}(t)$ in (17), the following dc part and ac part can be derived:

dc part:

$$I_{Lm} = K_1\hat{I}_{Lm}V_{d(rms)} \qquad (20)$$

ac part:

$$\begin{aligned}\Delta i_{Lm}(t) &= K_1V_{d(rms)}\Delta\hat{i}_{Lm}(t) + K_1\hat{I}_{Lm}\Delta v_{d(rms)}(t) \\ &\overset{\Delta}{=} g_f\Delta\hat{i}_{Lm}(t) + \frac{1}{r_f}\Delta v_{d(rms)}(t)\end{aligned} \qquad (21)$$

where

$$g_f \overset{\Delta}{=} K_1V_{d(rms)} \quad , \quad r_f \overset{\Delta}{=} \frac{1}{K_1\hat{I}_{Lm}} \qquad (22)$$

Similarly, from (18) one can derive

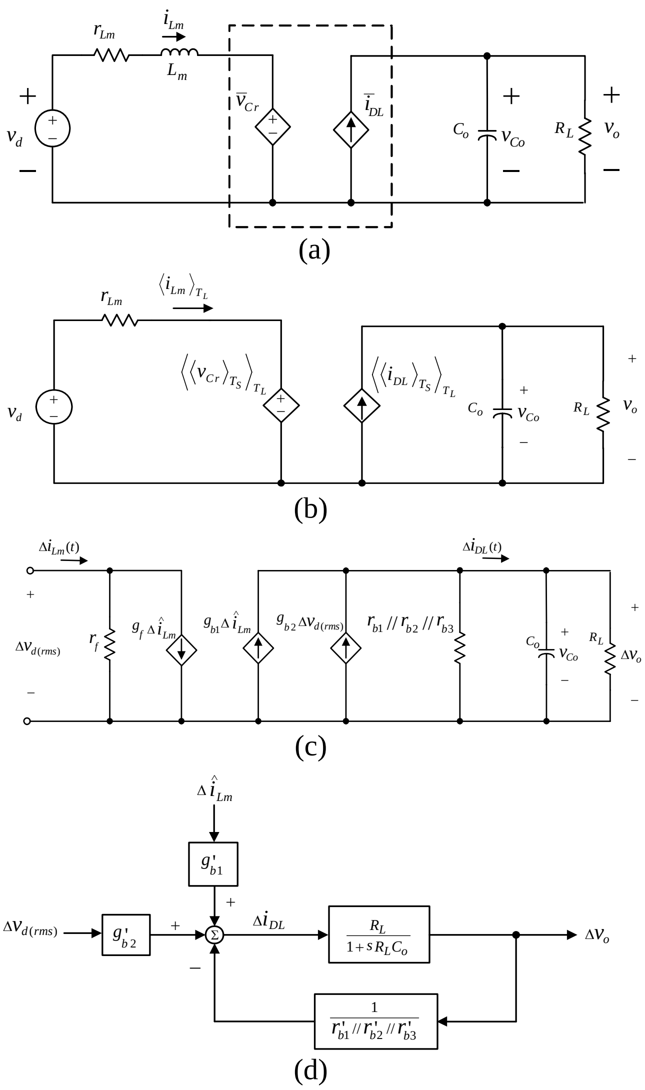


Fig. 7 (a) Averaged model of SSMR from a slow subsystem of view; (b) averaged model of SSMR over the line period T_L; (c)small-signal circuit model of single-module SSMR; (d)block diagram of the equivalent circuit of multi-module SSMR

dc part:

$$\begin{aligned}I_{DL} &= \frac{K_1\pi\hat{I}_{Lm}v_{d(rms)}^2}{2\sqrt{2}V_o} + \frac{K_1^2\pi^2L_r\hat{I}_{Lm}^2v_{d(rms)}^2}{8T_sV_o} \\ &+ \frac{K_1L_r\hat{I}_{Lm}v_{d(rms)}}{T_sZ_o} - \frac{C_rV_o}{2T_s}\end{aligned} \qquad (23)$$

ac part:

$$\Delta i_{DL}(t) = g_{b1}\Delta\hat{i}_{Lm}(t) + g_{b2}\Delta v_{d(rms)}(t) - \left[\frac{1}{r_{b1}} + \frac{1}{r_{b2}} + \frac{1}{r_{b3}}\right]\Delta v_o(t) \qquad (24)$$

where

$$\begin{aligned}g_{b1} &= \frac{K_1\pi V_{d(rms)}^2}{2\sqrt{2}V_o} + \frac{K_1^2\pi^2L_r\hat{I}_{Lm}V_{d(rms)}^2}{4T_sV_o} + \frac{K_1L_rV_{d(rms)}}{T_sZ_o} \\ &\overset{\Delta}{=} g_{b11} + g_{b12} + g_{b13}\end{aligned} \qquad (25)$$

$$g_{b2} = \frac{K_1 \pi \hat{I}_{Lm} V_{d(rms)}^2}{\sqrt{2} V_o} + \frac{K_1^2 \pi^2 L_r \hat{I}_{Lm} V_{d(rms)}}{4 T_s V_o} + \frac{K_1 L_r \hat{I}_{Lm}}{T_s Z_o} \quad (26)$$

$$\overset{\Delta}{=} g_{b21} + g_{b22} + g_{b23}$$

$$r_{b1} \overset{\Delta}{=} \frac{2\sqrt{2} V_o^2}{K_1 \pi \hat{I}_{Lm} V_{d(rms)}^2} = \frac{2\sqrt{2} V_o^2}{\pi I_{Lm} V_{d(rms)}} \quad (27)$$

$$r_{b2} \overset{\Delta}{=} \frac{8 T_s V_o^2}{K_1^2 \pi^2 L_r \hat{I}_{Lm}^2 V_{d(rms)}^2} = \frac{8 T_s V_o^2}{\pi^2 L_r I_{Lm}^2} \quad (28)$$

$$r_{b3} \overset{\Delta}{=} \frac{2T_s}{C_r} \quad (29)$$

Based on (21) and (24), the small-signal circuit model of single-module SSMR can be shown in Fig. 7(c). Suppose that the multi-module parallel SSMR system consists of N single identical modules but with different current distribution factor $W_1 \sim W_N$, one can find the single-module equivalent circuit from Fig. 7(c) with the following modifications:

$$g_f' = g_f \ , r_f' = r_f \quad (30)$$

$$g_{b1}' = N \times g_{b11} + g_{b12} + N \times g_{b13} \quad (31)$$

$$g_{b2}' = g_{b21} + (\sum_{i=1}^{N} W_i^2) \times g_{b22} + g_{b23} \quad (32)$$

$$r'_{b1} = r_{b1} \quad (33)$$

$$r_{b2}' = \frac{1}{\sum_{i=1}^{N} W_i^2} r_{b2} \quad (34)$$

$$r'_{b3} = \frac{r_{b3}}{N} \quad (35)$$

Based on (21), (24) and (30)-(35), the equivalent block diagram of the N-module parallel SSMR system can be derived as Fig. 7(d). The output voltage change $\Delta v_o(s)$ to control output $\Delta \hat{i}_{Lm}(s)$ (current command) change transfer function can be found as:

$$\left. \frac{\Delta v_o(s)}{\Delta \hat{i}_{Lm}(s)} \right|_{(v_{d(rms)}=0)} = \frac{g_{b1}' R_L}{s R_L C_o + \dfrac{R_L}{r_{b1}' // r_{b2}' // r_{b3}'} + 1} \quad (36)$$

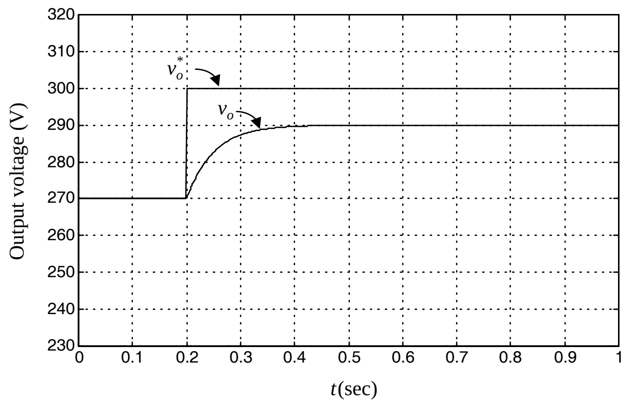
The experimental multi-module parallel SSMR system shown in Fig. 4 is assumed consisting of two modules (i.e. N=2) with $W_1 = 2/3$ and $W_2 = 1/3$. The parameters of the proposed single-module circuit model shown in Fig. 7(c) are listed below:

$v_{d(rms)} = 110V$, $L_m = 450\mu H$, $C_o = 2000\mu F$, $L_r = 20\mu H$, $C_r = 870pF$, $R_L = 150\Omega$ (nominal case), $T_s = 10\mu s$, $Z_s = 151.62\Omega$, K=5V/110V, $K_1 = 2\sqrt{2}K / \pi = 0.041$.

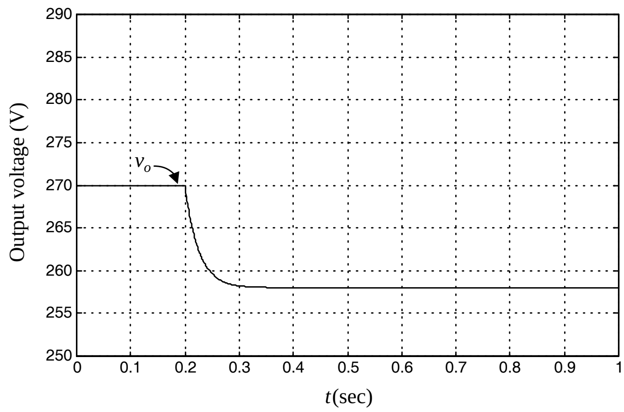
Then from (31) to (36) the dynamic model of the proposed two-module parallel SSMR system at nominal case ($R_L = 150\Omega,\ V_o = 270V,\ \hat{I}_{Lm} = 5A$) is derived to be

$$G_p(s) \overset{\Delta}{=} \left. \frac{\Delta v_o(s)}{\Delta \hat{i}_{Lm}(s)} \right|_{(\Delta v_{d(rms)}=0)} = \frac{b}{s+a} = \frac{83.333}{s+4.167} \quad (37)$$

The simulated voltage responses using the derived model due to voltage command $\Delta v_o^* = 30V$ and load power changes $\Delta p_o = 120W$ with voltage controller $G_{cv}(s) K_p = 5$ are shown in Figs. 8(a) and 8(b), respectively. The simulated results indicate that they are very close to the measured ones shown in Fig. 9(a) and 9(b) at same operation conditions. Thus, the accuracy of the derived dynamic model for multi-module SSMR is demonstrated.



(a)



(b)

Fig.8 Simulated output voltages of the two-module parallel SSMR system with $G_{cv}(s) = 5$ at the operation point ($V_o = 270V$, $P_o = 324W$): (a) due to step command change ($\Delta v_o^* = 30V$); (b) due to step load power change ($\Delta p_o = 120W$)

5.2 PI Type Voltage Controller Design

For achieving the desired control requirements with easy implementation, the following PI controller $G_{cv}(s)$ is chosen:

$$G_{cv}(s) = \frac{K_p s + K_I}{s} \tag{38}$$

From Fig. 6, the voltage output to load power disturbance closed-loop transfer function can be derived to be:

$$H_p(s) = \left.\frac{\Delta v_o}{\Delta p_o}\right|_{\Delta v_o^* = 0} = \frac{-sK_{pv}b}{s^2 + (a + bK_P)s + bK_I} \tag{39}$$

The following control requirements for the response of Δv_o due to step load power change at nominal case ($V_o = 270V, P_o = 324W$) are specified:

- Steady state error=0;
- Overshoot=0;
- The maximum voltage dip due to step load power change $\Delta p_o = 200W$ is $\Delta\hat{v}_{o,\max} = 8V$;
- The restore time is $t_r = 0.8s$, which is defined as the time at which $\Delta v_o(t = t_r) = 0.05\Delta\hat{v}_{o,\max}$.

Following the design procedure developed in [4], one can find the parameters of voltage controller $G_{cv}(s)$ as follows:

$$K_P = 12.51,\ K_I = 51.42 \tag{40}$$

5.3 The Proposed Robust Voltage Controller

When system configuration and plant parameter variations occur, the PI-type voltage controller designed for the nominal case can no longer satisfy the prescribed control requirements. To overcome this problem, a robust voltage controller based on direct cancellation of uncertainties is proposed in Fig. 10(a). A model error, denoted by e, is extracted using an inverse nominal plant model $G_I(s) \stackrel{\Delta}{=} (s + \bar{a})/(\bar{b}K_v)$, and then a compensation control signal, $\Delta I^* = we$, ($0 < w \le 1$), is generated for the purpose of disturbance cancellation. The plant model of multi-module parallel SSMR system can be represented as

$$G_p(s) = \frac{b}{s+a} \stackrel{\Delta}{=} \frac{1}{\alpha s + \beta} \tag{41}$$

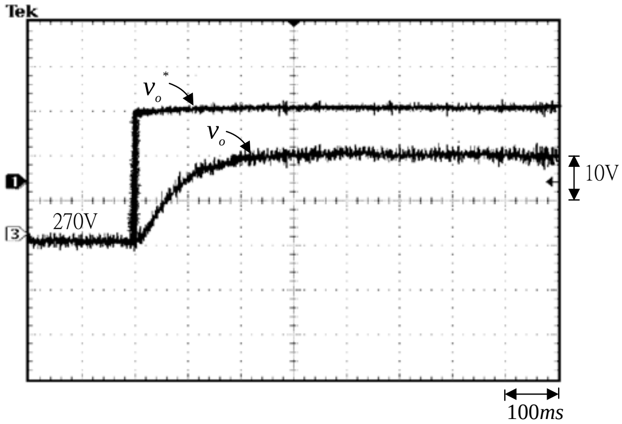
$$a \stackrel{\Delta}{=} \bar{a} + \Delta a, \text{ and } \alpha \stackrel{\Delta}{=} \bar{\alpha} + \Delta\alpha \tag{42}$$

$$b \stackrel{\Delta}{=} \bar{b} + \Delta b, \text{ and } \beta \stackrel{\Delta}{=} \bar{\beta} + \Delta\beta \tag{43}$$

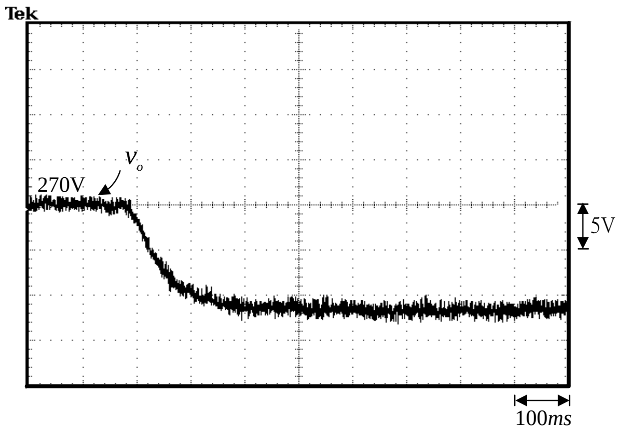
Where $\bar{\alpha}, \bar{\beta}, \bar{a}, \bar{b}$ are plant parameters at nominal case at which all parallel modules are normally operated. And $\Delta\alpha, \Delta\beta, \Delta a, \Delta b$ are system uncertainties. The transfer function of load disturbance Δp_o to output voltage Δv_o is derived as

$$\Delta v_o = \frac{\Delta\hat{i}_{Lm} - (1-w)k_{pv}\Delta p_o}{(\bar{\alpha} + (1-w)\Delta\alpha)s + (\bar{\beta} + (1-w)\Delta\beta)} K_v \tag{44}$$

An equivalent multi-module parallel SSMR system control block diagram corresponding to (44) is drawn in Fig. 10(b).



(a)



(b)

Fig. 9 Measured output voltages of the two-module parallel SSMR system with $G_{cv}(s) = 5$ at the operation point ($V_o = 270V$, $P_o = 324W$): (a) due to step command change ($\Delta v_o^* = 30V$); (b) due to step load power change ($\Delta p_o = 120W$)

Observations:

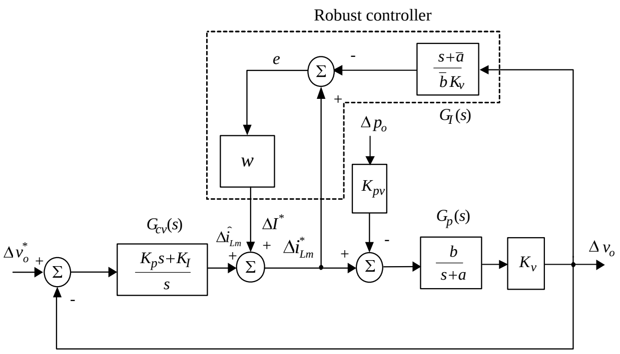
Some phenomena can be observed from the above transfer function:

(i) By using the robust control, the effects of load disturbance Δp_o and system uncertainties can be reduced by a factor of $(1-w)$.

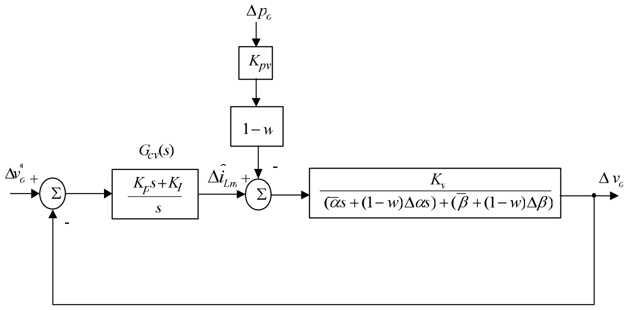
(ii) The larger value of w is chosen, the better control performance is obtained, but it is easier to yield instability due to the system nonlinearities.

(iii) For the ideal case ($w=1$), one can find from (44) that

$$\Delta v_o = \frac{\Delta \hat{i}_{Lm}}{\bar{\alpha}s+\bar{\beta}} K_v \quad (45)$$



(a)



(b)

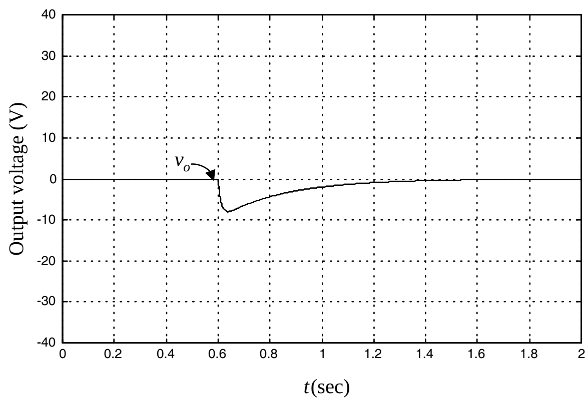
Fig. 10 (a)The proposed robust control scheme; (b) equivalent system of (a)

That is, all the load disturbances and uncertainties have completely eliminated by the compensation control signal ΔI^*. However of course, this ideal case is practically unrealizable. Thus suitable compromise between control performance and operating stability should be made.

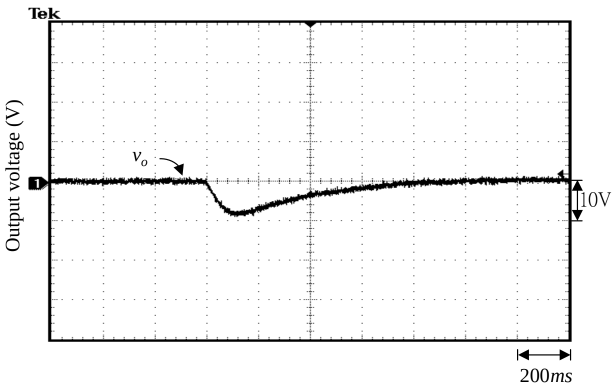
Hence for obtaining good performance without overshoot and taking into account the maximum control effort, the value w is set to 0.7 in this paper.

6 Simulation and Experimental Results

The simulated and experimental responses of Δv_o due to the step load change $\Delta p_o = 200W$ with the voltage controller parameters listed in (40) are shown in Fig. 11(a) and 11(b), respectively. The results indicate that the yielded dynamic response exactly satisfies the given specifications. Therefore, the validity of the developed dynamic model and the designed PI-type voltage controller is further confirmed. At the condition of ($v_{ac,rms}=110V$, $f=60Hz$, $V_o=300V$, $P_o=600W$), the measured i_{ac1} and i_{ac2} with v_{ac} of two module parallel SSMR system (W_1=2/3, W_2=1/3 i.e. $P_{o1}=400W$, $P_{o2}=200W$ are set) are shown in Fig. 12(a) and 12(b). One can find that the line drawn current of each module regulated to be lowly distorted sinusoidal with power factor closely to unity, and the load current is distributed according to the distribution factor set. If two modules in the parallel system are normally operated, the measured dynamic output voltage responses obtained by the PI and robust controllers under the load changes from 300 to 600W are shown in Figs. 13(a) and 13(b), respectively. The results show that better control performance obtained by adding the robust controller is clearly observed. If the load power kept at $P_o = 600W$, Figs. 14 and 15 show that output voltage responses yielded by the PI and the robust controllers when one module is suddenly fault and restarted its operation, respectively. It is clear from the results shown in Figs. 14 and 15 that the robust controller gives better intermodule load disturbance rejection characteristics.

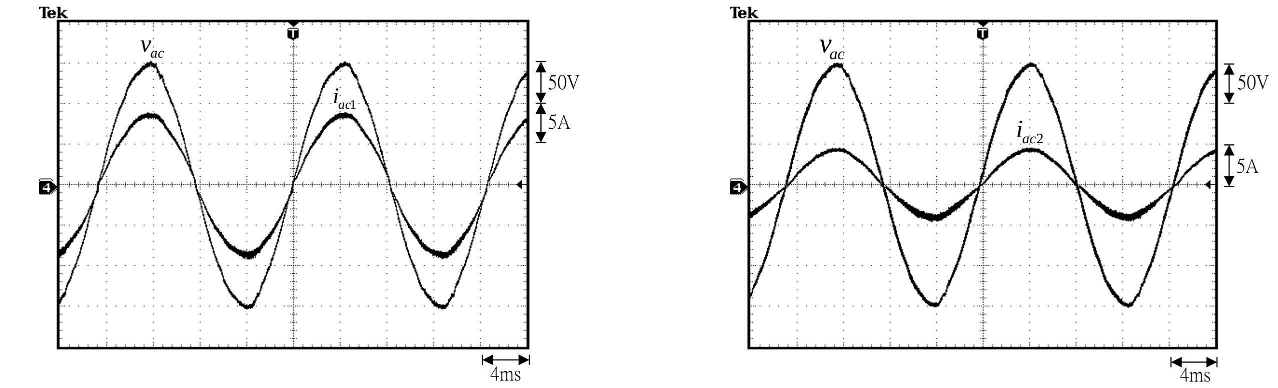


(a)



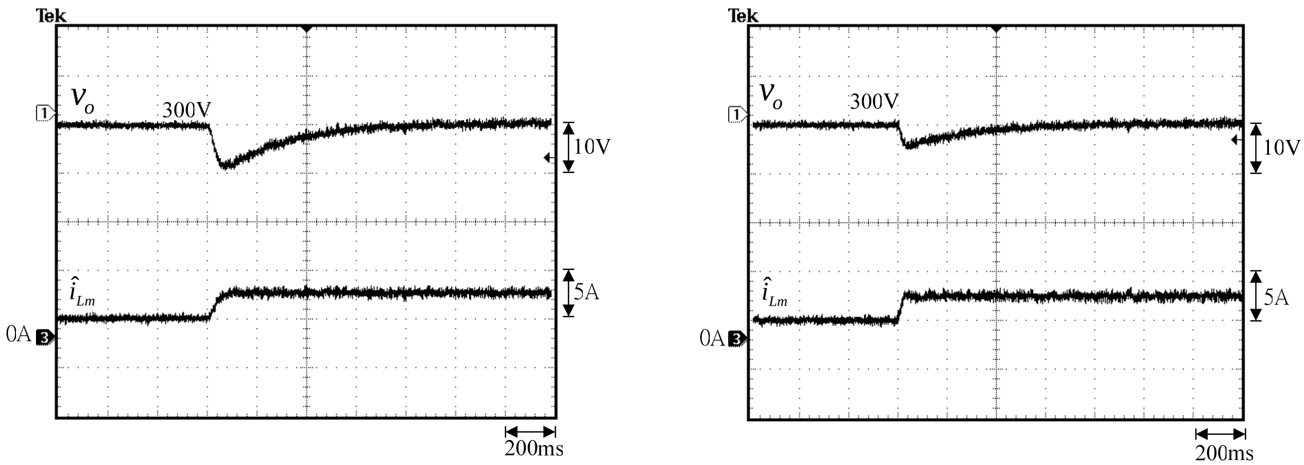
(b)

Fig. 11 The responses of output voltage Δv_o due to step load change of $\Delta p_o = 200W$ with the proposed PI-type voltage controller: (a) simulated results; (b) experimental results



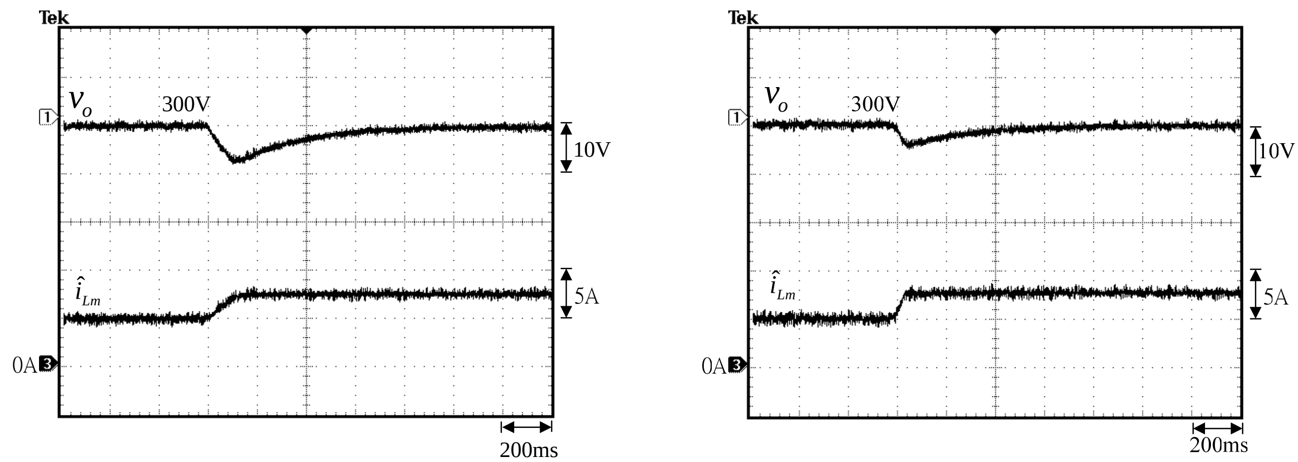
(a) (b)

Fig. 12 The measured input line current with v_{ac} of two module parallel SSMR system at ($v_{ac} = 110V$, $f = 60Hz$, $V_o = 300V$, $P_o = 600W$, $W_1 = 2/3$, $W_2 = 1/3$): (a) i_{ac1} with v_{ac}; (b) i_{ac2} with v_{ac}



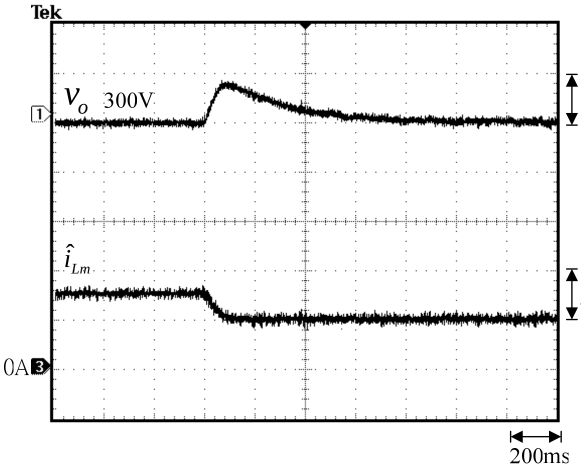
(a) (b)

Fig. 13 Measured dynamic output voltage responses due to step load changes from $P_o = 300W$ to $600W$ when two modules are normally operated: (a) PI controller; (b) robust controller

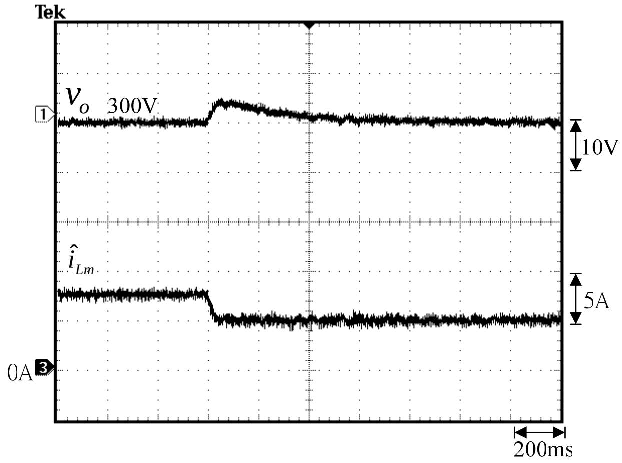


(a) (b)

Fig. 14 Measured dynamic output voltage responses (at load power $P_o = 600W$) when one module SSMR is suddenly turned off: (a) PI controller; (b) robust controller



(a)



(b)

Fig. 15 Measured dynamic output voltage responses (at load power $P_o = 600W$) when the turned off SSMR module is suddenly restored: (a) PI controller; (b) robust controller

7 Conclusion

The dynamic modeling, quantitative design and implementation of the proposed controller for a multi-module parallel ZVT SSMR system with current-controlled PWM scheme have been presented. An experimental ZVT SSMR is first established, and then the control for the multi-module parallel SSMR system is made. For the current-controlled PWM scheme, the small-signal model of current loop is obtained using state-space averaging method and the current controller parameters are found based on frequency response approach. Having derived the model of the multi-module parallel SSMR system, a systematical design technique has been adopted to find parameters of PI controller according the prescribed specifications. In addition, to let the dynamic responses of multi-module parallel SSMR system be insensitive to operating condition and parameter changes, a robust controller is designed and implemented. Validity of the proposed controller and the resulted performance of the SSMR have been confirmed by simulation and experimental results.

8 Acknowledgement

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