A Novel Control Strategy for Dynamic Voltage Restorer using Decoupled Multiple Reference Frame PLL (DMRF-PLL)

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Abstract: **-** This paper presents a new control scheme for dynamic voltage restorer (DVR), which consists of a set of series and shunt converters connected back-to-back (BTB), three series transformers, and a dc capacitor installed on the common dc-link. The DVR is characterized by installing the shunt converter on the source side and the series converter on the load side. A decoupled multiple reference frame phase-locked-loop (DMRF-PLL) is proposed, which decouples signals of different frequencies and eliminates interactions between the fundamental-frequency positive-sequence components and harmonic and/or negative-sequence components in the grid voltages. The proposed DMRF-PLL scheme achieves a fast, precise, and robust positive-sequence voltage detection even under unbalanced and/or distorted grid voltages conditions. A detailed description and derivation of the detection method is presented. Besides, a separate proportional-integral (PI) controller is adopted to regulate the dc-link capacitor voltage. The load voltage waveform is restored to be sinusoidal with fundamental frequency by dynamically injecting compensating voltages to the series brunch of converters. The validity and effectiveness of the presented scheme has been confirmed by extensive simulation results obtained from a 380V/50kVA system using Matlab/Simulink.

Key-Words: **-** Dynamic voltage restorer, decoupled multiple reference frame phase locked loop (DMRF-PLL), voltage sag detection, dc capacitor control, series converters, shunt converters, harmonic and unbalanced voltage compensation.

1 Introduction

Voltage sags in an electrical grid are well-known phenomenon due to the finite clearing time of the faults and the propagation of sags from the transmission and/or distribution system to the low-voltage loads. The theory of voltage sags and interruptions for electrical networks is thoroughly described in [1]. Dynamic voltage restorer (DVR) has been recognized as a cost effective solution for the protection of sensitive loads from voltage sags [2]. DVR is primarily used for the distribution system by injecting compensating voltage in series with the supply network when an upstream fault is detected [3]-[5]. Loads connected downstream of the DVR are thus protected from any voltage sags caused by faults elsewhere on the network.

The literature presents several control algorithms for the DVR. For example, the d-q-0 method is often used to determine the reference compensation voltage [6]-[7]. A novel control algorithm by use of PQR power theory was proposed in [8], which can generate the reference compensation voltages without using sag detection circuit that deteriorates dynamics of DVR. The instantaneous reactive power theory (IRPT) has been widely used for power converters, however, it is limited to situations where the supply voltages are pure sinusoidal, and the performance under distorted grid voltages is poor [9]-[10]. The symmetrical components estimation method is proposed in [11], which has some advantages, such as easy of implementation, fast convergence and less sensitivity to system parameter variations, but this method only considers the situation where the supply voltage waveforms are unbalanced.

To realize the aforementioned algorithms, the crucial prerequisite is the proper synchronization with the utility voltage. Specifically, the detection of the positive-sequence fundamental component of grid voltage is essential. The most popular technique used for the phase detection is the three-phase phase-locked-loop (PLL) based on the synchronous reference frame (SRF-PLL) [2]-[3], the SRF-PLL gives satisfactory performance under ideal input conditions, i.e. when the source voltage is balanced and free of harmonics. However, imbalance and

distortions in the supply voltage can cause large oscillations. Recently, a novel improvement called the decoupled double synchronous reference frame PLL (DDSRF-PLL) was proposed [12], which utilized double synchronous reference frames (DSRF) to process the input voltages. The two reference frames have the same angular speed, but rotating in opposite directions. Signals in the two reference frames are decoupled through a feedback network so that the interference between them can be totally eliminated. The technique had excellent performance even when input voltages were highly unbalanced. The effect of harmonics on the PLL was also investigated and the result showed that they have some impact on the detection of the positive-sequence fundamental component.

In this paper a new decoupled multiple reference frame phase-locked loop (DMRF-PLL) is proposed, which is based on DDSRF-PLL, however the structure of DDSRF is extended toward more generic scenarios , where not only positive- and negative-sequence components of the fundamental frequency, but the harmonic components are also taken into consideration . This PLL minimizes the detection error of the phase angle of the positive sequence fundamental component. It is achieved by decoupling signals of difference frequencies using multiple reference frame transformation which eliminates interactions between the fundamental-frequency positive-sequence components and harmonic and /or negative-sequence components in the utility voltage.

Moreover, the control strategy of the DVR system is also discussed. Many different topologies for DVRs and their performance are presented in [13].In this paper, the DVR with no energy storage and supply-side connected converter structure is adopted and the schematic diagram of DVR is shown in Fig.1. The DVR is composed of a shunt voltage source rectifier (VSR) on the source side and series voltage-source inverters (VSIs) on the load side using a common dc-link.

The structure of this paper is organized as follows: Section 2 reviews the DDSRF-PLL, and introduces the structure of the DMRF-PLL, and a comparison of performance between them is discussed. Section 3 discusses the corresponding control strategy of the DVR system including the feed-forward plus feed-back control scheme and the dc-link voltage control method. Finally extensive simulation results obtained from a 380V/50kVA system are presented to verify the performance of the proposed control strategy, which is verified that the DVR is not only suit for balanced voltage sag condition, but also for unbalanced or distorted voltage sag condition.

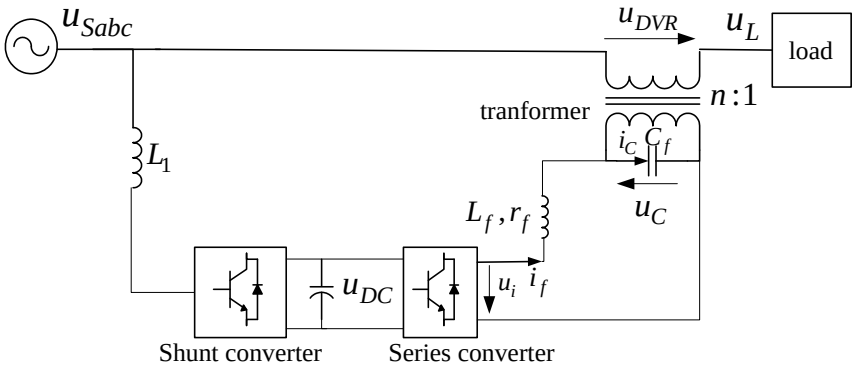


Fig.1. Schematic diagram of the DVR system

2 Structure of the DMRF-PLL

In order to generate a fast and accurate reference voltage, the most important aspect in the controller design process is to properly synchronize the system with the utility grid. Specifically, the detection of the positive-sequence fundamental component of grid voltage is essential for the precise control of DVR, even if the grid voltage is distorted and unbalanced.

A most extend technique used for this detection is based on a three-phase synchronous reference frame PLL (SRF-PLL), recently, based on the conventional SRF-PLL, a decoupled double synchronous reference frame PLL (DDSRF-PLL) was proposed [12], although the DDSRF-PLL works perfectly in case the utility voltage is unbalanced, which resolves the problem of SRF-PLL. However in the presence of high-order harmonic distortion in the utility voltage, there is some error in the phase angle estimation and some oscillations in the amplitude estimation of fundamental positive sequence component. However, in applications of dynamic voltage restorer (DVR), it requires high accuracy and a good dynamic response of PLL even under unbalanced or distorted utility voltage condition. Therefore, the conventional SRF-

PLL and the DSRF-PLL solutions may have drawbacks due to lack of estimation accuracy.

In this paper a new decoupled multiple reference frame phase-locked loop (DMRF-PLL) based on the DDSRF-PLL structure is proposed, which completely eliminates the detection errors of conventional SRF-PLL and DDSRF-PLL. The amplitude and the phase angle of the positive-sequence component are fast and accurately obtained, even when the utility voltage is under sag/swell, distorted or unbalanced.

The high estimation accuracy is achieved by regulating each component on its own rotating reference frame, not only positive- and negative-sequence components of the fundamental frequency, but also harmonic component, and then eliminate their interactions by using a decoupling network. Finally the positive- and negative-sequence components are precisely extracted and separated. The resultant MSRF–PLL results in a fast, precise, and robust positive-sequence voltage detection even under unbalanced and/or distorted grid conditions. A detailed description and derivation of the proposed detection method is presented in the following section.

Considering a three-phase three-wire system, the zero-sequence component is null. To introduce the DMRF-PLL, firstly, the double synchronous reference frame PLL is reviewed. It is supposed the voltage vector consisting two generic components rotating with $+\omega$ and $-\omega$ radius per second respectively, where ω is the fundamental frequency. The voltage vector in the $\alpha\beta$ plane is given as:

$$v_{S(\alpha\beta)}=\begin{bmatrix}v_{S\alpha}\\ v_{S\beta}\end{bmatrix}=V_S^{+1}\begin{bmatrix}\cos(\omega t+\phi^{+1})\\ \sin(\omega t+\phi^{+1})\end{bmatrix}+V_S^{-1}\begin{bmatrix}\cos(-\omega t+\phi^{-1})\\ \sin(-\omega t+\phi^{-1})\end{bmatrix} \tag{1}$$

The DSRF composed of two rotating reference axes: dq^{+1}, rotating with a positive direction and whose angular positive is θ, and dq^{-1}, rotating with a negative direction and whose angular positive is $-\theta$, Fig.2 shows the relative position of voltage vectors in $\alpha\beta$ plane and DSRF.

Hence the utility voltage in dq^{+1} and dq^{-1} axes can be expressed as:

$$v_{S(dq^{+1})}=\begin{bmatrix}v_{Sd^{+1}}\\ v_{Sq^{+1}}\end{bmatrix}=\left[T_{dq^{+1}}\right]v_{S(\alpha\beta)}$$

$$=V_S^{+1}\begin{bmatrix}\cos(\omega t+\phi^{+1}-\theta)\\ \sin(\omega t+\phi^{+1}-\theta)\end{bmatrix}+V_S^{-1}\begin{bmatrix}\cos(-\omega t+\phi^{-1}-\theta)\\ \sin(-\omega t+\phi^{-1}-\theta)\end{bmatrix} \tag{2a}$$

$$v_{S(dq^{-1})}=\begin{bmatrix}v_{Sd^{-1}}\\ v_{Sq^{-1}}\end{bmatrix}=\left[T_{dq^{-1}}\right]v_{S(\alpha\beta)}$$

$$=V_S^{-1}\begin{bmatrix}\cos(-\omega t+\phi^{-1}+\theta)\\ \sin(-\omega t+\phi^{-1}+\theta)\end{bmatrix}+V_S^{+1}\begin{bmatrix}\cos(\omega t+\phi^{+1}+\theta)\\ \sin(\omega t+\phi^{-1}+\theta)\end{bmatrix} \tag{2b}$$

Where

$$\left[T_{dq^{+1}}\right]=\begin{bmatrix}\cos\theta & \sin\theta\\ -\sin\theta & \cos\theta\end{bmatrix},\left[T_{dq^{-1}}\right]=\begin{bmatrix}\cos\theta & -\sin\theta\\ \sin\theta & \cos\theta\end{bmatrix}$$

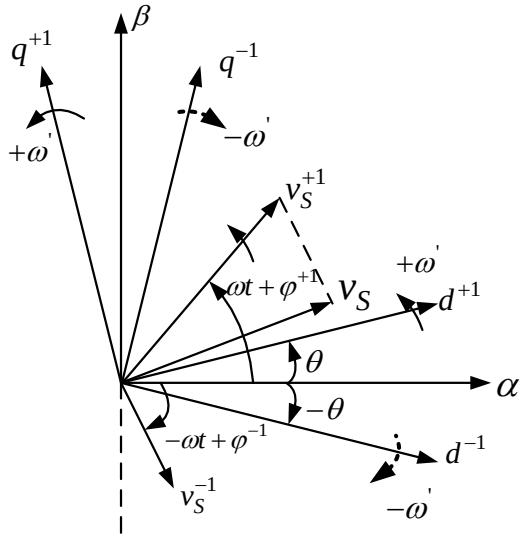


Fig.2 voltage vectors and axes of DSRF

If a precise synchronization of the proposed PLL is achieved, hence $\theta=\omega t$. Therefore, equation (2) can be rearranged as:

$$v_{S(dq^{+1})}=V_S^{+1}\begin{bmatrix}\cos(\phi^{+1})\\ \sin(\phi^{+1})\end{bmatrix}+V_S^{-1}\begin{bmatrix}\cos(-\omega t+\phi^{-1}-\omega t)\\ \sin(-\omega t+\phi^{-1}-\omega t)\end{bmatrix}$$

$$=V_S^{+1}\begin{bmatrix}\cos(\phi^{+1})\\ \sin(\phi^{+1})\end{bmatrix}+V_S^{-1}\cos(\phi^{-1})\begin{bmatrix}\cos(2\omega t)\\ -\sin(2\omega t)\end{bmatrix}$$

$$+V_S^{-1}\sin(\phi^{-1})\begin{bmatrix}\sin(2\omega t)\\ \cos(2\omega t)\end{bmatrix} \tag{3a}$$

$$v_{S(dq^{-1})}=V_S^{-1}\begin{bmatrix}\cos(\phi^{-1})\\ \sin(\phi^{-1})\end{bmatrix}+V_S^{+1}\begin{bmatrix}\cos(\omega t+\phi^{+1}+\omega t)\\ \sin(\omega t+\phi^{+1}+\omega t)\end{bmatrix}$$

$$=V_S^{-1}\begin{bmatrix}\cos(\phi^{-1})\\ \sin(\phi^{-1})\end{bmatrix}+V_S^{+1}\cos(\phi^{+1})\begin{bmatrix}\cos(2\omega t)\\ \sin(2\omega t)\end{bmatrix}$$

$$+V_S^{+1}\sin(\phi^{+1})\begin{bmatrix}-\sin(2\omega t)\\ \cos(2\omega t)\end{bmatrix} \tag{3b}$$

In (3a), the amplitude of the signal oscillation in the dq^{+1} axes depends on the mean value of the signal in the dq^{-1} axes. It can be easily understand that in the steady state, the following results can be satisfied:

$$\begin{cases} \overline{V_{Sd}^{+1}} = V_S^{+1}\cos\phi^{+1}, \overline{V_{Sq}^{+1}} = V_S^{+1}\sin\phi^{+1} \\ \overline{V_{Sd}^{-1}} = V_S^{-1}\sin\phi^{-1}, \overline{V_{Sq}^{-1}} = V_S^{-1}\sin\phi^{-1} \end{cases} \quad (4)$$

Therefore, to cancel the oscillations in the dq^{+1} axes signals, the decoupling cell shown in Fig.3 is obtained, for canceling out the oscillations in the dq^{-1} axes signals, the same structure may be used by interchanging +1 and -1 in Fig.3.

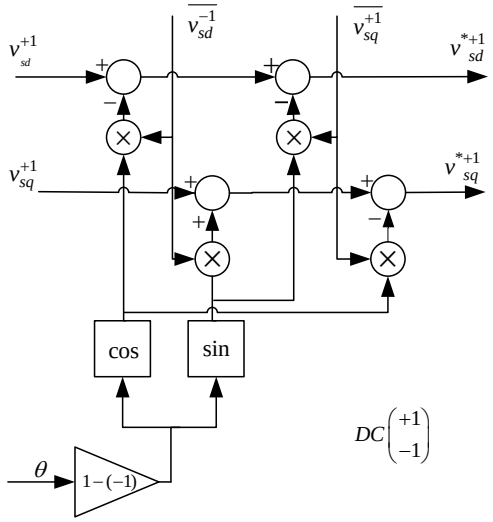


Fig.3 decoupling cell on the dq^{+1} frame signals

Logically, for a correct operation of both decoupling cells, it is crucial to get the value of $\overline{V_{Sd^{+1}}}$, $\overline{V_{Sq^{+1}}}$, $\overline{V_{Sd^{-1}}}$, $\overline{V_{Sq^{-1}}}$, Which can be got by using the low pass filter on the signals $V_{Sd^{+1}}^*, V_{Sq^{+1}}^*, V_{Sd^{-1}}^*, V_{Sq^{-1}}^*$ .A cross feedback decoupling network of DDSRF-PLL shown in Fig.4 is presented , it is based on a conventional three-phase SRF-PLL structure and its performance improvement comes from the decoupling network added to DSRF. The decoupling network of DSPF-PLL cancels out the double frequency oscillations at 2ω in $V_{Sq^{+1}}^*$, then $V_{Sq^{+1}}^*$ is applied to the input of the proportional-integral (PI) controller and later integrated in order to obtain θ. The drawback of this PLL was proposed in the forward section, therefore the decoupled multiple reference frame PLL is introduced in the following section.

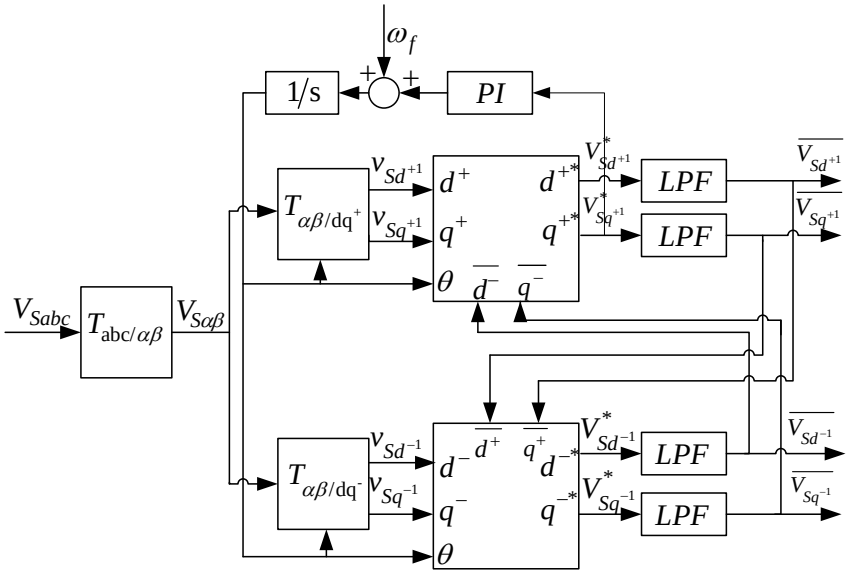


Fig. 4 Block diagram of the DSRF-PLL

In order to introduce the multiple reference frames, the above analysis is extended toward more generic scenarios, where not only two, but more voltage components should be considered. The voltage vector in the $\alpha\beta$ plane is expressed as the sum of a series of different frequency signals, that is

$$v_{S(\alpha\beta)} = \begin{bmatrix} v_{S\alpha} \\ v_{S\beta} \end{bmatrix} = \sum_{i=0}^{h} V_S^{m_i} \begin{bmatrix} \cos(m_i\omega t + \phi^{m_i}) \\ \sin(m_i\omega t + \phi^{m_i}) \end{bmatrix} \quad (5)$$

Where m_i can be positive or negative integer, $V_S^{m_i}$ and ϕ^{m_i} are respectively the magnitude and phase angle of the m_i frequency component. Then

considering a rotating reference frame, dq^{m_N} whose angular position is $m_N\theta$, m_N is one of $\{m_0, m_1, ..., m_h\}$.

$$v_{S(dq^{m_N})} = \left[T_{dq^{m_N}}\right] v_{S(\alpha\beta)}$$
$$= V_S^{m_N}\begin{bmatrix}\cos(\phi^{m_N})\\ \sin(\phi^{m_N})\end{bmatrix} + \sum_{\substack{i=0\\ i\neq N}}^{h} V_S^{m_i}\cos(\phi^{m_i})\begin{bmatrix}\cos((m_N - m_i)\omega t)\\ -\sin((m_N - m_i)\omega t)\end{bmatrix}$$
$$+ \sum_{\substack{i=0\\ i\neq N}}^{h} V_S^{m_i}\sin(\phi^{m_i})\begin{bmatrix}\sin((m_N - m_i)\omega t)\\ \cos((m_N - m_i)\omega t)\end{bmatrix} \quad (6)$$

Where $\left[T_{dq^{m_N}}\right] = \begin{bmatrix}\cos m_N\theta & \sin m_N\theta\\ -\sin m_N\theta & \cos m_N\theta\end{bmatrix}$

In (6), the amplitude of the signal oscillation in the dq^{m_N} axes depends on the mean value of the signal in the dq^{m_i} axes ($m_i = m_0, m_1, ...m_h$ except m_N). In order to cancel the oscillations in the dq^{m_N} axes signals, the same decoupling cells shown in Fig.3 is obtained, however the number of decoupling cells increases, in each part consists of $m_h - 1$ decoupling cells (DC) as shown in Fig.5.According to the principle proposed in formula (4), in the steady state, the following can be obtained:

$$\overline{V_{Sd^{m_i}}} = V_S^{m_i}\cos(\phi^{m_i}), \overline{V_{Sq^{m_i}}} = V_S^{m_i}\sin(\phi^{m_i}) \quad (7)$$

where $i = 0,1,2...,h$.

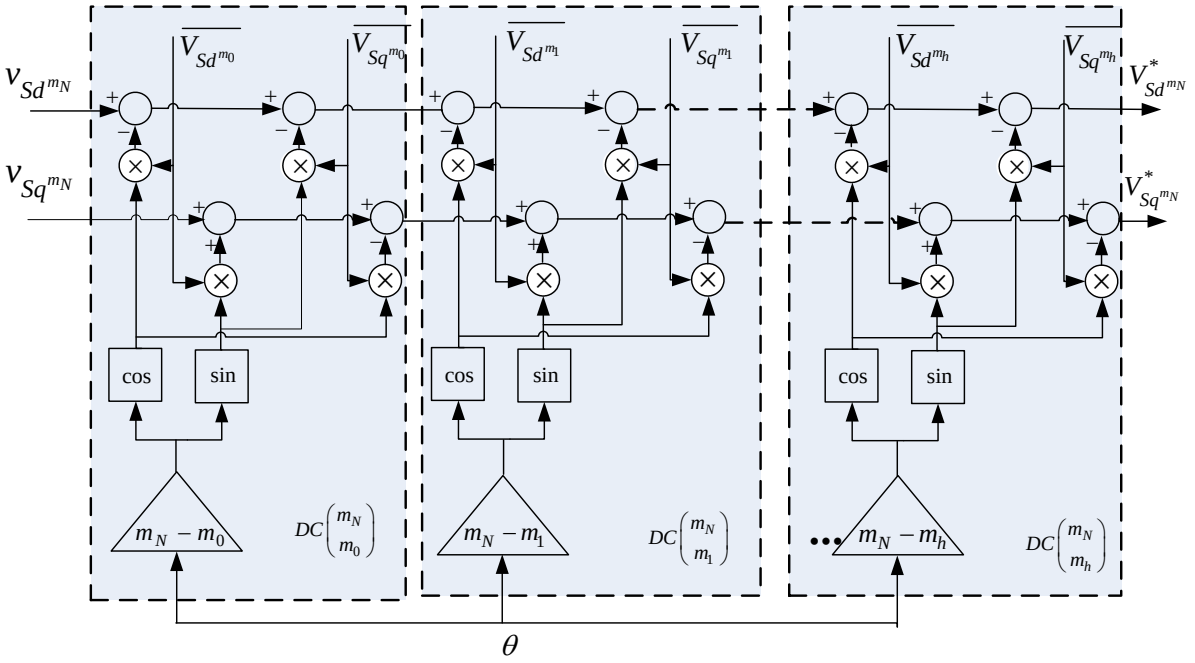


Fig.5 Decoupling cells for cancelling the signal oscillation on the dq^{m_N} frame signals

Logically, for a correct operation of each decoupling cells, it is crucial to get the value of $\overline{V_{Sd^{m_i}}}$, $\overline{V_{Sq^{m_i}}}$ ($i = 0,1,...h$). Then, the cross feedback decoupled multiple reference frame (DMRF) network shown in Fig.6 is proposed. In this decoupling network the block *LPF* is a one-order low-pass filer such as

$$LPF(s) = \frac{\omega_f}{s + \omega_f} \quad (8)$$

Where ω_f is the cut-off frequency, a detailed design of this parameter has been given in [14]. There exists a clear trade-off between dynamic response and stability, thus in this paper, $\omega_f = 2\times\pi\times 50/\sqrt{2}\, rad/s$.

Fig.6 can be seen as a generalized version of decoupled multiple reference frames (DMRF) synchronous estimator, as can be seen in this figure, a three-phase voltage signal is processed by several parallel channels, each representing a frame of reference ($m_0, m_1, ...m_h$). The inputs of each decoupling cell are obtained by the transformation shown in the expression (6).

This DMRF structure subtracts the sum of all estimated component from the original signal, and adds to it the estimated component resulted from the specific reference frame the signal is being to transform into. In the steady state, this cross feedback decoupling network allows only one component to pass through each reference frame, and

that component is exactly the one that is in synchronization with the reference frame. Therefore, the scheme essentially decouples all the different reference frames so that the output of each channel contains only constant quantities, which are the *d*-axis and *q*-axis values of the voltage signal set that rotates synchronously with the reference frame. In other words, the DMRF structure is capable of extracting cleanly fundamental frequency and harmonic component in the input signal either positive- or negative- sequence.

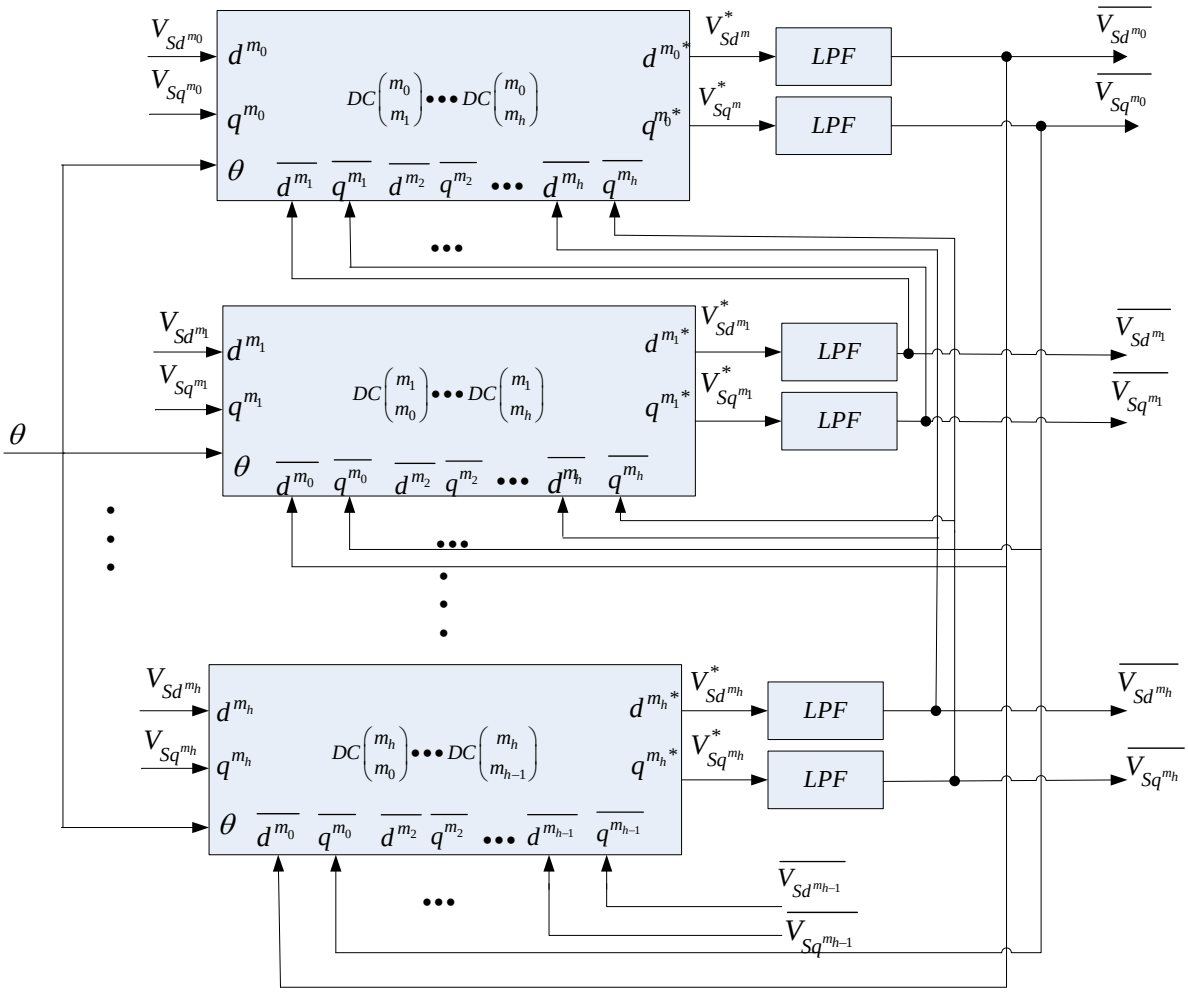


Fig.6 Block diagram of the decoupled multiple reference frame (DMRF) network

To demonstrate the intuitive explanation of the decoupling network shown in Fig.6, formal mathematical justification is necessary. Beginning from the block diagram in Fig.6, to an arbitrary channel $m_N \in \{m_0, m_1, ..., m_h\}$, the following functions (9) and (10) can be obtained:

$$\overline{V_{Sd}^{m_N}}(s) = \frac{\omega_f}{s+\omega_f}(V_{Sd}^{m_N}(s) - \sum_{i=0, i\neq N}^{h} \cos((m_N - m_i)\omega t) * \overline{V_{Sd}^{m_i}}(s) - \sum_{i=0, i\neq N}^{h} \sin((m_N - m_i)\omega t) * \overline{V_{Sq}^{m_i}}(s) \quad (9)$$

$$\overline{V_{Sq}^{m_N}} = \frac{\omega_f}{s+\omega_f}(V_{Sq}^{m_N}(s) + \sum_{i=0, i\neq N}^{h} \sin((m_N - m_i)\omega t) * \overline{V_{Sd}^{m_i}}(s) - \sum_{i=0, i\neq N}^{h} \cos((m_N - m_i)\omega t) * \overline{V_{Sq}^{m_i}}(s) \quad (10)$$

Where * represents the convolution product of the signals in the s-domain. Transform the above formula into time domain and substituting (6), and simplifying yields the following formula:

$$\frac{1}{\omega_f}\dot{\overline{V_{Sd}^{m_N}}} = -\sum_{i=0}^{h} \cos((m_N - m_i)\omega t) \times (\overline{V_{Sd}^{m_i}} - V_S^{m_i} \cos(\phi^{m_i})) - \sum_{i=0}^{h} \sin((m_N - m_i)\omega t) \times (\overline{V_{Sq}^{m_i}} - V_S^{m_i} \sin(\phi^{m_i})) \quad (11)$$

$$\frac{1}{\omega_f}\dot{\overline{V_{Sq}^{m_N}}} = \sum_{i=0}^{h} \sin((m_N - m_i)\omega t) \times (\overline{V_{Sd}^{m_i}} - V_S^{m_i} \cos(\phi^{m_i})) - \sum_{i=0}^{h} \cos((m_N - m_i)\omega t) \times (\overline{V_{Sq}^{m_i}} - V_S^{m_i} \sin(\phi^{m_i})) \quad (12)$$

Although DMRF structure provided a fast and accurate means to estimate individual harmonic components in a three-phase periodic signal, it has not been widely adopted in practical applications. One drawback of the DMRF implementation is that it

requires very intensive computational power to perform the transformations of different reference frames. For each harmonic component, signals need to be transformed into the *dq* reference frame, therefore for practical implementation with DSP, the DMRF structure presents hardware and software challenges, especially when the number of harmonic channels is high.

In order to apply DMRF in DVR control, one major challenge is to reduce the amount of calculations it requires. For a three-phase three-wire system, the following assumption is given: the supply voltage almost consists of positive sequence fundamental frequency, negative sequence fundamental frequency, fifth order negative sequence , seventh order positive sequence component, furthermore, the higher the frequency is, the lower the magnitude is, therefore higher frequency components can be negligible [15].

Based on the above assumption, only four components are considered in the decoupling cell in Fig.6, then a modified DMRF-PLL scheme is proposed in this paper, which is just considering the case that $m_0 = 1$, $m_1 = -1, m_2 = -5, m_3 = 7$. The block diagram of the scheme is shown in Fig.5, where the superscript +1 ,-1, -5,+7 stand for fundamental frequency positive sequence, negative sequence,-5 fifth harmonic negative sequence, seventh harmonic positive sequence component s.

This DMRF-PLL, as shown in Fig.7, is based on a conventional three-phase SRF-PLL structure and its performance improvement comes from the decoupling network added to MRF. The decoupling network of DMPF-PLL cancels out the double frequency oscillations at 2ω, 6ω in $V_{Sq^{+1}}^{*}$, therefore, the real amplitude of the positive sequence voltage component is indeed exactly detected, then $V_{Sq^{+1}}^{*}$ is applied to the input of the proportional-integral (PI) controller and later integrated in order to obtain θ,

$$\omega_{err} = (k_p + \frac{k_i}{s}) \times (V_{Sq^{+1}}^{*} - 0) \tag{13}$$

The selection of k_p and k_i is based on the small-signal analysis reported in [14].

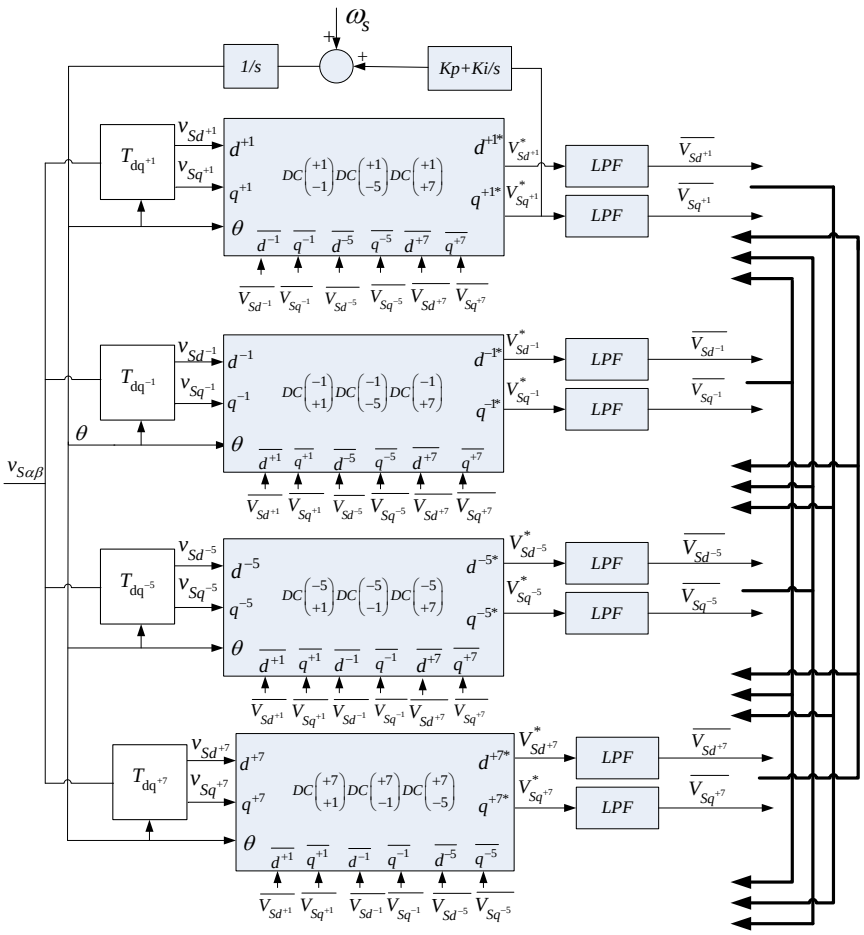


Fig.7. Block diagram of the DMRF-PLL

To show the promising behavior of the proposed DMRF-PLL, two kinds of grid operating conditions are considered in the following simulation:

(i) Unbalanced grid voltage condition:

$V_s^{+1} = 380V$, $V_s^{-1} = 114V$, $\phi^{+1} = \phi^{-1} = 0^\circ$;

(ii)Unbalanced and distorted grid voltage condition:

$V_s^{+1} = 380V$, $V_s^{-1} = 76V$, $V_s^{-5} = 38V$, $V_s^{+7} = 22V$.

$\phi^{+1} = \phi^{-1} = 0^\circ$, $\phi^{-5} = 0^\circ$, $\phi^{+7} = 0^\circ$

In both simulations, the PI control parameters are set to $k_p = 0.3$, $k_i = 20$. The cut-off frequency of the LPF is set to $50/\sqrt{2}$ HZ. The plots of column (a) and column (b) in Fig.8 show the response of the DMRF–PLL under the conditions (i) and (ii) respectively, Fig.8.a shows the utility voltage, Fig.8.b-c respectively show the estimated angular speed ω ,and the detected amplitude $\overline{V_{Sd}^{+1}}$,for the fundamental frequency positive sequence voltage component, Fig.8.c also shows the evolution of the signal at the input of the PLL controller, $V_{Sq^{+1}}^*$,which is free of oscillation at 2ω and 6ω thanks to the action of the decoupled multiple reference frame network. Fig.8.d shows the detected phase angle θ , Fig.8.e shows the detected amplitude for the fundamental frequency negative sequence, fifth harmonic negative sequence, and seventh harmonic positive sequence components.

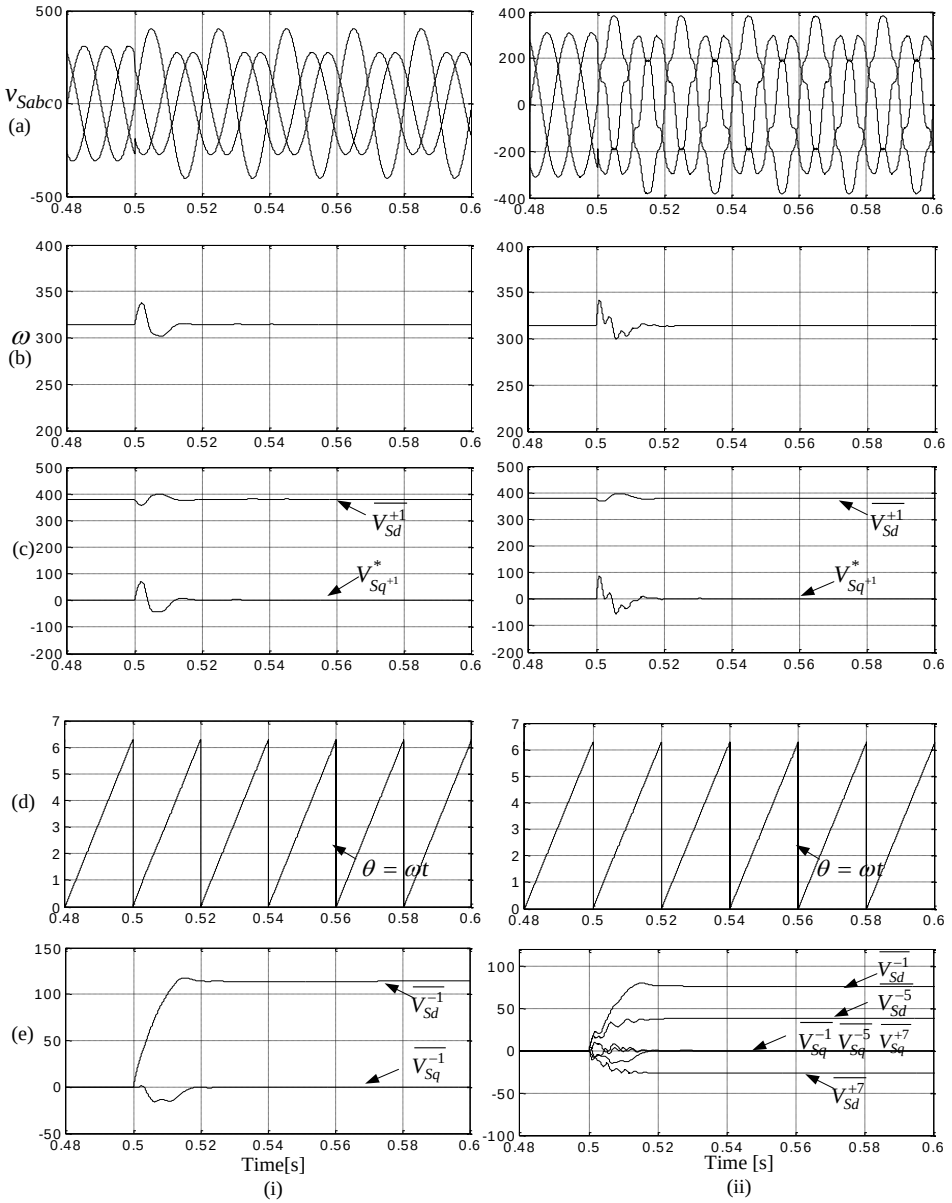


Fig.8. Response of the DMRF-PLL under (i) unbalanced (ii) unbalanced and distorted grid operating conditions: (a) grid voltage [V] ;(b) Estimated angular speed ω ;(c) detected voltage $\overline{V_{Sd}^{+1}}$ and $V_{Sq^{+1}}^*$;(d) detected phase angle θ [rad/s];(e) Detected positive- or negative sequence fundamental frequency and harmonic component [V];

It can be seen that the decoupled MRF structure is able to extract precisely not only positive- and negative-sequence components of the fundamental frequency voltage signals, but also the harmonic components. The extracted positive-sequence q-axis component $V^*_{Sq^{+1}}$ is passed through a PI controller to generate an estimation of the angular speed of the component. The speed estimation ω is integrated to give the angle θ which is used in the transformation matrices for multiple reference frames.

Compared the simulation results with DDSRF-PLL in [12], the proposed DMRF-PLL method has a very straightforward implementation, it can be easily extended to include other harmonic components in the decoupling feedback structure if these components are large enough to degrade the PLL's performance. Under the unbalanced grid operating condition shown in Fig.8 (a,i)-Fig.8 (e,i), DMRF-PLL has an identical performance like DDSRF-PLL, $\overline{V^{+1}_{Sd}} \equiv V^{+1}_{S}$, $\theta = \omega t$. Under the unbalanced and distorted grid operating condition shown in Fig.8.ii, estimated angular speed ω only had a short period of transient process, then quickly settled down to its nominal value of $314 rad/s$ shown in Fig.8(b,ii),no visible distortion in the phase angle θ shown in Fig.8(d,ii) is observed, which means $\theta = \omega t$, but there is some oscillation in $V^*_{Sq^{+1}}$, which caused $\theta \approx \omega t$ [12]. Moreover, the positive- or negative-sequence of fundamental frequency and harmonic component in *d*-axis and *q*-axis are extracted precisely as shown in Fig.8 (e,ii).

In all, the DMRF-PLL completely eliminates the problems of the conventional SRF-PLL and the DDSRF-PLL. The results presented above shows that the proposed DMRF-PLL is a very comfortable technique to the detection of fundamental-frequency positive-sequence component under unbalanced and distorted utility voltages condition, which is quite essential for the control of DVR system. In the next section, the control strategy of DVR system will be discussed in detail.

3 Control of the DVR

In order to design the control strategy of the DVR, the DVR model is built first, according to the schematic diagram of the DVR system in Fig.1, the load voltage is regulated by the DVR through the injection voltage u_{DVR}. Assume that the load has an inductance L_l and resistance r_l and the DVR harmonic filter has an inductance of L_f ,a resistance of r_f and a capacitance of C_f ,the DVR injection transformer has a combined winding resistance of r_t ,leakage inductance of L_t and turns ratio of $n:1$ .The following state-space equations can be obtained:

$$u_i = u_c + i_f r_f + L_f \frac{di_f}{dt} \tag{14}$$

$$i_f = i_c + n i_l \, , \, i_c = C_f \frac{di_c}{dt} \tag{15}$$

$$u_{DVR} = n(u_c - n(r_t i_l + L_t \frac{di_l}{dt})) \tag{16}$$

$$u_L = u_S + u_{DVR} \tag{17}$$

$$u_L = r_l i_l + L_l \frac{di_l}{dt} \tag{18}$$

Equation (14)-(18) form the basis of the DVR model which will be used for the controller design. The main considerations for the control system of a DVR include: load voltage reference generation, transient and steady-state control of the injected voltage, the stability and response of the system, the dc-link voltage of the VSI. In the following section, the discussion is focus on three points: (1) load voltage reference generation. (2) The analysis of feed-forward and feed-back controller. (3) the dc-link voltage control strategy.

3.1 Load voltage reference generation

To determine the desired load voltage reference, a phase-locked-loop is essential. In this paper, a new structure DMRF-PLL is used to create sinusoidal load voltage references for the d-q coordinate system of the controller, which has been discussed in section 2. This PLL can detect the amplitude and the phase of the positive-sequence component of the grid voltage very fast and accurately during voltage sag, unbalance and distorted condition.

Meanwhile, the desired response from DVR PLL system is quite different from other applications. If the PLL responses too fast to changes in the phase during a voltage sag, the post-sag phase may be used. Therefore, the DVR would not be able to compensate for this phase jump. Conventionally, once a sag is detected, the target phase of the voltage reference is fixed to the pre-sag phase, to ensure that if the reference is faithfully tracked, then the load voltage phase will remain unaffected [16].

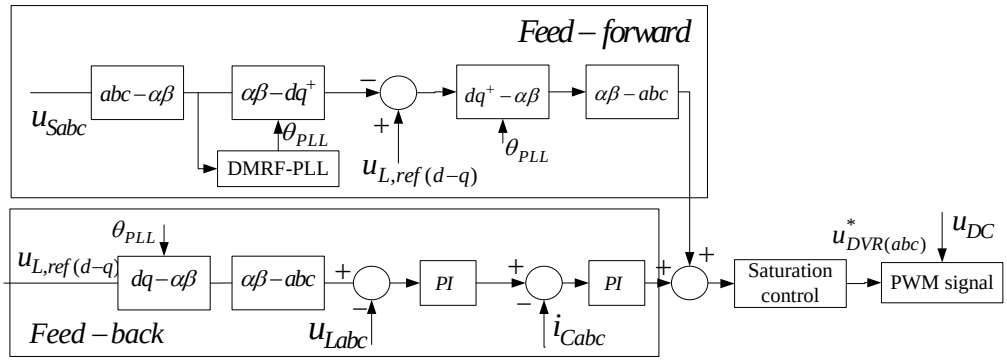


Fig.9. Control structure of the combined feed-forward/feed-back DVR

In this paper, the phase is not frozen to the pre-sag phase, but instead the PLL response is properly slowed. Once a sag event occurs, the phase will therefore very slowly shift from the pre-sag phase to the post-sag phase. This gives the benefit of improved series voltage injection utilization of in-phase compensation, but without any sudden jump in voltage phase as seen by the load side.

The load reference voltage in d-q frame is set as follows: $U_{Ld,ref} = 380V$, $U_{Lq,ref} = 0V$. Then the d-q coordinate variables are transformed to the a-b-c coordinates by the transformation $dq - \alpha\beta$, $\alpha\beta - abc$:

$$T_{dq^+/\alpha\beta} = \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix} \tag{19}$$

$$T_{\alpha\beta/abc} = \sqrt{2/3} \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \tag{20}$$

where θ is the angular frequency of the synchronous rotating reference frame synchronized with grid voltages by using DMRF-PLL.

3.2 Feed-forward/feed-back controller

The primary existing control structure of DVR system is based on feed-forward control that the voltage on the source side of the DVR is compared with a load-side reference voltage and the error is fed to the PWM pulse generator.

In this paper, the primary control structure shown in Fig.9 is based on a closed-loop controller with supply voltage feed-forward, load voltage and filter capacitor current feed-back. The feed-forward component provided the required transient response and uses the dc-link voltage to calculate the required modulation depth, but this doesn't account for the voltage droop the filter inductor and the transformer. Therefore, a closed loop load voltage feedback is added, but only such a feedback scheme is still inadequate because the level of damping deteriorates as the load power factor decreases [17]. Therefore, the filter capacitor current is fed back to achieve a sinusoidal capacitor while the outer voltage loop is used to regulate the load voltage.

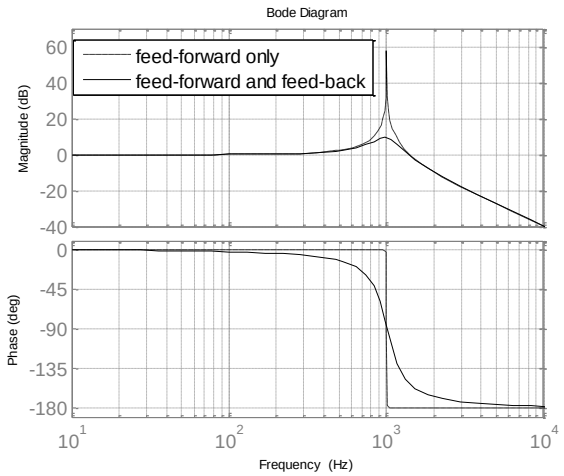


Fig.10 Comparison of frequency response between feed-forward only and feed-forward/feed-back controller

Fig.10 shows a comparison of frequency response between the feed-forward only and the combined feed-forward/feed-back controller proposed in this paper, which shows the bode-magnitude and bode-phase frequency diagram from the load reference voltage $u_{L,ref}$ to load voltage u_L .It can be observed that the feed-forward only controller has serious resonance problem introduced by the LC filter, this resonance is effectively attenuated by the feed-back provides some damping for the resonance in the LC switching ripple filter.

3.3 Control strategy of dc-link voltage

During a voltage sag, the DVR exchanges active and reactive power with the surrounding system. If active power is supplied to the load from the DVR, it needs a source for this energy. In this paper, the energy is delivered from the voltage source rectifier (VSR)

connected to supply side. During a voltage sag condition, the dc link voltage can maintain almost constant which can provide adequate energy for voltage compensation. The control scheme of dc-link voltage on VSR shown in Fig.11 is based on an unbalanced and distorted system, which is suit for most voltage distributions.

The control strategy consists of two parts: outer voltage loop and inner current loop, the outer loop forms the average rectifier bridge output power reference P_0 which is used to generate the current commands for the inner current loop, and the inner loop is used to regulate the positive- and negative sequence currents.

In order to regulate the dc-link voltage to be a desired level u_{DC}^* , a simply PI controller is implemented as the outer voltage loop, where the measured DC capacitor voltage u_{DC} is compared with the reference voltage u_{DC}^*, and the error signal is used to produce a reference DC current signal i_{DC}^* according to

$$i_{DC}^* = (k_{PV} + {k_{IV}}/{s}) \times (u_{DC}^* - u_{DC}) \quad (21)$$

The selection of k_{PV} and k_{IV} has been discussed in [18]. Then the required power P_0 is obtained by multiplying u_{DC}^* to the I_{DC}^*, i.e, $P_0 = U_{DC}^* I_{DC}^*$ .Then the current commands for the inner loop is generated as per (22),

$$\begin{bmatrix} I_d^{+1*} \\ I_q^{+1*} \\ I_d^{-1*} \\ I_q^{-1*} \end{bmatrix} = \frac{2P_0}{3D} \begin{bmatrix} \overline{V_{sd}^{+1}} \\ \overline{V_{sq}^{+1}} \\ \overline{V_{sd}^{-1}} \\ \overline{V_{sq}^{-1}} \end{bmatrix} \quad (22)$$

where $D = (\overline{V_{sd}^{+1}})^2 + (\overline{V_{sq}^{+1}})^2 - (\overline{V_{sd}^{-1}})^2 - (\overline{V_{sq}^{-1}})^2$.

The positive and negative sequences of supply voltage $\left\{\overline{V_{Sd}^{+1}}, \overline{V_{Sq}^{+1}}, \overline{V_{Sd}^{-1}}, \overline{V_{Sq}^{-1}}\right\}$ can be obtained by the DMRF-PLL. If regulating the current in dq^{+1} and dq^{-1} coordinate system directly, there needs four PI current controllers, the regulation of the PI parameter will become very complex. To reduce the number of the inner current loop, both the positive and negative current commands in dq^{+1} and dq^{-1} coordinate system are transformed to $\alpha\beta$ coordinate system,

$$\begin{bmatrix} I_\alpha^{+1*} \\ I_\beta^{+1*} \end{bmatrix} = T_{dq^+/\alpha\beta} \begin{bmatrix} I_d^{+1*} \\ I_q^{+1*} \end{bmatrix}, \quad \begin{bmatrix} I_\alpha^{-1*} \\ I_\beta^{-1*} \end{bmatrix} = T_{dq^-/\alpha\beta} \begin{bmatrix} I_d^{-1*} \\ I_q^{-1*} \end{bmatrix} \quad (23)$$

$$I_\alpha^* = I_\alpha^{+1*} + I_\alpha^{-1*}, I_\beta^* = I_\beta^{+1*} + I_\beta^{-1*} \quad (24)$$

The transform matrix $T_{dq^+/\alpha\beta}$ and $T_{dq^-/\alpha\beta}$ can be expressed as

$$T_{dq^+/\alpha\beta} = \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix} T_{dq^-/\alpha\beta} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \quad (25)$$

where θ is the angular frequency of the synchronous rotating reference frame synchronized with grid voltages by using DMRF-PLL. In order to realize zero steady state tracking error, a hybrid PI and resonant controllers are designed in the current loop, the transfer function of the current loop can be expressed as

$$H(s) = K_{pI} + \frac{K_{iI}}{s} + \sum_{i=3,5,7} \frac{K_i s}{s^2 + \omega_i^2}, \omega_i = 2\pi \times 50 \times i\, rad/s \quad (26)$$

The selection of parameters K_{pI} , K_{iI} , K_i has been discussed in [19]. This control strategy of dc-link voltage can both eliminate the dc-link voltage ripple and provide adequate active power for the voltage source inverter (VSI), the simulation results verify the correctness of the proposed method which will be shown in Section 4.

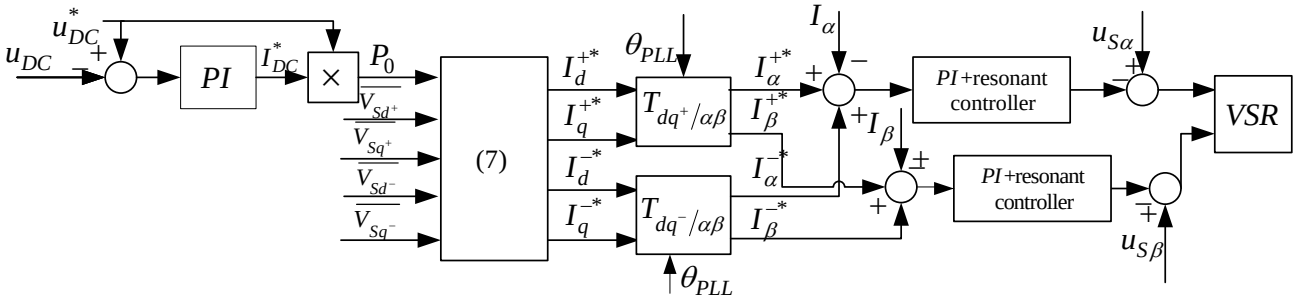


Fig.11. Control structure of DC-link voltage on VSR

4 Simulation results

A detailed simulation has been carried out using MATLAB/SIMULINK software to verify the efficacy of the proposed control algorithm on a DVR system. All the simulations are based on the 380V/50kVA power rating system which is shown in Fig.1 and the system parameter is shown in Table 1. The DVR consists of three single-phase full-bridge voltage-source inverters (VSIs), a six-leg voltage

source rectifier (VSR), three second-order low pass filters (LPF) and three single-phase matching transformers. The VSIs have 12-IGBT switches and a dc power supply in the common dc link, which is charged to 650V by VSR which is connected to the supply-side. The load of this simulated system is Y-connected 40*kW* linear resistive load.

Three types of voltage sags were generated by the power source as described in Table 2.Case 1 is a typical three-phase fault where all the phase voltages are symmetrically decreased to 50% from the rated value. Case 2 is a typical unbalanced fault where the a-phase voltage decreased to zero, the b-phase voltage and c-phase voltage decreased 20%, from the normal condition.Case3 is a unbalanced fault together with voltage distorted. The a-phase voltage increased 20%, the b-phase voltage and c-phase voltage decreased 20%, meanwhile 10% fifth order harmonic and 10% seventh order harmonic components are added to all the phases. The fault interval in the three cases is 100*ms* (five fundamental cycles) from 200*ms* to 300*ms.*

Table 1 Specifications and system parameters

Parameters	value
Distribution supply Voltage	380V
Compensation power	50kVA
transformer turns ratio	1:1
DC link capacitor	$10000\mu F$
DC link voltage	650V
Filter capacitance C_f	$55\mu F$
Filter inductance L_f	$462\mu H$

Table 2 Source side terminal voltage for the voltage sag fault in the simulation

Phase voltage	Normal condition	When voltage sags occurred		
		Case 1	Case 2	Case 3
v_{sa} [V]	$220\angle 0^\circ$	$110\angle 0^\circ$	0	$264\angle 0^\circ$ +22V 5th /22V 7th harmonic
v_{sb} [V]	$220\angle -120^\circ$	$110\angle -120^\circ$	$187\angle -120^\circ$	$187\angle -120^\circ$ +22V 5th /22V 7th harmonic
v_{sc} [V]	$220\angle 120^\circ$	$110\angle 120^\circ$	$187\angle 120^\circ$	$187\angle 120^\circ$ +22V 5th /22V 7th harmonic

4.1 voltage sag in case 1

The first simulation is carried out for a balanced voltage sag in case 1 and linear *RL* load (5 Ω+5mH). The supply voltage drops to 50% of its nominal value from 200 to 300 ms (five fundamental cycles) as shown in Fig. 11.a. The load voltages and DVR injected voltages are shown in Fig. 11.b and Fig.11.c. It can be seen that the DVR would inject the compensating voltage immediately after supply voltage sag is detected, to maintain load voltages at desired level. Meanwhile in views of the load voltage responses at the beginning of the sag and recovery from the sag, a smooth transient is shown with only very limited waveform distortions.

Also, it can be seen that there is the presence of very slight ripples during the sag recovery moment. This ripple can be attributed to the DVR *LC* filter. Similar phenomena can also be seen at the recovery tail of DVR injection voltages, as shown in Fig. 11.c.The DC-link voltage shown in Fig.11.d can maintain at its desired level 650V during the voltage sag, at the beginning of the sag and recovery from the sag, the overshoots of the voltage are -0.7V and 0.5V respectively, the response time is about half cycle.

4.2 voltage sag in case 2

The second simulation is carried out for unbalanced voltage sag in case 2 and linear *RL* load (5 Ω+5mH). The phase *a* voltage of drops to 0, meanwhile phase *b* and phase *c* voltage drop to 85% of their normal values from 200 to 300ms as shown in Fig. 12a. The load voltages and DVR injected voltages are shown in Fig. 12b and Fig.12c.

Once again, the transient is smooth with only negligible. The DC-link voltage shown in Fig.12.d also can maintain at its desired level 650V during the voltage sag, at the beginning of the sag and recovery from the sag, the overshoots of the voltage are -0.5V and 0.8V respectively.

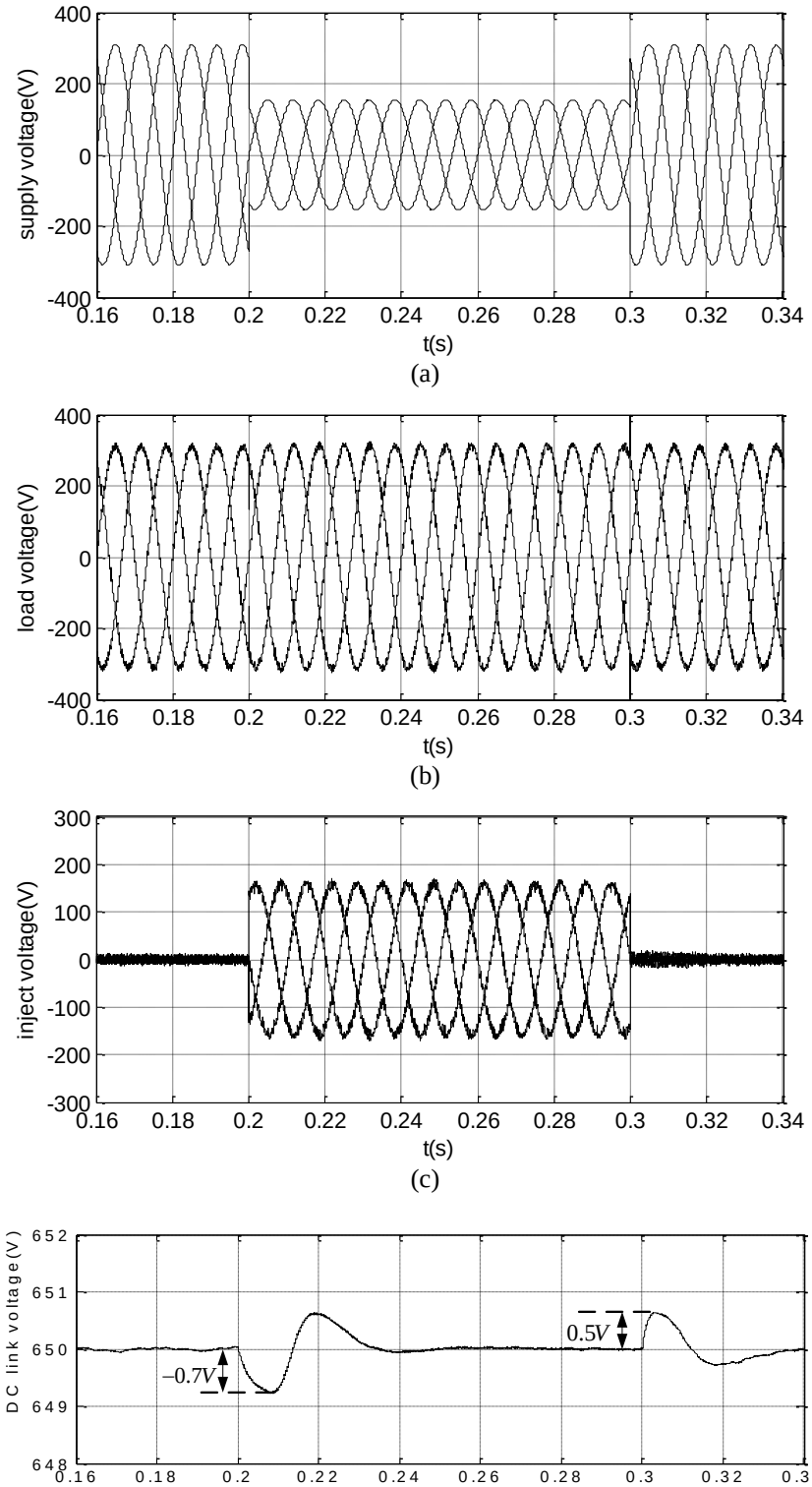
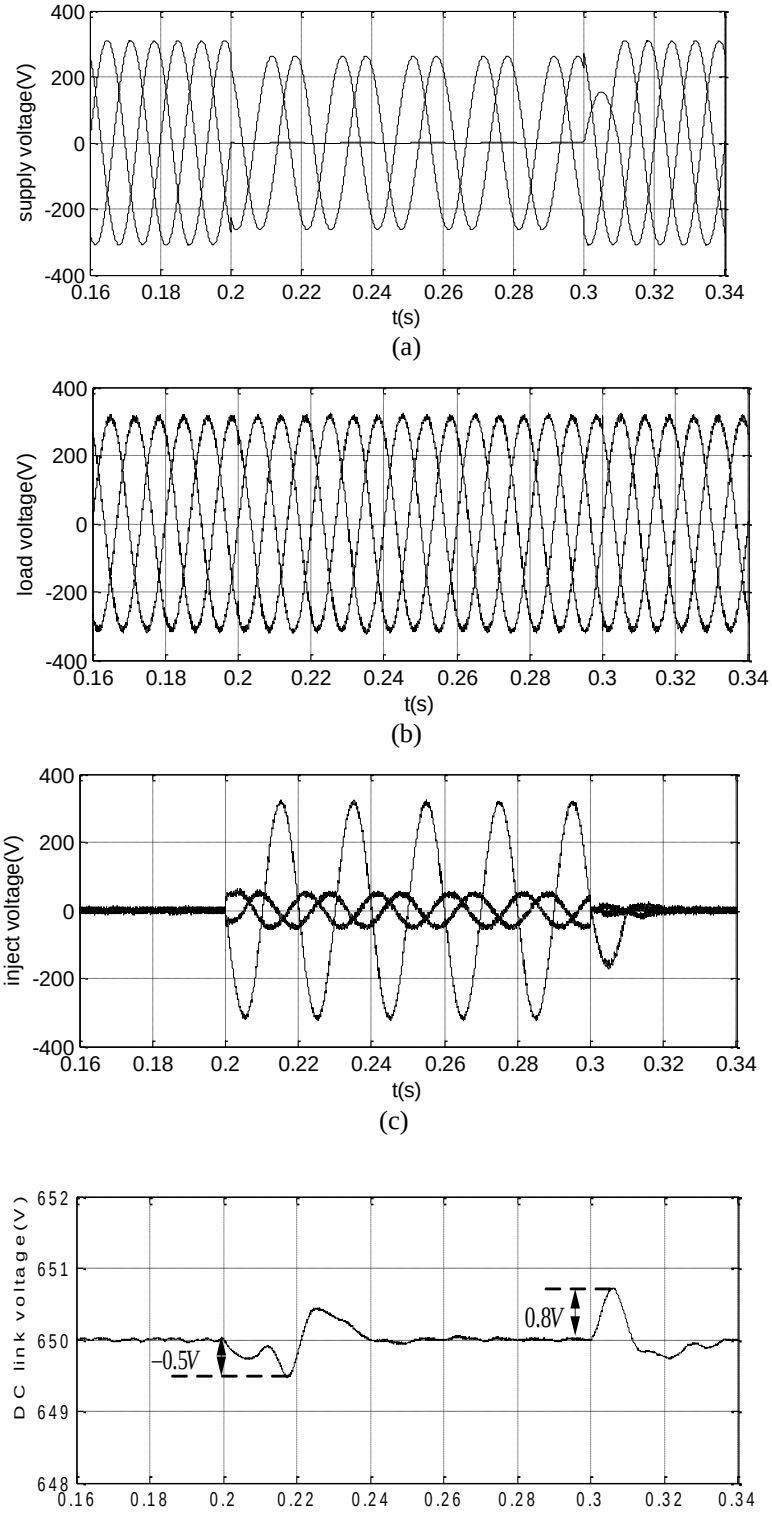


Fig.11. Simulated voltage sag fault compensation performance in Case 1:
a) Supply voltage (b) Load voltage (c) Inject voltage by DVR (d) DC-link voltage

4.3 voltage sag in case 3

The third simulation is carried out for distorted and unbalanced voltage sag in case 3. The phase *a* voltage increased 20%, the phase *b* voltage and phase *c* voltage decreased 20%, and meanwhile 10% fifth order harmonic and 10% seventh order harmonic components are added to all the phases as shown in Fig.13.a. The load voltages and DVR

injected voltages are shown in Fig. 13b and Fig.13c. the DVR can not only compensate the positive and negative-sequence component of fundamental frequency, but also the harmonic component, which means that the DVR system provides voltage harmonic compensation capability, the transient is also smooth regardless of the presence of harmonic. At the beginning and recovery from the sag, the overshoot of the dc-link voltage are 0.4V and -0.3V.



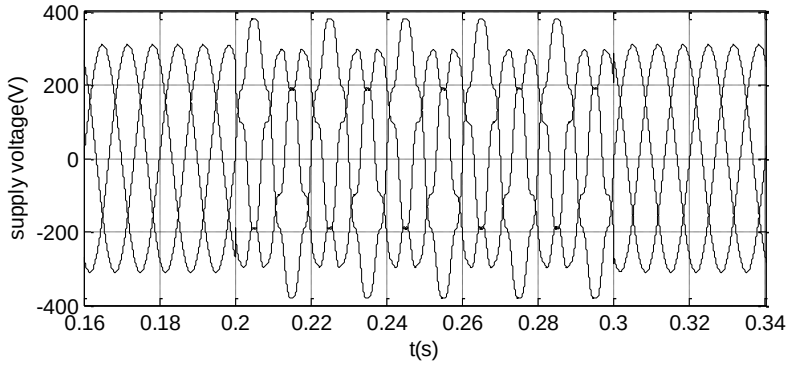
(a)

(b)

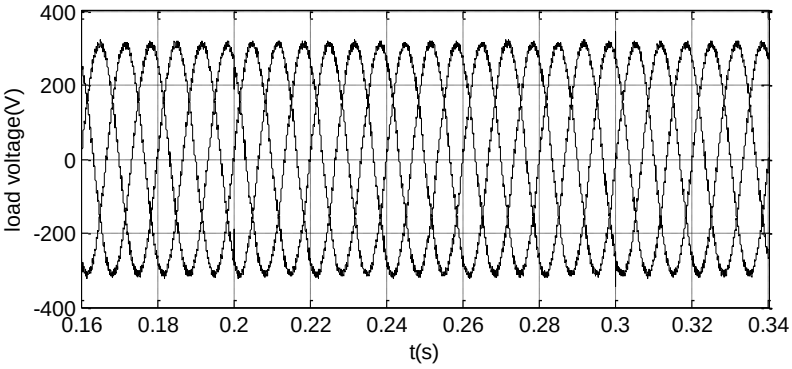
(c)

(d)

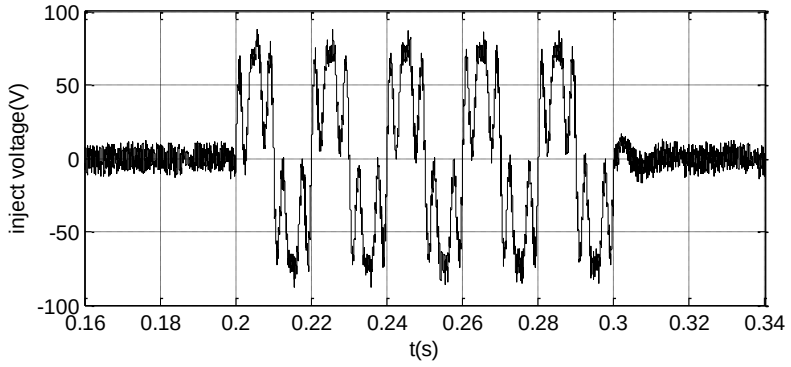
Fig.12. Simulated voltage sag fault compensation performance in Case 2:
(a) Supply voltage (b) Load voltage (c) Inject voltage by DVR (d) DC-link voltage



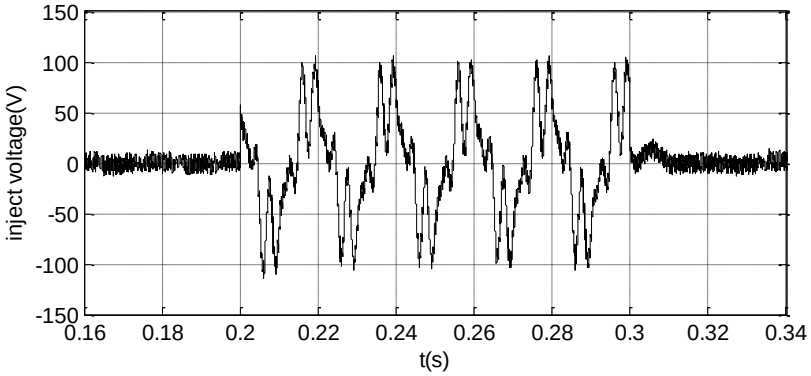
(a)



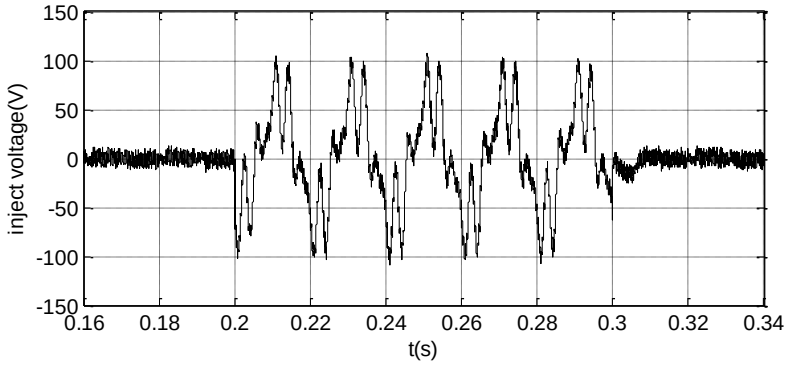
(b)



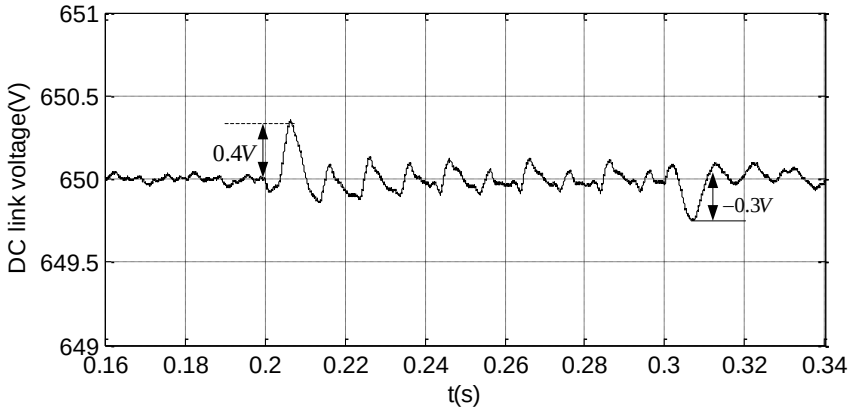
(c- Phase A)



(c- Phase B)



(c- Phase C)



(d)

Fig.13. Simulated voltage sag fault compensation performance in Case 3:
(a) Supply voltage (b) Load voltage (c) Inject voltage by DVR (d) DC-link voltage

The performance in the three typical cases shown in Figs.11-13 verifies the validity and effectiveness of the proposed algorithm. In all the three cases, the load terminal voltages appeared completely symmetrical without transient problem. The DSRF-PLL guarantees the accurate detection of the amplitude and the phase of the positive-sequence component of the grid voltage under grid voltage sag, unbalanced and distorted conditions; meanwhile, the PLL response is properly slowed. Once the sag event occurs, the phase slowly shifts from the pre-sag phase to the post-sag phase. This gives the benefit of improved series voltage injection utilization of in-phase compensation, but without any sudden jump in voltage phase as seen by the load. The dc-link voltage can remain the rated voltage 650V during the voltage distribution in the three cases.

5 Conclusion

Dynamic voltage restorer has been recognized as the most promising solution to protect the sensitive loads from voltage sags. This paper proposes a novel scheme for controlling of DVR by using double reference frame phase-locked-loop (DRF-PLL). Detailed analysis and simulation results presented in this paper showed that DMRF-PLL is a suitable solution to the detection of fundamental positive-sequence component of unbalanced and/or distorted grid voltages. Moreover, the corresponding control strategy of the DVR based on the hybrid PI and resonant controllers is presented. The validity and effectiveness of a combined feed-back and feed-forward control scheme has been verified by the extensive simulation of 380V/50kVA prototype system, and excellent transient and steady state performance has been achieved. The proposed phase-locked-loop (PLL) technique can also find wide applications in grid-tie power converters, especially in the area of power quality conditioners, such as dynamic voltage restorers and active filters.

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