

An Effective Joint Implementation Design of Channel Equalizer and DDC for WDAR Receiver

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Abstract: - In this paper, the technique of digital down conversion (DDC) and channel equalization in wideband digital array radar (WDAR) are introduced. The analysis about the frequency domain equalization algorithm based on weighted least squares (WLS) is derived in detail at first. Then, an efficient DDC based on polyphase structure with intermediate frequency (IF) bandpass sampling is presented. Moreover, a simple structure which combines equalizer and DDC is proposed, which is proven to be valid, feasible and efficient. A design example is given and the FPGA resource consumption saving is discussed also. The corresponding simulations and test results demonstrate the effectiveness of the proposed DDC and show that the performance of the channel mismatch after equalization is improved obviously.

Key-Words: - wideband digital array radar (WDAR), channel equalization, bandpass sampling, digital down conversion (DDC), polyphase structure

1 Introduction

Digital array radar (DAR), a kind of fully digitized array antenna radar, applies for the digital technique in both of transmitting and receiving. It can realize beam forming and beam steering control via using amplitude-phase weighting and digital delay in baseband. Therefore, it makes the implementation easy for low side lobe, multi-beam and multi-target processing, adaptive anti-jamming, wideband and wide-angle scanning. The DAR that uses wideband waveforms is called wideband DAR(WDAR). Compared with conventional radar, there are many advantages for WDAR, such as high dynamic range (DR), high resolution, multifunction, rapid multi-beam steering, low side lobe, multi-target tracking, anti-jamming, adaptive processing, target identification and discrimination [1-3]. Hence, the development of WDAR is of great importance.

Superheterodyne receiver technique is widely used in communication and radar receivers. With the development of the effective analogue-to-digital converters (ADC), the application specific integrated circuit (ASIC) devices, digital signal processing (DSP) technique, digital receiver has gradually become popular in recent years. The digital receiver, which performs the digital conversion process close to the antenna and carries

out various functions by changing the software on a universal hardware platform, is a typical application of software radio in radar receiver. The received wideband signal with high frequency is hard to be processed directly. Nowadays, DDC, DSP and intermediate frequency (IF) digital technique, which can decrease the difficulty of sampling, place a dominant role in receiver systems [2,3]. As a key to digital receivers, DDC technique has more and more wide application in radar systems.

Most tasks of the WDAR receiver are completed in digital signal processors after sampling and DDC. Therefore, it must ensure that the amplitude and phase of the digital baseband signals processed via ADC and DDC identical with each other. This requires distortionless array channels for the whole signal bandwidth and identical frequency responses for all channels. However, the differences between the analog circuits in each channel will cause inconsistent amplitude and phase responses of receiver and transmitter channels in WDAR. The difference among the frequency responses of the channels are called channel mismatch. The channel mismatch will seriously affect the DBF performance of WDAR [4-8].

This paper is organized as follows. In section 2 the frequency-domain equalization algorithm based on weighted least squares is analyzed in detail.

Section 3 presents several different structures of DDC and shows a design example. By considering this example, a simple structure which combines equalizer and DDC is proposed in section 4. The corresponding simulation and test results are shown in section 5. Finally, section 6 concludes the paper.

2 Equalization Theory and Algorithm

The equalizer, a digital filter, is inserted behind each receiver channel to reduce channel mismatch. The processing structure is shown in Fig.1.

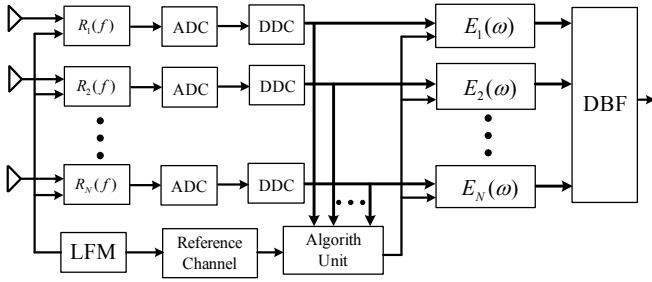


Fig.1 The equalization structure

If the frequency response of each receiver channel and that of each equalizer are denoted by $R_i(\omega)$ and $E_i(\omega)$, respectively, the equalized channel frequency response $H_i(\omega)$ equals to their product

$$H_i(\omega) = R_i(\omega) \cdot E_i(\omega) \quad (1)$$

$$i = 1, 2, \dots, N$$

where N is the number of channels.

The result of the equalization is that all $H_i(\omega)$ are identical with each other and equal to the frequency response of a reference channel. This can be written as

$$H_1(\omega) = H_2(\omega) = \dots = H_N(\omega) = H_{ref}(\omega) \quad (2)$$

So the frequency response of each equalizer can be expressed as follow

$$E_i(\omega) = H_{ref}(\omega) / R_i(\omega) \quad (3)$$

$$i = 1, 2, \dots, N$$

A linear frequency modulation (LFM) signal is fed into every mismatched channel under the radar calibration mode. The reference channel could be an

ideal channel or one of the receiver channels. In this paper, we consider the ideal channel.

Define the outputs of receiver channels as $R_1(m), \dots, R_N(m)$ which are the discrete values of $R_1(\omega), \dots, R_N(\omega)$.

$H_{ref}(\omega)$ is the frequency response of the ideal channel and usually is given as

$$H_{ref}(\omega) = e^{-j\omega(L-1)\tau/2} \quad (4)$$

where L is the order of equalizer and τ is the unit time delay of equalizer. Its corresponding discrete value is $H_{ref}(m)$.

So the discrete value of $E_i(\omega)$ should be

$$E_i(m) = H_{ref}(m) / R_i(m) \quad (5)$$

$$i = 1, 2, \dots, N$$

In order to compensate the channel mismatch, it is common to insert an adaptive Finite Impulse Response (FIR) filter as an equalizer to a mismatched channel [9-12,15]. At this time, the equalizer is a FIR filter of L order. As a matter of fact, the main issue becomes that how to determine coefficients adaptively for an FIR equalizer.

The FIR equalizer frequency response is

$$F_i(\omega) = \sum_{l=0}^{L-1} h_i(l) e^{-j\omega l \tau} = \mathbf{a}^T(\omega) \mathbf{h}_i \quad (6)$$

$$\mathbf{a}(\omega) = [1, e^{-j\omega \tau}, \dots, e^{-j\omega(N-1)\tau}]^T \quad (7)$$

$$\mathbf{h}_i = [h_i(0), h_i(1), \dots, h_i(L-1)]^T \quad (8)$$

where τ is the unit time delay of equalizer and T denotes transpose of a matrix.

Usually, the Weighted Least Square Fitting (WLSF) method is applied for approximating $F_i(\omega)$ to $E_i(\omega)$. The optimum coefficient vector \mathbf{h}_i should satisfy

$$\min_{\mathbf{h}_i} \sum_{m=0}^{M-1} |W(m) \cdot (E_i(m) - \mathbf{a}^T(m) \mathbf{h}_i)|^2 \quad (9)$$

$$= \min_{\mathbf{h}_i} \left(\left\| W \cdot (E_i - \mathbf{A} \mathbf{h}_i) \right\|^2 \right)$$

$$W = \text{diag}(W(0), W(1), \dots, W(M-1)) \quad (10)$$

$$E_i = [E_i(0), E_i(1), \dots, E_i(M-1)] \quad (11)$$

$i = 1, 2, \dots, N$

$$\mathbf{a}(m) = \left[1, \exp\left(-j\frac{2\pi m}{M}\right), \dots, \exp\left(-j\frac{2\pi m(L-1)}{M}\right) \right]^T \quad (12)$$

$m = 0, 1, \dots, M-1$

$$\mathbf{A} = \begin{bmatrix} 1 & 1 & \dots & 1 \\ 1 & \exp\left[-j\frac{2\pi}{M}\right] & \dots & \exp\left[-j\frac{2\pi(L-1)}{M}\right] \\ \vdots & \dots & \dots & \vdots \\ 1 & \exp\left[-j\frac{2\pi(M-1)}{M}\right] & \dots & \exp\left[-j\frac{2\pi(M-1)(L-1)}{M}\right] \end{bmatrix} \quad (13)$$

$$= \begin{bmatrix} \mathbf{a}^T(0) \\ \mathbf{a}^T(1) \\ \vdots \\ \mathbf{a}^T(M-1) \end{bmatrix}$$

where W is a weighting matrix which is related to the required fitting accuracy for different frequency. $W(i)$ is a window function which could be, for example, Hanning window, Triangle window, Hamming window and cosine window, and so on. These window functions improves the fitting accuracy in center of passband [9].

Matrix \mathbf{A} is a full rank matrix since it is composed of L linearly uncorrelated row vectors. The least square solution problem in equation (9) can be obtained by quadrature decomposition method [10-12]. Thus, h_i can be obtained by equation (14) or (15).

$$1) \quad h_i = R^{-1} \cdot d \quad (14)$$

where $R = A^H \cdot W^* \cdot W \cdot A$, $d = A^H \cdot W^* \cdot W \cdot E_i$, “ $*$ ” represents complex conjugate, “ H ” represents complex conjugate transposition.

$$2) \quad h_i = (W \cdot A)^+ (W \cdot E_i) \quad (15)$$

where “ $+$ ” represents Pseudo-inverse transformation.

3 DDC for WDAR

Thanks to the development of high performance ADC, ASIC devices and DSP technique, digital receiver has gradually become popular in recent years. However, the frequency of the signal received by the antennas is usually larger than 1GHz and is thereby difficult to process directly. Hence, IF digitalization including bandpass sampling and DDC is often used as a tradeoff.

3.1 Typical IF DDC Structure

A typical DDC structure is shown in fig.2. For narrow band signal, it usually has a relatively low sample rate and can be implemented with typical DDC structure directly. However, for wide band signal, it often requires a higher sample rate. It results in the problem that the digital mixers and filters should work with high data rate. Whereas, due to the limitation of current hardware, the method shown in fig.2 is difficult to work effectively for wideband signal in real time, that is, it is hard to realize wideband DDC with current ASIC devices. In fact, the speed and number of multipliers in mixers and filters are very important for determining the speed and resource consumption of ASIC devices.

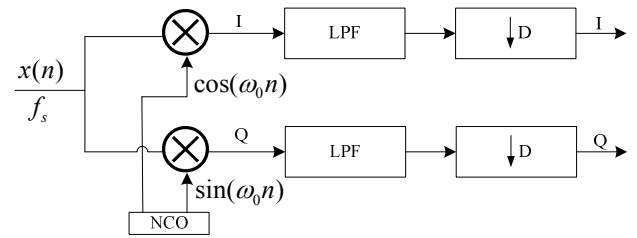


Fig.2 Typical DDC structure

3.2 DDC Based on Postpositional Mixer Structure

We can express the Numerically Controlled Oscillator (NCO) in complex form, then the typical DDC structure can be depicted as the structure in Fig.3.

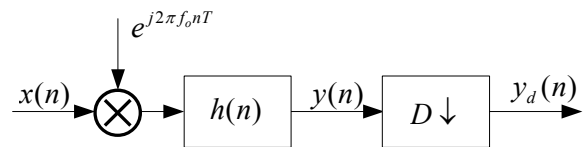


Fig.3 DDC in Complex form

$$y(n) = \sum_{m=0}^{N-1} h(m)x(n-m)e^{j2\pi f_o(n-m)} \quad (16)$$

$$= e^{j2\pi f_o nT} \sum_{m=0}^{N-1} h(m)e^{-j2\pi f_o mT} x(n-m)$$

where f_o is the NCO frequency , and N is the filter order.

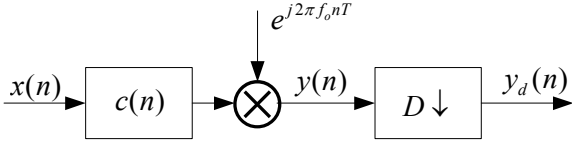


Fig.4 Exchange mixer and filter

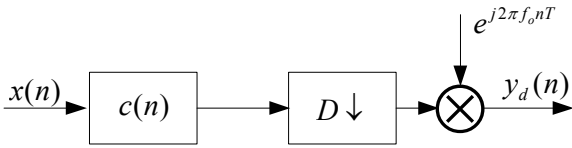


Fig.5 Postpositional mixer structure

Let $h(n)e^{-j2\pi f_o nT} = c(n)$, then the $c(n)$ can be regard as a new filter . According to the above equation, the mixer can be exchanged with the filter as it is shown in Fig.4. The output $y_d(n)$ is obtained by decimating $y(n)$, which means to discard some data in $y(n)$. If these data are discarded before mixing, the mixer and the decimator can be exchanged too. Then we get the postpositional mixer structure as it is shown in Fig.5. It is equal the structure in Fig.3. The output is

$$y_d(n) = y(nD)$$

$$= e^{j2\pi f_o nDT} \sum_{m=0}^{N-1} h(m)e^{-j2\pi f_o mT} x(nD-m) \quad (17)$$

The rate of input signal $x(n)$ is the sampling frequency f_s , but the rate of output signal $y_d(n)$ is f_s/D . Therefore, the multiplication rate in mixer decreases from f_s to f_s/D [13].

3.3 DDC Based on Polyphase Structure

The multi-rate signal processing provides us with a new method to implement DDC efficiently. According to the polyphase decomposition and the cascade equivalence shown in fig.6, a new wideband DDC structure is depicted in fig.7(a) , where h_1, h_2, \dots, h_M and W_1, W_2, \dots, W_M are obtained

from the prototype filter and the original mixer coefficients by polyphase decomposition, respectively .

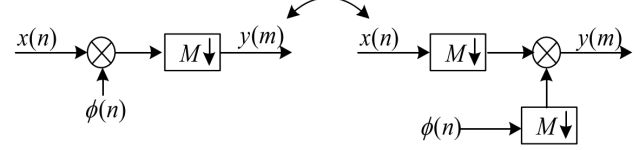


Fig.6 Cascade equivalence

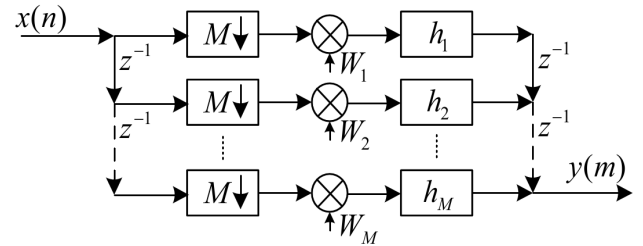


Fig.7(a) DDC 1 based on polyphase structure

The use of famous polyphase decomposition structure can decrease the rate of filter in DDC. If we substitute polyphase decomposition structure for polyphase decomposition structure, each branch of polyphase filter works at f_s/D and their total order is also N .

To improve the Signal-to-Noise Ratio (SNR) of output baseband signal, in fact, the filter order is pretty high. This is likely to result in large numbers of multiplier consumption in ASIC chip. In postpositional mixer structure, the $c(n)$ is complex and should be divided into real part and image part. In typical DDC structure, the filters of I channel are the same as that of Q channel. If we shared the filters, the resource consumption of realizing the filters especially the multiplier consumption could be reduced by half.

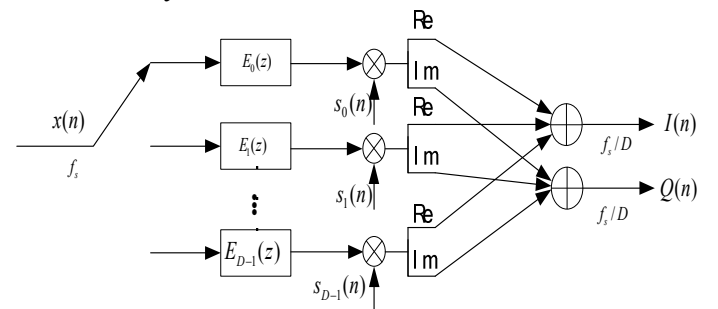


Fig.7(b) DDC 2 based on polyphase structure

The complex NCO data can be expressed as

$$e^{j2\pi f_o nT} = e^{j2\pi n f_o / f_s} = e^{j2\pi n m / M} \quad (18)$$

where m and M are two integers and their common divisor are eliminated, so the period of NCO data is M . As it is shown in Fig.7(b) NCO data $s_0(n), s_1(n), \dots, s_{D-1}(n)$, are distributed to D branches periodically. NCO data $s_i(n)$ of each branch is a constant if M is equal to D . So the mixers in Fig.7(a) could be placed after the polyphase filters. In addition, the filter bank in I channel and Q channel can be shared. As we can see from the Fig.7(b), the DDC structure is efficient but the following condition must be satisfied

$$\begin{cases} \frac{f_o}{f_s} = \frac{m}{M}, & m = 1 \dots M-1 \\ \frac{f_s}{M} = \frac{f_s}{D} = f_{out} \end{cases} \quad (19)$$

3.4 A DDC Example

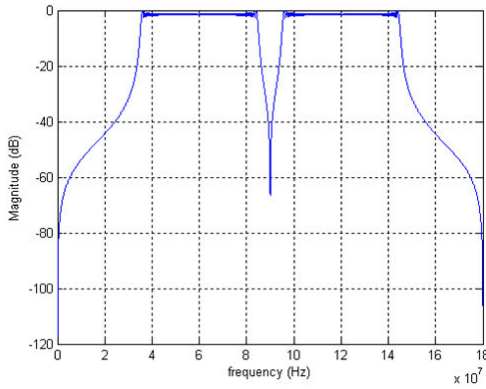


Fig.8 LFM frequency spectrum after sampling

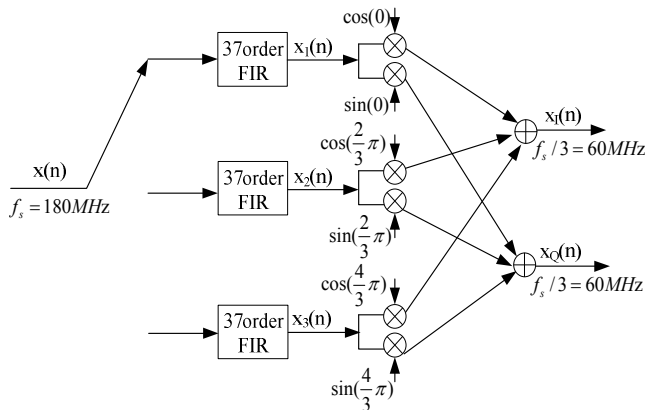


Fig.9 A wideband DDC design

On the basis of the analysis and deduction above, we carry out a wideband DDC design with the DDC structure 2 based on polyphase structure. Suppose

that the input is linear frequency modulation (LFM) signals, the center frequency of the intermediate frequency (IF) signal is $f_0 = 120MHz$, the signal bandwidth is $B = 50MHz$ and the width of linear frequency modulation (LFM) rectangle pulse signal is $T = 40us$.

The frequency spectrum of intermediate frequency signal after sampling is shown in Fig.8.

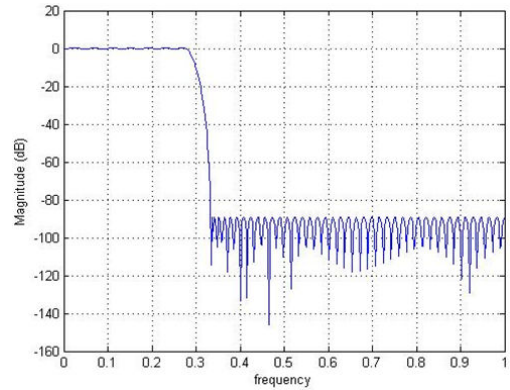


Fig.10 Frequency spectrum of filter

When using intermediate frequency bandpass sampling, we must follow this principle:

$$\begin{cases} \frac{2f_H}{n} \leq f_s \leq \frac{2f_L}{n-1} \\ 2 \leq n \leq \frac{f_H}{f_H - f_L} \end{cases} \quad (20)$$

where $f_H = f_0 + B/2 = 145MHz$ and $f_L = f_0 - B/2 = 95MHz$, so $n = 2$ and $145MHz \leq f_s \leq 190MHz$.

Because the spectrum of LFM signal is symmetrical, the output rate must be higher than $50MHz$ according to the Nyquist sampling theory. It is determined that the sampling frequency is $f_s = 180MHz$, $M=D=3$, so the output rate is $60MHz$. According to equation (19), it can be deduced that

$$\frac{f_o}{f_s} = \frac{m}{M} = \frac{60}{180} = \frac{1}{3} \quad (21)$$

Since the NCO data in Fig.7(b) are complex, it should be realized by real part and image part respectively. When $M=3$, the real parts of NCO data are $\cos(2\pi nm/M) = \cos(2\pi n/3)$. They are periodic and the fundament data are $1, -1/2, -1/2$.

Similarly the image parts of NCO data are $\sin(2\pi nm/M) = \sin(2\pi n/3)$. They are periodic and the fundamnt data are $0, \sqrt{3}/2, -\sqrt{3}/2$.

The block diagram of this example is shown in Fig.9. All multipliers work at 180MHz. The filter total order is 111, so the filter can be divided into 37 order filter. The spectrum of filter after sampling is shown in Fig.10.

For this filter, the parameters would be
 passband : $\geq \frac{B/2}{f_s} \times 2\pi = \frac{25}{180} \times 2\pi = \frac{5}{18} \pi$;
 stopband : $\leq \frac{(f_s/3)/2}{f_s} \times 2\pi = \frac{30}{180} \times 2\pi = \frac{1}{3} \pi$;
 passband ripple : 0.5dB ;
 stopband attenuation : 90dB

The output can be depicted as follow.

$$\begin{aligned} x_I(n) &= x_1(n) \cdot \cos(0) + x_2(n) \cdot \cos\left(\frac{2}{3}\pi\right) + x_3(n) \cdot \cos\left(\frac{4}{3}\pi\right) \\ &= x_1(n) + x_2(n) \cdot \left(-\frac{1}{2}\right) + x_3(n) \cdot \left(-\frac{1}{2}\right) \\ &= x_1(n) - \frac{1}{2}[x_2(n) + x_3(n)] \end{aligned} \quad (22)$$

$$\begin{aligned} x_Q(n) &= x_1(n) \cdot \sin(0) + x_2(n) \cdot \sin\left(\frac{2}{3}\pi\right) + x_3(n) \cdot \sin\left(\frac{4}{3}\pi\right) \\ &= x_1(n) \cdot 0 + x_2(n) \cdot \left(\frac{\sqrt{3}}{2}\right) + x_3(n) \cdot \left(-\frac{\sqrt{3}}{2}\right) \\ &= \frac{\sqrt{3}}{2}[x_2(n) - x_3(n)] \end{aligned} \quad (23)$$

where “*” denote convolution.

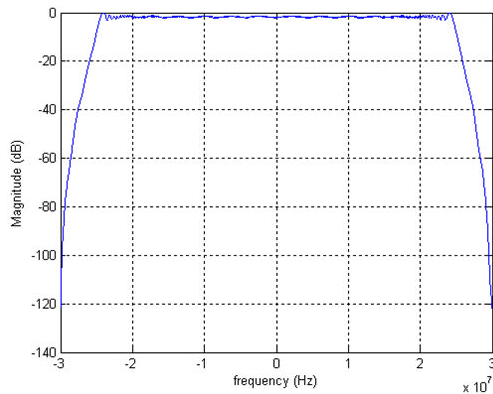


Fig.11 Frequency spectrum of baseband

The in-phase and in quadrature baseband signal are obtained after sampling and proposed DDC. The frequency spectrum of baseband signal is shown in Fig.11. The output rate is 60MHz, and the baseband signal bandwidth is 50MHz.

As shown in Fig.11, frequency spectrum of baseband signal without aliasing distortion is relatively flat in its passband. According to the simulation result, the DDC structure based on polyphase filter is proved correct.

Building a wideband digital down converter in FPGA, the working speed and the number of multipliers are most important because they will determine the wideband digital receiver's speed and resource consumption. The basic principle for high-speed and real-time signal processing is to reduce the cost and make full use of the hardware resources by algorithm and software optimization.

With the development of FPGA chip, the number and speed of multipliers upgrade quickly. Based on the speed priority principle we can easily find a FPGA chip out to realize the proposed DDC structure in Fig.8. The multipliers work at 180MHz. The product of 1/2 and $[x_2(n) - x_3(n)]$ can easily obtained by bit shift technique, so can 1/2 and $[x_2(n) + x_3(n)]$. So the total using number of multipliers is 38, therein 37 time division multiplexed multipliers used to carry out polyphase filter and one multiplier used to carry out multiplying $\sqrt{3}$ and $[x_2(n) - x_3(n)]$.

The DDC structure based on polyphase filter proposed in this paper adopts an appropriate multiplication rate and save a lot of hardware resources especially in multiplier consumption.

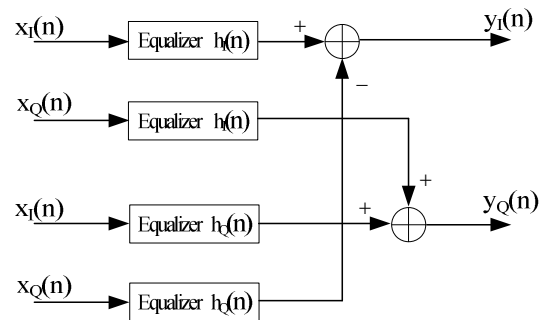


Fig.12 The equalization process in baseband

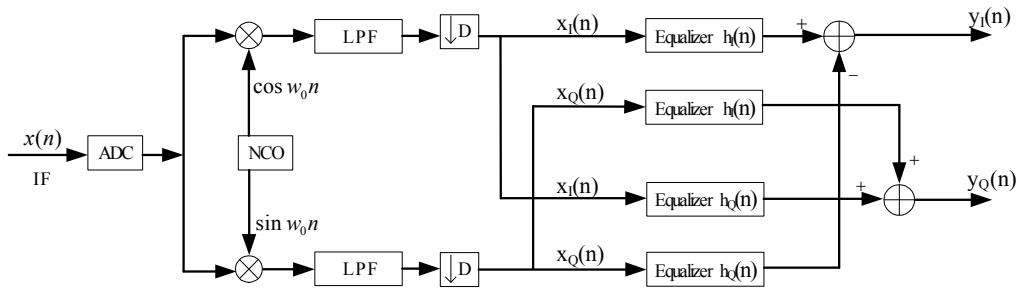


Fig.13 Equalizer behind typical DDC

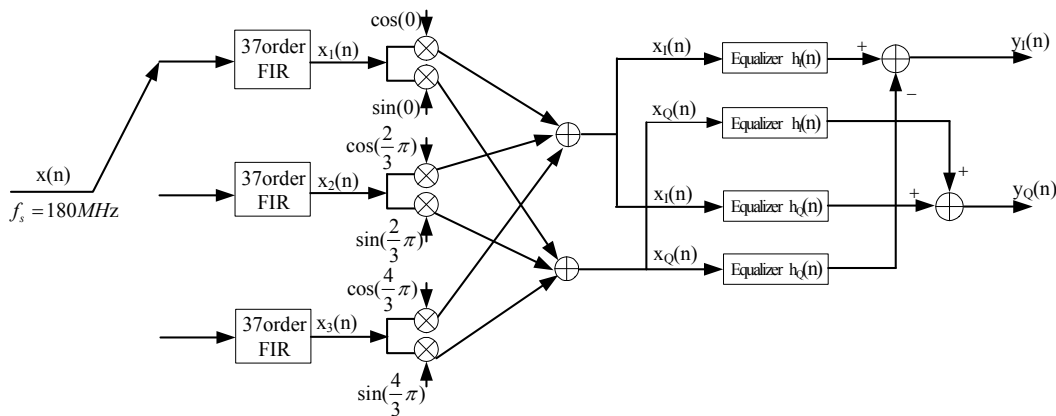


Fig.14 Equalizer behind DDC based on polyphase structure

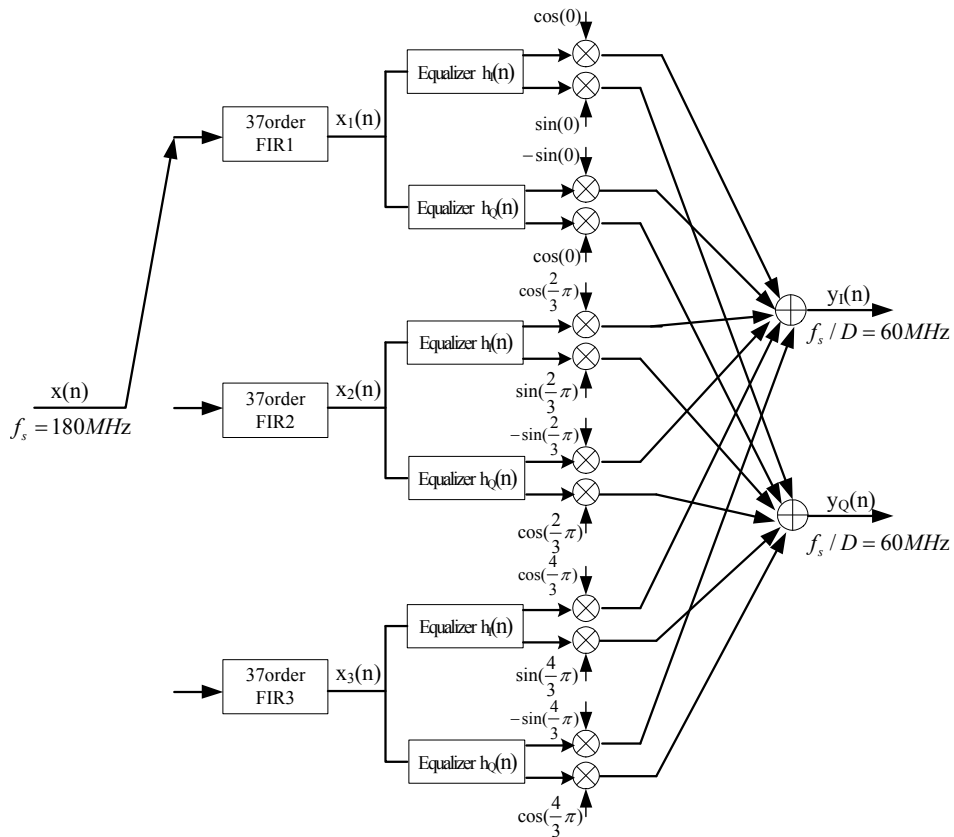


Fig.15 Equalizer embedded in DDC based on ployphase structure

4 Joint Implementation Design of DDC and Channel Equalizer

Most tasks of WDAR receiver are implemented in digital signal processors after sampling and DDC. Therefore, amplitude and phase of the digital baseband signals processed via ADC and digital down converters should be identical with each other.

In many application situations, we always suffer from the problems of the amplitude and phase error among different channels [9-12,14]. The frequency dependent interchannel mismatch may severely make the wideband digital arrays performance degrades. It is a hard nut to crack with analog devices. But now it can be easily resolved through the use of digital devices. In order to compensate the mismatch, we usually insert an adaptive FIR filter as an equalizer to a mismatch channel [15].

Suppose that the digital baseband signal after DDC and filter is $x_I(n) + jx_Q(n)$, the equalization filter is $h(n) = h_I(n) + jh_Q(n)$, and the order of the equalization filter is L . So the digital baseband signal after the equalization filter can be expressed as

$$y(n) = (x_I(n) + jx_Q(n)) * (h_I(n) + jh_Q(n)) \quad (24)$$

It can be expanded into

$$\begin{aligned} y(n) &= (x_I(n) * h_I(n) - x_Q(n) * h_Q(n)) \\ &\quad + j(x_I(n) * h_Q(n) + x_Q(n) * h_I(n)) \end{aligned} \quad (25)$$

Then the output orthogonal signals can be expressed as

$$\begin{aligned} y_I(n) &= x_I(n) * h_I(n) - x_Q(n) * h_Q(n) \\ y_Q(n) &= x_Q(n) * h_I(n) + x_I(n) * h_Q(n) \end{aligned} \quad (26)$$

On the basis of the analysis and deduction above, the equalization process in baseband can be depicted as in Fig.12. If the order of the FIR equalization filter is L , $4L$ multipliers are needed to fulfil the equalization process in all.

4.1 Equalizer behind Typical DDC

The block diagram of equalizer behind typical DDC is shown in Fig.13.

As it is shown in Fig.13, the foreside is a typical DDC and the following part is a equalizer. We can draw a conclusion that the consumption of multiplier is a huge challenge to FPGA resource.

4.2 Equalizer behind DDC Based on Polyphase Structure

From the analysis and deduction in subsection 3.4 of this paper, we can conclude that DDC based on polyphase structure is high efficient due to the reduction of multiplier consumption. The block diagram of equalizer behind DDC based on polyphase structure is shown in Fig.14.

As we can see from Fig.14, the foreside is DDC based on polyphase structure and the following part is equalizer. Although it can save a lot of multiplier consumption in the foreside, the multiplier consumption in the equalization process is still a huge challenge to FPGA resource.

4.3 Equalizer Embedded in DDC Based on Polyphase Structure

To save the multiplier consumption, we put forward a new structure which combines DDC and equalizer. The method to realize equalizer embedded in DDC based on polyphase structure shown in Fig.15.

As it is shown in Fig.15, the multiplier consumption of realizing the equalization process reduces by half.

According to equation (22) and (26), the output $y_I(n)$ can be depicted as

$$\begin{aligned} y_I(n) &= x_1(n) \cdot \cos(0) * h_I(n) + x_2(n) \cdot \cos\left(\frac{2}{3}\pi\right) * h_I(n) \\ &\quad + x_3(n) \cdot \cos\left(\frac{4}{3}\pi\right) * h_I(n) - x_1(n) \cdot \sin(0) * h_Q(n) \\ &\quad - x_2(n) \cdot \sin\left(\frac{2}{3}\pi\right) * h_Q(n) - x_3(n) \cdot \sin\left(\frac{4}{3}\pi\right) * h_Q(n) \\ &= x_1(n) * h_I(n) - \frac{1}{2}[x_2(n) + x_3(n)] * h_I(n) \\ &\quad + \frac{\sqrt{3}}{2}[x_2(n) - x_3(n)] * h_Q(n) \end{aligned} \quad (27)$$

According to equation (23) and (26), the output $y_Q(n)$ can be depicted as

$$\begin{aligned}
 y_I(n) &= x_1(n) \cdot \sin(0) * h_I(n) + x_2(n) \cdot \sin\left(\frac{2}{3}\pi\right) * h_I(n) \\
 &+ x_3(n) \cdot \sin\left(\frac{4}{3}\pi\right) * h_I(n) + x_1(n) \cdot \cos(0) * h_Q(n) \\
 &+ x_2(n) \cdot \cos\left(\frac{2}{3}\pi\right) * h_Q(n) + x_3(n) \cdot \cos\left(\frac{4}{3}\pi\right) * h_Q(n) \\
 &= x_1(n) * h_Q(n) - \frac{1}{2}[x_2(n) + x_3(n)] * h_Q(n) \\
 &\quad + \frac{\sqrt{3}}{2}[x_2(n) - x_3(n)] * h_I(n) \quad (28)
 \end{aligned}$$

Based on the speed priority principle, a FPGA chip can be used to realize the whole structure in Fig.15, and the multipliers work at 180MHz. If the order of the FIR equalization filter is L , $2L$ multipliers are needed to fulfil the equalization process in all. Here we suppose L equal to 33, so the number of the multipliers to fulfil the equalization process are 66 which is half compared to the structures in Fig.13 and Fig.14. The product of $1/2$ and $[x_2(n) - x_3(n)]$ can easily obtained by bit shift technique, so can $1/2$ and $[x_2(n) + x_3(n)]$. Thus, the total using number of multipliers is about 105, therein 37 time division multiplexed multipliers to realize polyphase filter, 66 multipliers to fulfil equalization process and two multipliers to carry out multiplying $\sqrt{3}$ and $[x_2(n) - x_3(n)]$ in two baseband channels.

5 Simulation and Test Results

5.1 Simulation Results

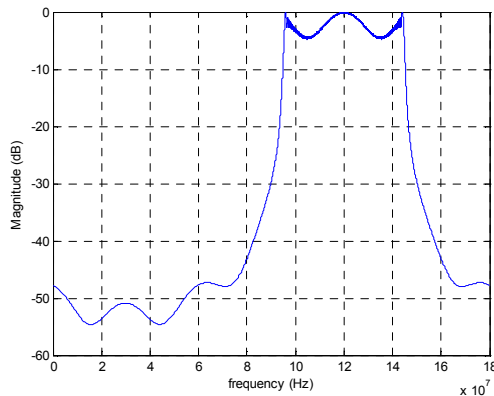


Fig.16 Simulation of anamorphic IF signal

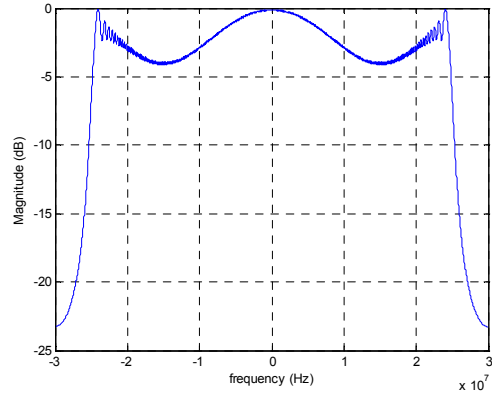


Fig.17 Simulation spectrum after DDC

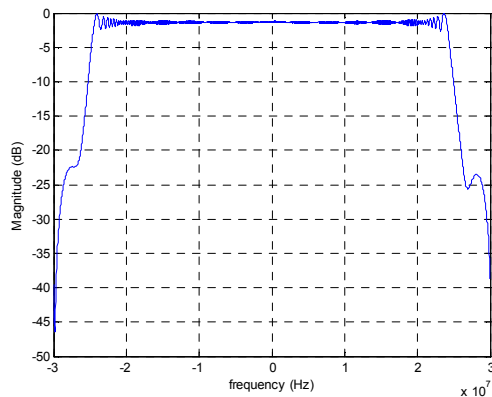


Fig.18 Simulation after DDC and equalization

On the basis of the deduction and analysis above, we carry out the computational simulation to validate the structure in Fig.15. Suppose that the input is anamorphic IF signals, the center frequency is $f_0 = 120MHz$, the signal bandwidth is $B = 50MHz$ and the width of LFM rectangle pulse signal is $T = 40\mu s$. The simulation spectrum of anamorphic IF signal is shown in Fig.16. The simulation spectrum of anamorphic baseband after DDC is shown in Fig.17. The simulation spectrum after DDC and equalization is shown in Fig.18.

From the simulation results above, we can see that the DDC and equalizer work perfectly. The simple structure in Fig.15 which combines DDC and equalization is proven to be valid, feasible and efficient.

5.2 Test Results

We have done an experiment on a test board which shows in Fig.19 and contains one FPGA chip, two

ADC chip and two DAC chip. The two structures as in Fig.14 and Fig.15 have been realized in the FPGA chip. The sampling frequency of ADC is $f_s = 180MHz$. The rate of input data in the FPGA chip is $f_s = 180MHz$, and the output rate is $60MHz$. A Spectrum Analyzer is used to measure the signal frequency spectrum. The test frequency spectrum of anamorphic IF signal is shown in Fig.20.

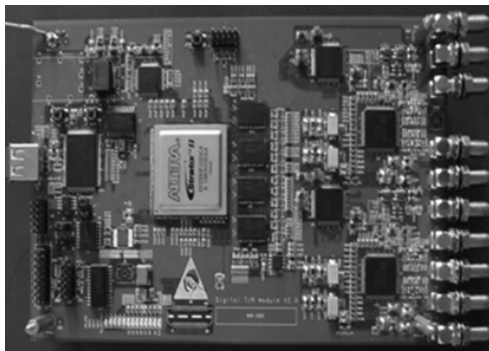


Fig.19 Test Board

EP2S90F1020C4 is used to carry out the effective joint implementation design of channel DDC and equalizer. It is based on a 1.2v, 90nm, all-layer copper SRAM process and features a new logic structure that maximizes performance, and enables device densities approaching 91,000 equivalent logic elements (LEs). And it offers up to 4.5 Mbits of on-chip, TriMatrix memory available without reducing logic resources for demanding, memory intensive applications and has up to 48 DSP blocks with up to 192 (18-bit \times 18-bit) multipliers for efficient implementation of high performance filters and other DSP functions [16].

In our experiments, the number of multipliers needed for realizing the DDC and channel equalizer is relatively larger than that of the logic elements and memory. So the multiplier consumption is our main concern. The order of the FIR filters used in the DDC and equalizer are 111 and 33, respectively. According to the analysis in Sections 3 and 4, using the structure in Fig.13 requires 356 multipliers for realizing the wideband DDC and equalization, which can hardly to be implemented on EP2S90F1020C4. The multiplier consumption of two structures in Fig.14 and Fig.15 are shown in Table 1. From the table, we can see that the multipliers needed for the structure in Fig.15 is about 62% of those in Fig.14. Thus the reduction of multiplier consumption is obvious.

Table.1 Consumption comparison

Structure	Used multipliers	Proportion of used multipliers (%)
Fig.14	170	89
Fig.15	105	55

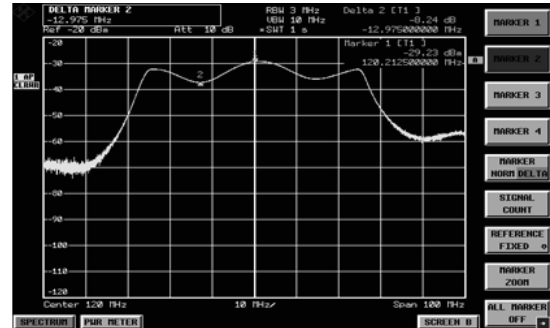


Fig.20 Test spectrum of anamorphic IF signal

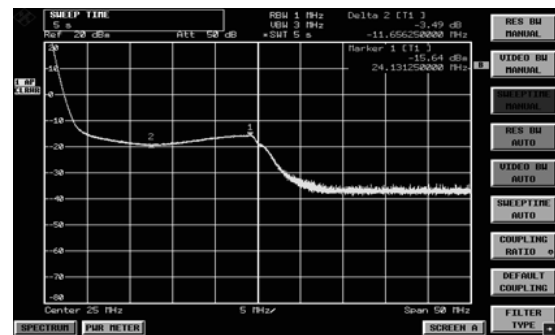


Fig.21 Test baseband spectrum after DDC

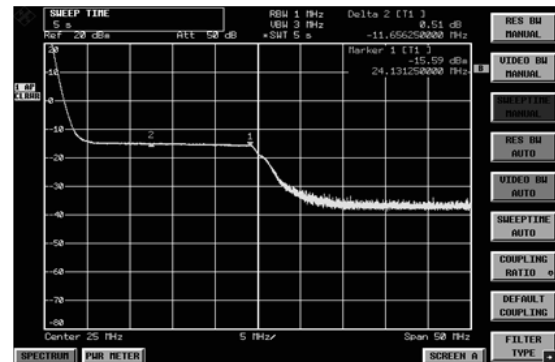


Fig.22 Test spectrum after DDC and equalization

To verify the effect of DDC and equalizer, we send out the baseband signals after DDC and equalization as is shown in Fig.21 and Fig.22. From the test results, we can find that the DDC and equalizer work perfectly.

The IF signal is down converted to baseband signal correctly as is shown in Fig.21. The baseband signal after DDC and equalization is shown in

Fig.22, is almost equal to the ideal baseband LFM signal.

6 Conclusion

Summarily, this paper presents a valid, feasible and highly efficient method to design and implement a simple structure which combines equalizer and DDC with least number of multiplier consumption. We have succeed in realizing the simple structure in a FPGA chip. The reduction of resource consumption is obvious. The corresponding simulation and test results show the obvious improvement to the channel mismatch after equalization and demonstrate the effectiveness of the DDC based on polyphase structure.

References:

- [1] R. J. Mailloux, *Phased Array Antenna (Second Edition)*, Norwood: Artech House, 2005, pp.353-377.
- [2] B. Cantrell, J. de Graaf, Development of a Digital Array Radar(DAR), *IEEE Aerospace and Electronic Systems Magazine*, Vol.17, No.3, 2002, pp. 22-27.
- [3] D. J. Rabideau, R. J. Galejs, et al, An S-Band Digital Array Radar Testbed, *2003 IEEE Int.Symp.on Phased Array System and Technology*, 2003, pp.113-118.
- [4] K. Gerlach, The effects of IF bandpass mismatch errors on adaptive cancellation. *IEEE Trans. on AES*, Vol.26, No.3, 1990, pp. 455-468.
- [5] I. F. Progni, B. W. Nicholson, et al, Impacts of frequency dependent mutual coupling and channel errors on digital beaming antenna performance. Proc. of ION, Nashville, 1998, pp. 275-283.
- [6] D. D. Aalfs, E. J. Holder, Impact of wideband channel-to-channel mismatch on adaptive array, *2000 IEEE Proc. of SAMSP*, 2000, pp. 459-463.
- [7] J. C. Medley, F. C. Dacke, F. J.Adams, The impact of channel dispersion errors and equalisation filtering on subarrayed adaptive beamforming, *2005 IEEE International Radar Conference*, 2005, pp. 703-708.
- [8] J. Russell Johnson, Alan J. Fenn, M. Aumann, An Experimental Adaptive Nulling Receiver Utilizing the Sample Matrix Inversion Algorithm with Channel Equalization, *IEEE Transaction on Microwave theory and techniques*, Vol.39, No.5, 1991, pp. 798-808.
- [9] Shunjun Wu, Yingjun Li, Adaptive channel equalization for space-time adaptive processing, *IEEE International Conference*, 1995, pp. 624-628.
- [10] Simon Haykin, *Adaptive Filter Theory (Fourth Edition)*, Englewood Cliffs: Prentice Hall, 2002, pp.231-446.
- [11] A. Farina, Digital equalisation in adaptive spatial filtering for radar system: a survey, *Signal Processing*, Vol.83, No.1, 2003, pp. 11-29.
- [12] Jianping Li, Research of wideband digital array radar channel equalization, *University of Electronic Science and Technology of China Master dissertation*, 2007, pp.46-64.
- [13] Wang Hong, Lu Youxin, Wang Xuegang, Wan yonglun, Efficient structures for wideband digital receiver, *Journal of Systems Engineering and Electronics*, Vol.17, No.3, 2006, pp. 483-486.
- [14] Wang feng, Fu Youguang, Meng Bing, et al, Performance Analysis and Improvement of the Equalization Algorithm Based on Fourier Transform for Radar Channel, *Acta Electronica Sinica*, Vol.34, No.9, 2006, pp.1677-1680.
- [15] Yong Ran, Xuegang Wang, Lin Zou, Performance of the improved channel equalization method for Wideband Digital Array Radar, *Circuits and Systems. ICCAS 2009. International Conference*, 2009, pp.443-445.
- [16] USA: Altera Corporation, *Stratix II Device Handbook Volume1 & Volume2*, 2007, pp.1-766.