Real Time Generation of the Quinquenary Pulse Compression Sequence using FPGA

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Abstract- Quinquenary codes have been widely used in radar and communication areas, but the design of Quinquenary codes with good merit factor is a nonlinear multivariable optimization problem, which is usually difficult to tackle. To get the solution of above problem many global optimization algorithms like genetic algorithm, simulated annealing, and tunneling algorithm were reported in the literature. All these optimization algorithms have serious drawbacks of non guaranteed convergence, slow convergence rate and require large number of evaluations of the objective function. To overcome these drawbacks, recently we proposed an efficient VLSI architecture for identification of the Quinquenary Pulse compression sequences. Integrating this architecture with the currently proposing architecture provides an efficient real time Hardware solution for identification and generation of the Quinquenary Pulse compression sequences. This paper describes the real time generation of the Quinquenary Pulse compression sequences using Field Programmable Gate Array (FPGA). In this paper an effort is made for the generation of the Pulse compression sequences using an efficient VLSI architecture. The Proposed VLSI architecture is implemented on the FPGA as it provides the flexibility of reconfigurability and reprogrammability.

Key-Words: Pulse compression, Quinquenary sequence, VLSI architecture, FPGA, Merit Factor, Behavioral Simulation.

1 Introduction

Pulse compression for radar is characterized by Meritfactor or Discrimination [1]. But for Radar application a set of sequences could be required such that the Meritfactor of each of the sequences in the set should be as large as possible and simultaneously the cross correlation between any two sequences should be as small as possible. Another major requirement is on the number of sequences in the set. The number of sequences in the set should be as large as possible. All the above requirements are not simultaneously met automatically. The situation is akin to simonization. m- Sequences or Kaiser Sequences cannot be applied for spread spectrum and defense application where secrecy is more important as the sequences are periodic.

Pulse compression can be defined as a technique that allows the radar to utilize a long pulse to achieve large radiated energy but simultaneously obtaining the range- resolution of a short pulse. Theoretically, in pulse compression, the code is modulated onto the pulsed waveform during transmission. At the receiver, the code is used to combine the signal to achieve a high range resolution. Range-resolution is the ability of the radar receiver to identify near by targets.

Pulse compression is a method of breaking the unwanted constraint between range and resolution. Pulse compression radar transmits a modulated pulse, which is both long (having good range characteristic) and wideband (having good resolution criteria). The pulse compression receiver compresses the long received signal of length T into a narrow signal of width l/B. It does this by delaying each sub-part of the input signal spectrum for different amounts so that each sub-part arrives at the output at the same instant. The pulse

compression ratio is T/ (1/B) or B*T.

Range can be defined as the distance between any given point and a target or an object. The range-resolution of radar is the radar ability to distinguish targets that are very closely spaced together in either range or bearing.

The main criterion of good pulse compression is the Meritfactor and discrimination factor.

Let

$S=[x_{0,1}, x_2, x_3 \ldots..x_{N-1}]$ (1)

be a real sequence of length N.

Let $r(k)=\sum_{i=0}^{n-1-k} x_i x_{i+k}$ (2)

Where k=0, 1, 2… N-1 is its aperiodic autocorrelation. The Meritfactor F is defined as the ratio of energy in the main peak and the side lobes.

$$F=\frac{r^2(0)}{2\sum_{k=1}^{N-1} r^2(k)} \quad (3)$$

The Meritfactor F must be as large as possible for good sequence.

Discrimination is used to measure whether coded signal is a good or poor. This means that a code with high discrimination is a good code while a code with low discrimination is a poor code. Discrimination can be defined as a ratio of main peak of autocorrelation function to the magnitude of peak sidelobe value of autocorrelation function.

$$D=\frac{r(0)}{\max|r(k)|_{k\neq 0}} \quad (4)$$

The problem of obtaining long sequences with peaky autocorrelation [2] has long been an important problem in the field of radar, sonar and system identification. It is viewed as the problem of optimization [3-4]. The signal design problem for radar application is suggested by sequences like binary, Polyphase, ternary and Quinquenary sequences. There has been extensive work on binary, Ternary, Four Phase and Quinquenary sequences for obtaining good merit factor or discrimination [5-20]. This work was based on global optimization techniques such as genetic algorithm [4], Eugenic algorithm [20-21], and SKH (Simon-Kronecker-Hamming) algorithm [22]. One of the problems facing the radar pulse compression system designer is accurate generation of the transmitted waveform, given that the capability to generate virtually arbitrarily phase-coded waveforms is required. As described in [23], there are two main techniques, both of which rely on holding a hard copy of the waveform in memory. The first technique is analog, and here the memory is a surface acoustic wave (SAW) device in which the transducer pattern carries the coded waveform. The SAW based pulse compression system has the drawbacks of expansion loss and SAW device insertion loss. The other is digital waveform generation (DWG). The Hardware Implementation architectures for Pulse compression signal processing systems available in the literature have the capability of generating the pulse compression sequences with limited speed [24-25]. Hence we proposed novel and efficient VLSI architectures for the generation of Binary, Ternary and Fourphase Pulse compression sequences [26-27]. In this paper we propose an efficient VLSI architecture that can generate Quinquenary Pulse Compression sequences with FPGA clock rate.

2 Proposed architecture

The Quinquenary phase pulse compressed sequence elements are +1, +2, -1, -2, and 0. The element +1 is transmitted as sinusoidal with an amplitude of 1 unit, the element +2 is transmitted as sinusoidal signal with an amplitude of 2 units, the element -1 is transmitted as sinusoidal signal with a negative amplitude of 1 unit, the element -2 is transmitted as sinusoidal signal with a negative amplitude of 2 units, and during the period of the element ‘0’, no signal is transmitted. The VLSI architecture for generation of Quinquenary phase pulse compression sequences using FPGA for the purpose of transmission shown in fig.1. Memory1, Memory2, Memory3, Memory4 and Memory 5 shown in fig.1. are of 8 x 8 bits.Memory1 holds the information of 8 sample values of the sinusoidal signal with an amplitude of 1 unit. Memory2 holds the information of 8 sample values of the sinusoidal signal with amplitude of 2 units. Memory3 holds the

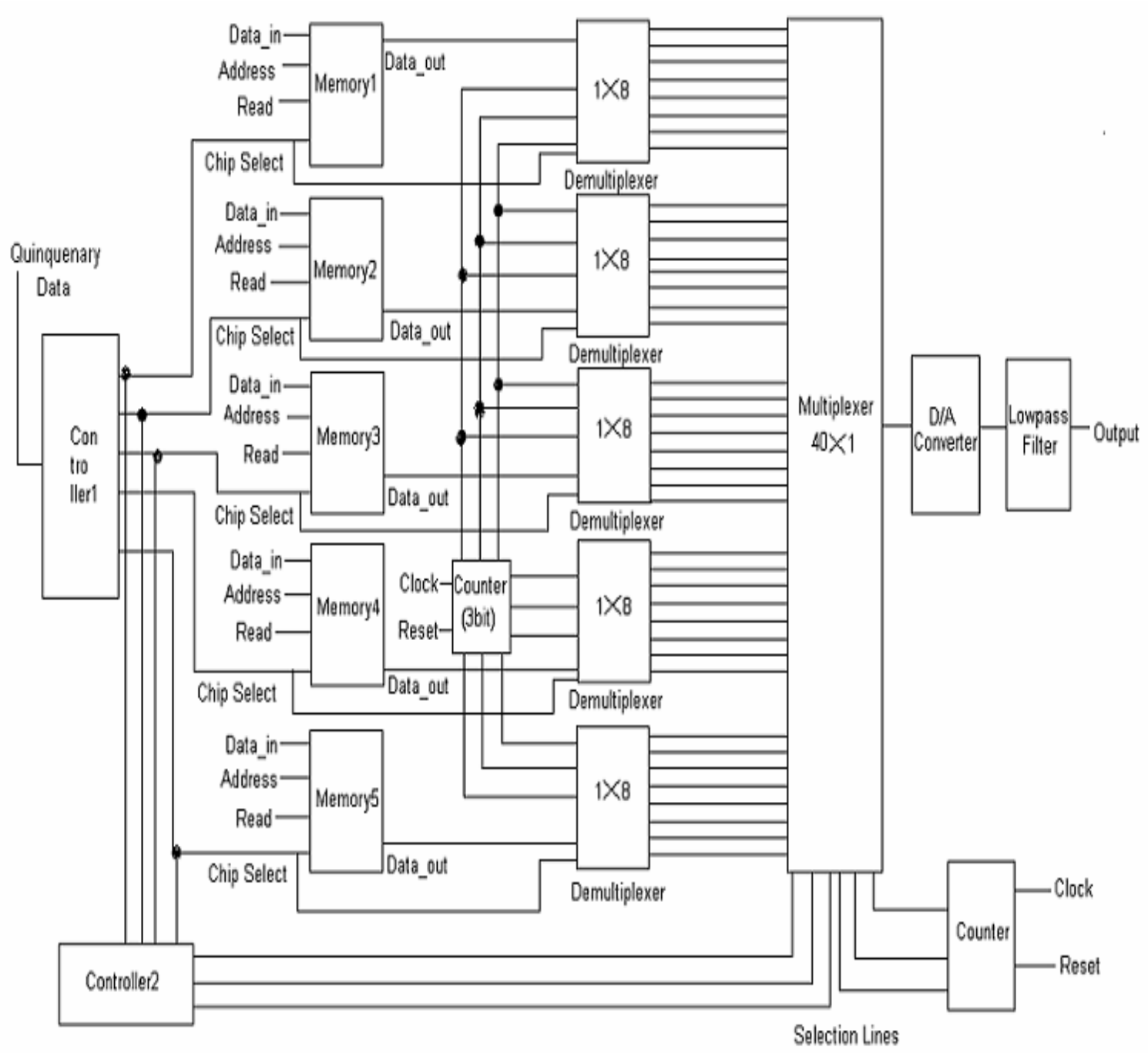

Fig. 1. VLSI Architecture for generation of Quinquenary phase Pulse Compression Sequences

information of 8 sample values of the sinusoidal signal with negative amplitude of 1 unit, Memory4 holds the information of the sinusoidal signal with negative amplitude of 2 units and Memory5 holds the information of the sinusoidal signal with zero amplitude. When the Quinquenary phase pulse compression sequence element is +1, the 8 locations of memory1 are read. When the Quinquenary phase pulse compression sequence element is +2, the 8 locations of Memory2 are read. When the Quinquenary phase pulse compression sequence element is -1, the 8 locations of Memory3 are read When the Quinquenary phase pulse compression sequence element is –2, the 8 locations of Memory4 are read and when the Quinquenary phase pulse compression sequence element is 0, the 8 locations of Memory5 are read. Based on Quinquenary phase pulse compression sequence element value '+1' or '+2' or '-1' or '-2' or '0' to send data of 8 locations of Memory1 or Memory2 or Memory3 or Memory4 or Memory5 serially to D/A Converter, Demultiplexer and, Multiplexer logic is shown in fig.1. To read all the 8 locations of Memory1 or Memory2 or Memory3 or Memory4 or Memory5, the architecture shown in fig.1. takes 8 clock cycles. This means that if 'K' Hz clock is used to read Memory1, Memory2, Memory3, Memory4 and Memory5 the frequency of the sinusoidal signal generated with an amplitude of '+1' or '+2' or '-1' or '-2' or '0' at filter out is K/8 Hz.

Therefore the frequency of sinusoidal signal generated to represent Quinquenary phase pulse compression sequence using architecture shown in fig.1. is determined by the frequency of the clock signal applied to the Memory1, Memory2, Memory3, Memory4 and Memory5.The clock signal applied to Memory1, Memory2, Memory3, Memory4 and Memory5 has wide range up to clock rate of FPGA.
Therefore the architecture shown in fig.1. can generate sinusoidal signal to represent Quinquenary phase pulse compression sequences with frequency range up to FPGA clock rate divided by 8..Since this proposed architecture shown in fig.1.is targeted to FPGA, throughout this paper the +1 of Quinquenary phase pulse compression sequence is represented by 001,-1 is represented by 011 ,+2 is represented by 101 , 0 is represented by 000 and -2 is represented by 111.

3 Technology and Tools

The architecture shown in fig.1. has been authored in VHDL and its synthesis was done with Xilinx XST.
The VHDL model was simulated and validated both functional and post-synthesis with Xilinx ISE 9.1. Xilinx ISE foundation 9.1i has been used for performing, mapping, placing and routing for Behavioral simulation Modelsim 6.0 has been used. The synthesis tool was configured to optimize for area and high effort considerations.

4 FPGA implementation and Results

The use of the FPGA technology was chosen due to it provides some important advantages over general purpose processors and Application Specific Integrated Circuits (ASICs) such as: 1) FPGAs provide massive parallel structures and high density logic arithmetic with short design cycles compared to ASICs, 2) In FPGA devices, tasks are implemented by spatially composing primitive operators rather than temporally, 3) In FPGAs, it is possible to control operations at bit level to build specialized data-paths. The targeted device was Spartan-3 xa3s1500fgg676-4 with detailed specifications at [28].The behavioral simulation results for the architecture shown in Fig.1 are shown in Fig.2, Fig.4. Fig.6, Fig.8 Fig.10.andfig.12.for all combinations of Quinquenary pulse compression sequence elements. Fig.2 shows the generated Quinquenary Pulse Compression Sequence for the alphabets '+1 'and '+2'. Fig.4 shows the generated Quinquenary Sequence for the alphabets '1 'and '-2'. Fig.6 shows the generated Quinquenary Sequence for the alphabets '-1 'and '+2'. Fig.8 shows the generated Quinquenary Sequence for alphabets '-1 'and '-2'. Fig.10 shows the generated Quinquenary Sequence for the alphabets '+2' and '0'. Fig.12 shows the generated Quinquenary Sequence for alphabets '+2' and '-2'.
Fig.3, Fig.5, Fig.7, Fig.9, Fig.11 and Fig.13 show the sampled Quinquenary waveform for all combinations of Quinquenary pulse compression sequence elements represented in Binary. Fig.14 shows the RTL schematic of the proposed architecture that was obtained with the aid of the ISE 9.1i. Fig.15 shows the Pinout and Area Constraints Editor Diagram.

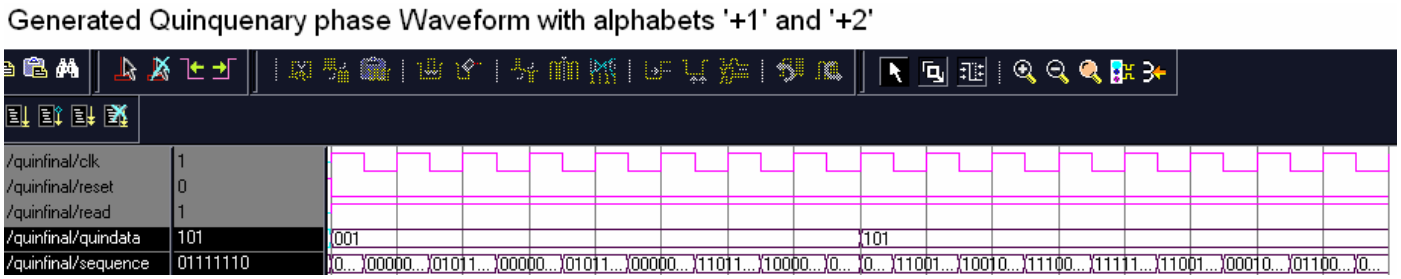

Fig. 2. Generated Quinquenary phase Sequence for alphabets '+1 'and '+2'

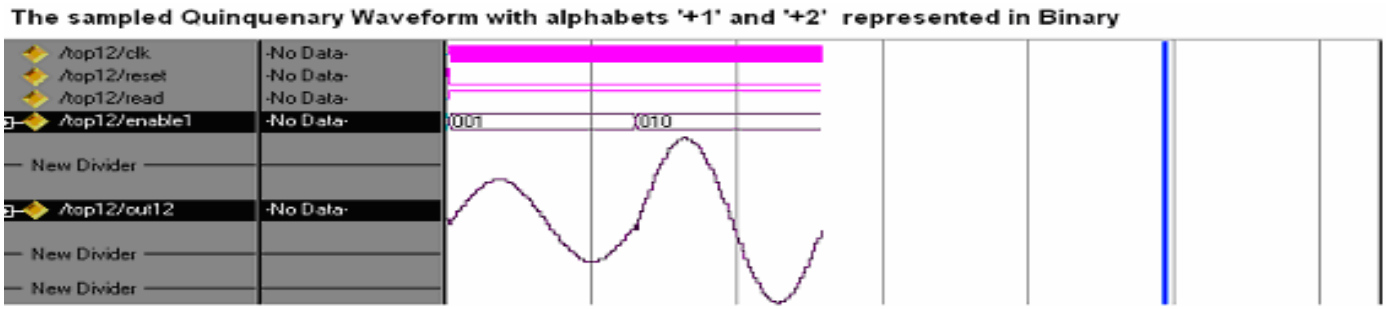

Fig.3. The sampled Quinquenary waveform for alphabets '+1 'and '+2'

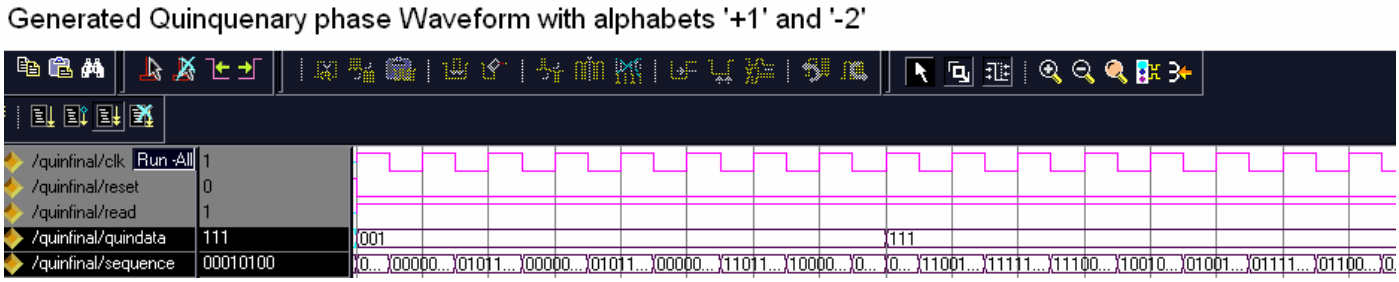

Fig. 4. Generated Quinquenary phase Sequence for alphabets '1 'and '-2'

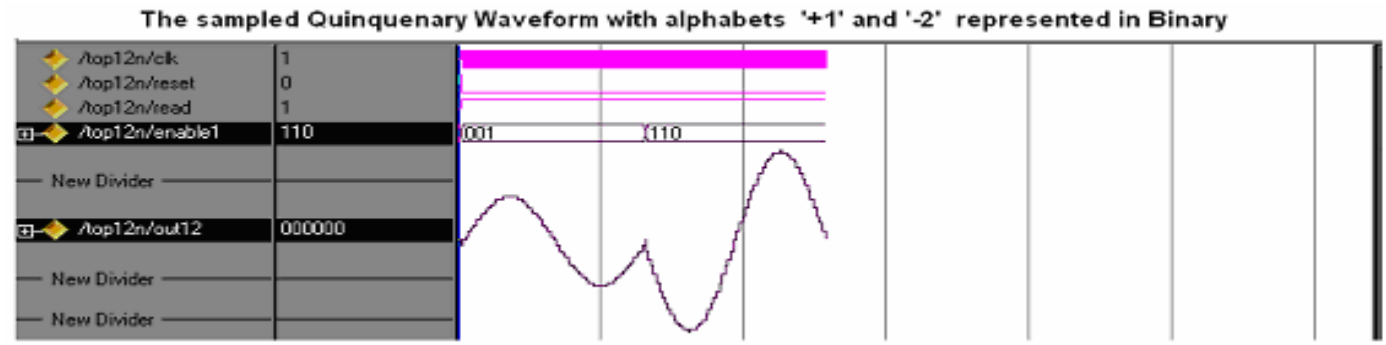

Fig.5. The sampled Quinquenary waveform for alphabets '1 'and '-2'

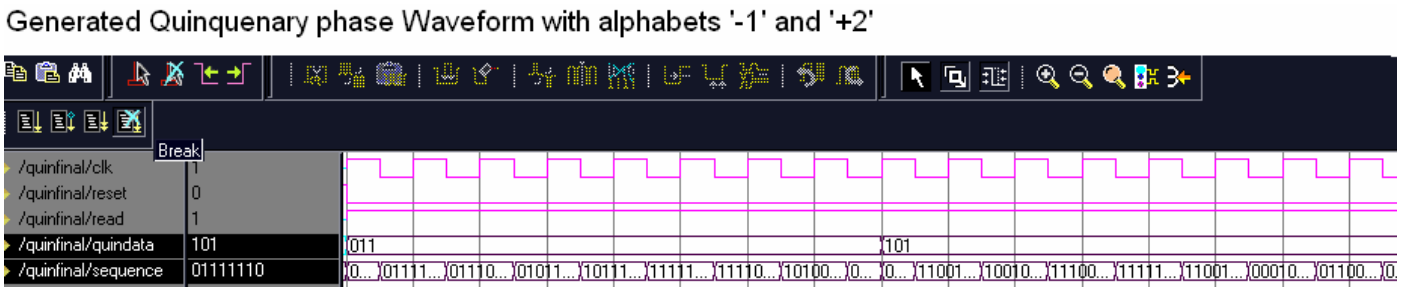

Fig. 6. Generated Quinquenary phase Sequence for alphabets '-1 'and '+2'

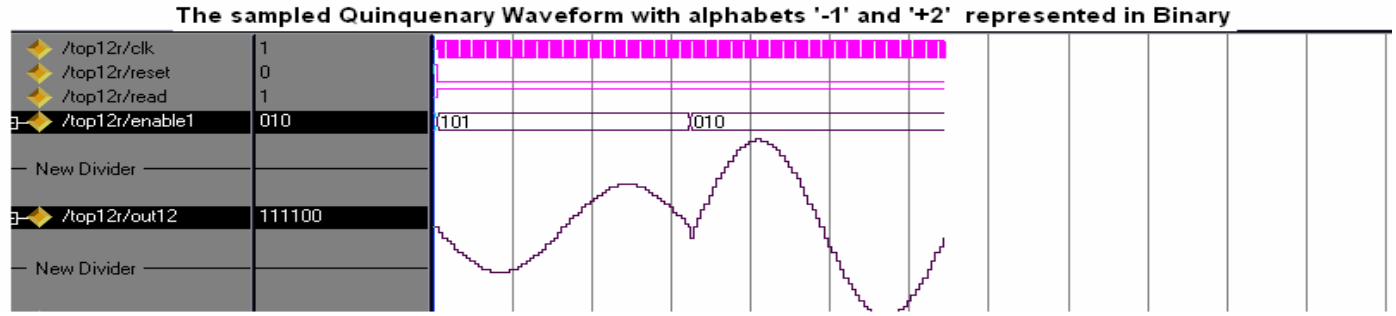

Fig.7. The sampled Quinquenary waveform for alphabets '-1 'and '+2'

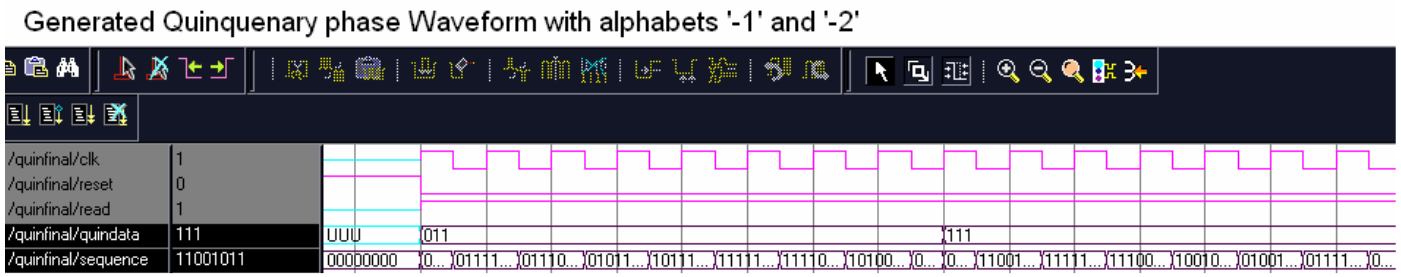

Fig. 8. Generated Quinquenary phase Sequence for alphabets '-1' and '-2'

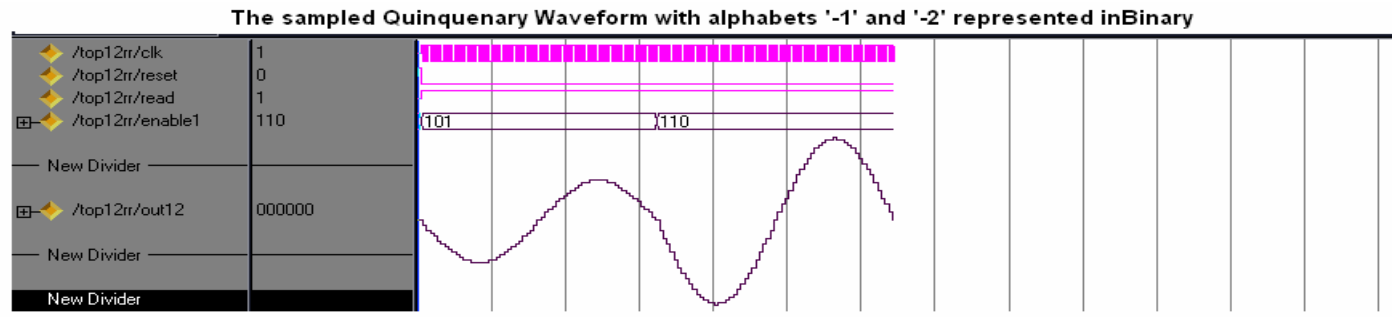

Fig.9. The sampled Quinquenary waveform for alphabets '-1' and '-2'

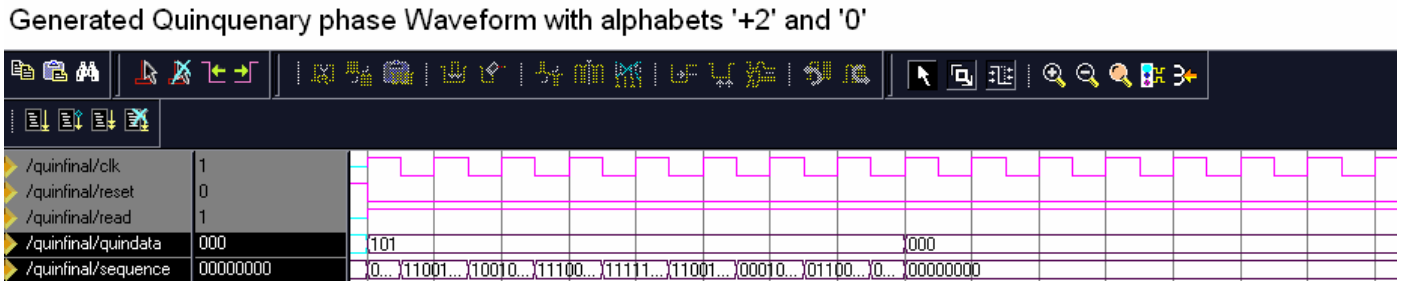

Fig.10. Generated Quinquenary phase Sequence for alphabets '+2' and '0'

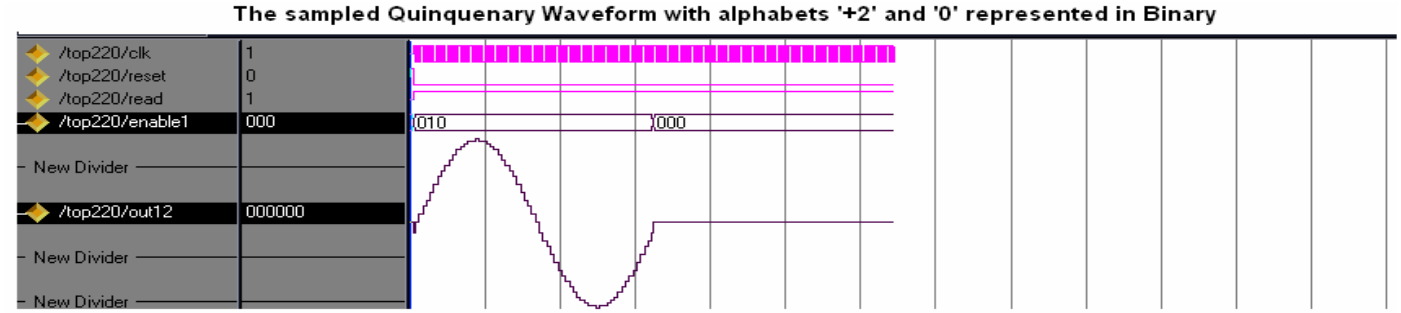

Fig. 11. The sampled Quinquenary waveform for alphabets '+2' and '0'

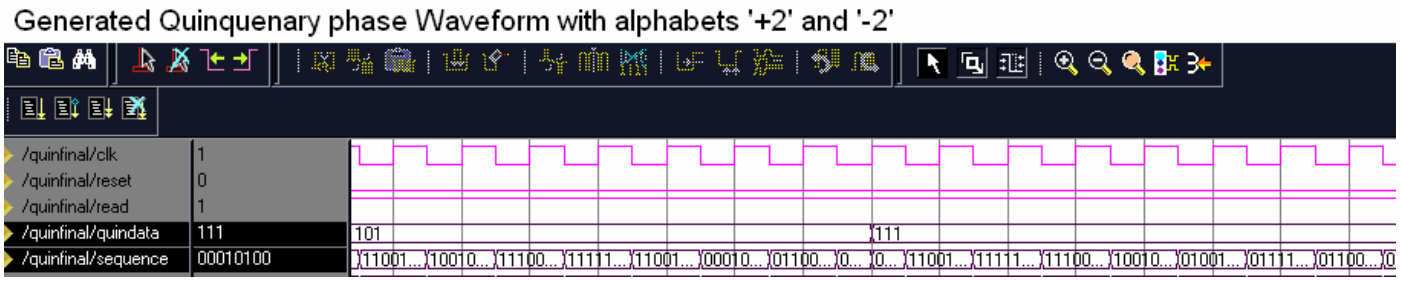

Fig. 12. Generated Quinquenary phase Sequence for alphabets '+2' and '-2'

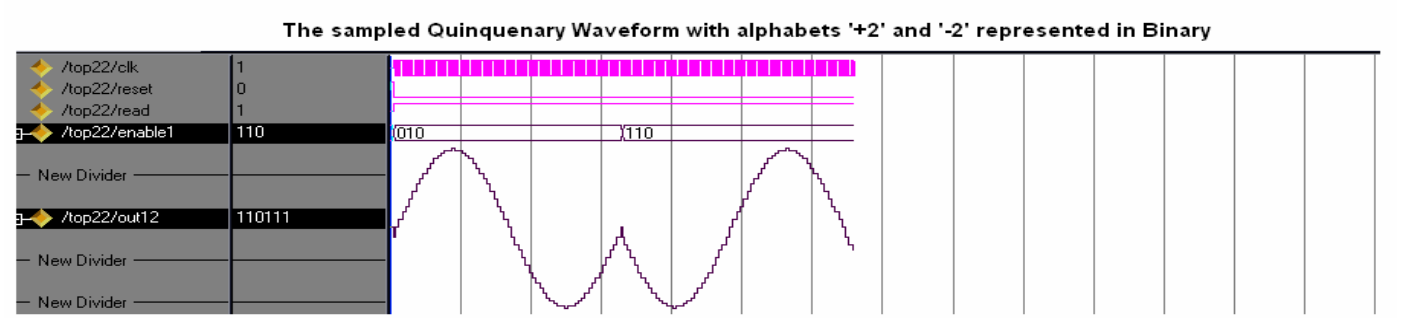

Fig.13. The sampled Quinquenary waveform for alphabets '+2' and '-2'

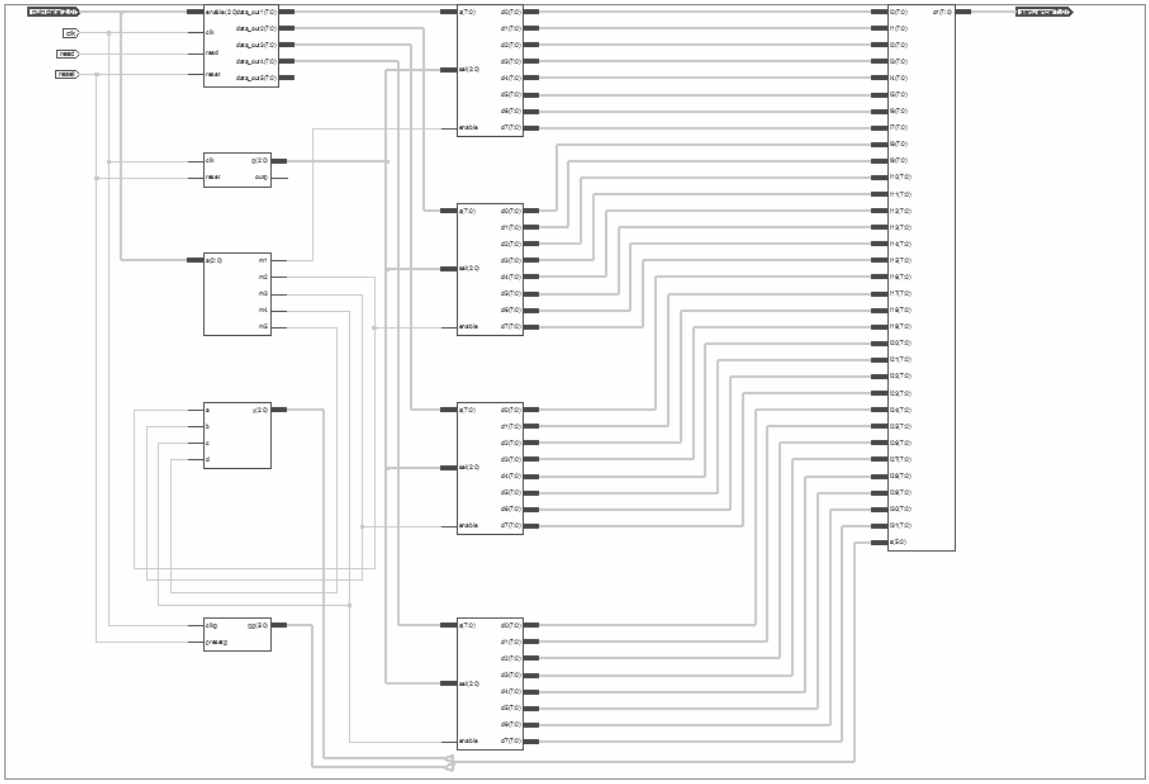

Fig.14 RTL schematic of the proposed architecture

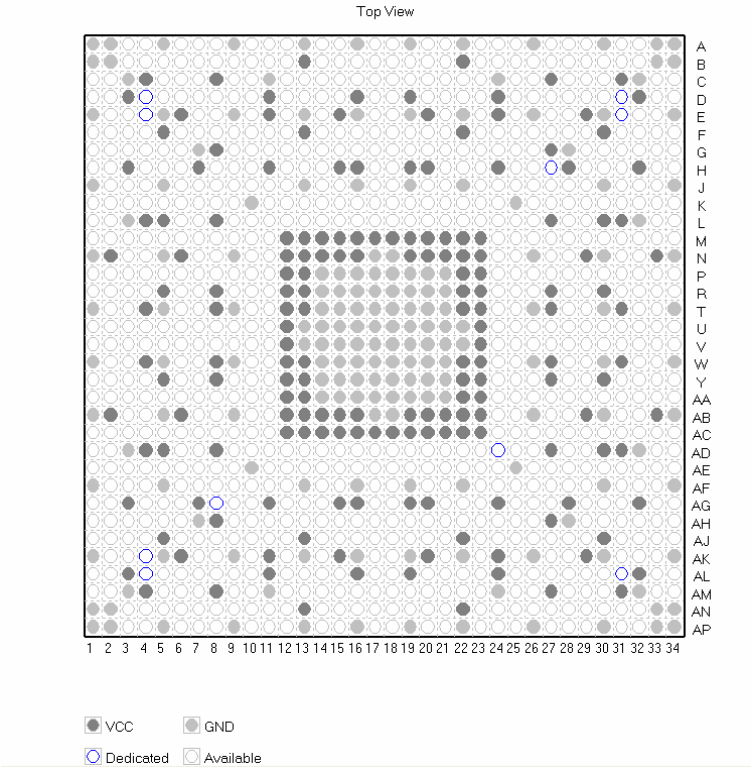

Fig.15 .Pinout and Area Constraints Editor Diagram

Design Summary:		
Number of errors:	0	
Logic Utilization:		
Number of 4 input LUTs:	13 out of 66,560	1%
Logic Distribution:		
Number of occupied Slices:	7 out of 33,280	1%
Total Number of 4 input LUTs:	13 out of 66,560	1%
Number of bonded IOBs:	11 out of 784	1%
Total equivalent gate count for design:	113	
Additional JTAG gate count for IOBs:	528	
Peak Memory Usage:	201 MB	
Total REAL time to MAP completion:	5 secs	
Total CPU time to MAP completion:	4 secs	
Timing Summary:		
Minimum input arrival time before clock:	2.835ns	
Maximum output required time after clock:	8.965ns	

Table I Design Implementation summary for the generation of Fourphase Pulse Compression sequence

5. Conclusion

In this paper we have proposed and implemented a novel and efficient VLSI architecture for generation of Quinquenary phase pulse compression sequence for the purpose of transmission. The architecture proposed in this paper has the flexibility of varying the generated signal frequency up to clock rate of FPGA divided by 8, which has virtually no cost. The generated pulse compression sequences have stable frequency. The latest FPGA Virtex-5 has a clock frequency of 550 MHZ. The proposed VLSI architecture can generate pulse compression sequences with a frequency of clock rate of Virtex-5 divided by 8 with out using up conversion. Further to get high frequency pulse compression sequences an up converter may be used at the output of the proposed VLSI architecture shown in the fig.1. The Memory size of the Memory blocks in the architecture of the fig.1. can be extended to 256 x 8 bits for higher resolution of the generated waveform.

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