Synchronised Linear Ramp-Pulse Based Triggering Pulse Generation ON/OFF Control for Solid-State Switches: Capacitor Switching Applications

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Abstract: -This paper describes a newly developed triggering circuit, has been use to turn on and off the solid-state switches, such as TRIAC switched capacitors applications. A linear ramp signal based synchronization technique has been propose and implemented successfully, for the capacitor switching operation of a simple power system. This scheme enables the firing circuit to adjust itself against any phase and/or sequence alterations. This feature leads to elimination of the phase locked-loop (PLL) control, are commonly used to synchronize the pulse generations with respect to the system the supply frequency. Those pulses are, to control the converter / inverter operation of an industrial drives and the FACTS controllers also. The proposed circuit has been constructing and tested experimentally in the laboratory. The simulation work completed using Or CARD software. The result shows a good agreement with the theoretical waveforms.

Key Words: - *linear ramp signal, synchronization, capacitor switching*

1 Introduction

In electrical drives applications either in industries or in elsewhere, induction motors are widely used. Therefore, the system has a low power factor. The shunt-connected capacitors are widely used to improve the power factor. In addition to that, shunt capacitors have been to regulate the voltage of the transmission line at the receiving end. In earlier days, mechanical switches used to connect the capacitor in aforementioned applications. After the development of power semiconductor devices with higher power handling capabilities and current ratings, solid-state switches (like thyristors, IGBT, GTO, MOSFET, TRIAC etc..) are used instead of mechanical switches, because of its compactness and easy to control.

Static power conversion manufacturers have developed a variety of thyristor firing circuits based on commercially available discrete and integrated circuits. Ainsworth [1] has presented a phase locked oscillator control system for thyristor-controlled reactor. Frank J. Bourbeau [2] developed, LSI based three-phase thyristor firing circuit insensitivity to frequency and direction of phase rotation with PLL circuit. A microprocessor based firing circuit for thyristors working under a three-phase variable frequency supply has been suggest and implemented by H. M. EL Bolok [3]. In his work, zero crossing has been detected and to fix the frequency reference. L.S.Torseng [4] discussed the reactive power compensation of a power system by thyristor switched capacitors (TSC) and thyristor controlled reactor (TCR) schemes. In view of capacitor switching operation, T.J.E Miller [5] and N. H. Hingorani et al [6] have discussed the constraints and control strategy.

In case of stand-alone power generators, such as self-excited induction generator, excitation control says, either adding or removing the capacitor to the stator windings of the generators. T.A. Ahemed et al [7] discussed the terminal voltage regulation of a three-phase capacitor excited induction generator using switched capacitor and fixed capacitor-thyristor controlled reactor with zero crossing technique. In single-phase generator, also the same technique has been implemented [8]. Ebenezer Prates Da Silveira et al. [9] describe the low cost optical TRIAC with a built in zero-crossing function based voltage regulation of three phase induction motor with direct on line staring.

However, aforementioned applications need a separate control, to synchronize the frequency and pulse generations. The aim of this work, propose a new technique, can be automatically synchronised with supply frequency variations. Analog and digital integrated circuit based triggering pulse generation circuit (with less number of component) has been

develop and tested in the laboratory.

2 Proposed Triggering Circuit

The proposed triggering circuit, shown in Fig.1, consist of a single-phase full bridge diode rectifier, ramp pulse generator, comparator, edge detector, opto coupler and buffer circuit.

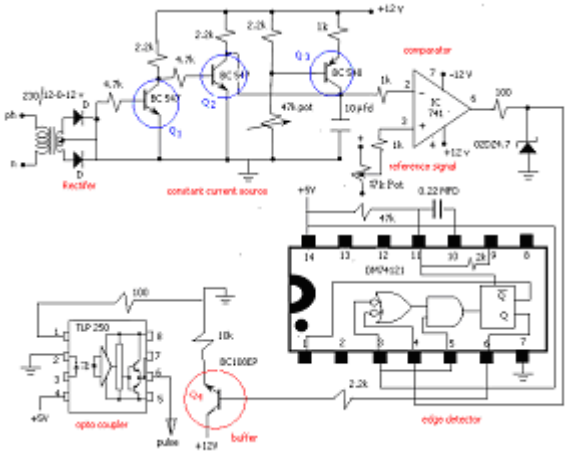

Fig.1 Proposed triggering pulse generation circuit for ON/OFF control of TRIAC switch

Descriptions of the individual blocks have been discusses in sub-sequence paragraphs in details. Fig.2 illustrates the typical waveform of the triggering circuit at different points, had been used for TRIAC switch ON/OFF control.

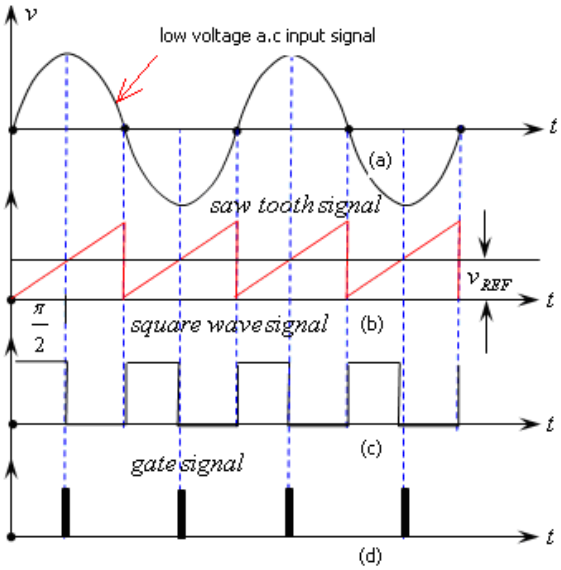

Fig.2 Typical waveform of proposed triggering circuit

3 Principle of operation

Fig.3. shows a 3-Ø inductive load powered from a variable frequency, capacitor excited induction generator. Low-level voltage signal of load voltage has taken from the load terminal, feeding to the triggering pulse generation circuit.

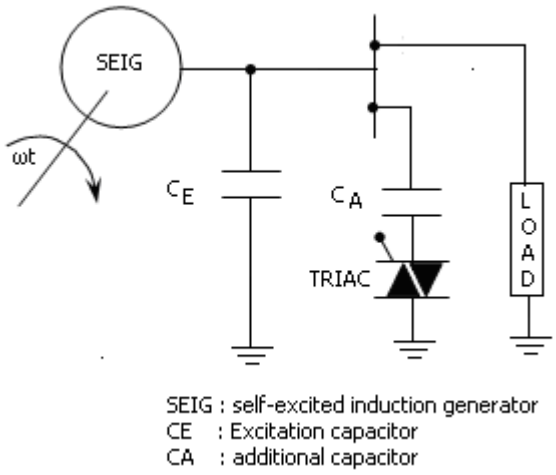

Fig.3. single line diagram of variable frequency generator with load and TRIAC switched capacitor

3. 1 Full bridge rectifier

Fig.3 (a) depicts the full bridge rectifier, consists of a shunt-connected transformer, two diodes D_1 and D_2 connected in secondary windings of the transformer. Load voltage of 230V (line-to-neutral) applied to the transformer primary as shown in Fig.3 (b). The secondary voltage of 12V, ac (feed back signal) rectified by the diodes (as shown in Fig.3(c), and, feeding to the next stage of constant current source.

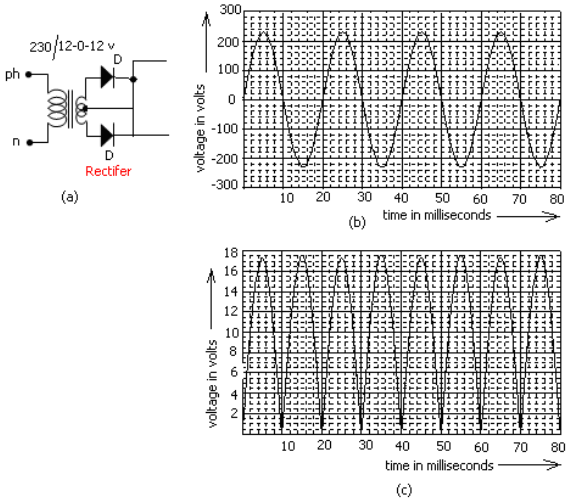

Fig.3 full bridge diode rectifier (a) circuit connection (b) simulated input voltage (c) rectified voltage waveforms

3. 2 Ramp Signal Generation

The base of the transistor Q_1 biased by the rectifier voltage using 4.7 kΩ resistance (R_1) if the base voltage, above 0.7 V, Q_1 conducts and the collector to emitter voltage is zero. When base voltage is between 0V and 0.7V, Q_1 is OFF, therefore, 12V dc, divides between 2.2 kΩ (R_2) and 4.7 kΩ (R_3) resistances. The collector to emitter

voltage waveform of Q_1 is showing in Fig. 4(b). This voltage applied to the base of Q_2. This causes Q_2 to turn on when Q_1 is off and to turn off when Q_1 is on. The collector to emitter voltage waveform of Q_1 is showing in Fig.4 (b). Resistors R_5 and R_6 form a voltage divider bias for transistor Q_3. The base voltage of Q_3 varies by varying the resistor R_6. It is adjusted such that Q_3 conducts always, thus charging the capacitor C_3. However, at the end of each half cycle, when voltage is going from 0.7V to 0V, Q_2 conducts hence discharging the capacitor to ground. This charging and discharging in each half cycle produces a ramp wave. It is showing in Fig.4(c) along with the full wave rectified sine wave to show the synchronization of the ramp with the input supply.

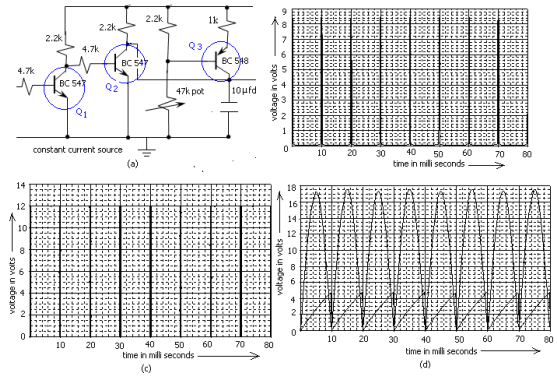

Fig.4 constant current source (a) circuit connection (b) simulated collector-to-emitter voltage of transistor Q_1 (c) corresponding ramp signal

The advantages of this firing circuit are to generate a linear and synchronised ramp wave generation and self-adjust the firing instant with frequency variation, therefore, no need of separate synchronism control loop. Any change in frequency of the input signal will cause a corresponding change in the period of the ramp. This can be eliminating the phase locked loop (PLL) adjustment usually needed due to synchronise the firing signal generation with frequency variations.

2. 3 Comparator Circuit

An integrated circuit (IC) of uA741 operational-amplifier (op-amp) has been used as comparator as shown in Fig.5 (a). The synchronised ramp wave and reference signal are given to the inverting terminal and non-inverting terminal of the op-amp respectively. +12V DC is given to the seventh pin and -12V DC is given to the fourth pin of the op-amp. The op-amp compares the ramp with the reference signal as shown in Fig.5(b). When the instantaneous value of the ramp is lower than the reference signal, the output of the op-amp goes to positive saturation voltage of the op-amp. As soon as the instantaneous value of the ramp becomes more than the reference dc voltage, the output goes to negative saturation voltage of the op-amp, thus a square wave (as shown in Fig. 5(c)) produced. The on time of the square wave, varies by changing the value of the reference dc voltage.

The output of the op-amp applied as an input to the edge detector IC. Since it is a digital IC, a maximum of 5 volts is allowing to its input terminals. Therefore, 4.7V zener diode (02DZ4.7) has been connecting in front of the edge detector circuit. Fig.5(c) shows the square wave, which is the output of zener diode terminal.

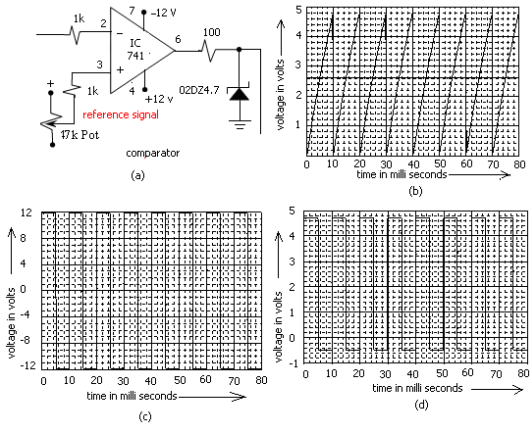

Fig.5 (a) Input signals to op-amp; (b) Output of op-amp; (c) Output at zener diode

2. 4 Edge Triggering

An IC of DM74121, used as edge detection circuit as shown in Fig.6 (a). The IC could detect both positive (rising) and negative (falling) edges, depending on the mode of operation. The negative edge-triggering scheme chosen (Fig.6 (a)), for that, an external connection has been modifying by using the logic shown in Fig.6 (b).

IC DM74121 is a monostable multi-vibrator featuring both positive and negative edge triggering with complementary outputs. An internal $2k\Omega$ timing resistor is using to design convenience minimizing component count and layout problems. This device could be use with a single external capacitor. Inputs (A) are active-LOW trigger transition inputs and input (B) is an active-HIGH transition Schmitt trigger input that allows jitter-free triggering from inputs with transition rates as slow as 1 volt/second. A high immunity to VCC noise of typically 1.5V is providing by internal circuitry at the input stage. The main features of the IC are, can be triggered from active-HIGH transition or active-LOW transition inputs; the pulse width can be varied from 30 ns to 28 seconds; excellent noise

immunity of typically 1.2V; Stable pulse width up to 90% duty cycle. The function of the IC is as given in Fig. 6 (b). Here, the first mode has been choosing where the inputs A_1 and B are high and a negative edge is giving to the input A_2. This produces a positive pulse at the output Q and a negative pulse $\vec{Q}$. The output at Q used for the next stage. The pulse width is keeping at three milliseconds by adjusting the external resistor. The reason is that to fire the TRIAC in series with the capacitor, in TSC, at least 30% on-time pulse is required. Fig.6(c) shows the output of DM74121.

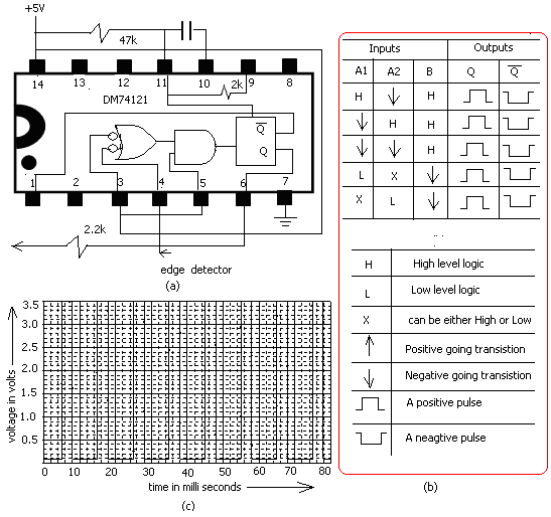

Fig.6 Edge triggering scheme (a) connection diagram (b) logic for connection (c) output waveform

4 Experimental Work

To validate the proposed triggering circuit, a 240V, 4,7A, capacitor excited induction generator (as shown in Fig.3 single line diagram) rig up in the laboratory, generates the voltage with variable frequency. A TRIAC switched capacitor used as a voltage regulator.

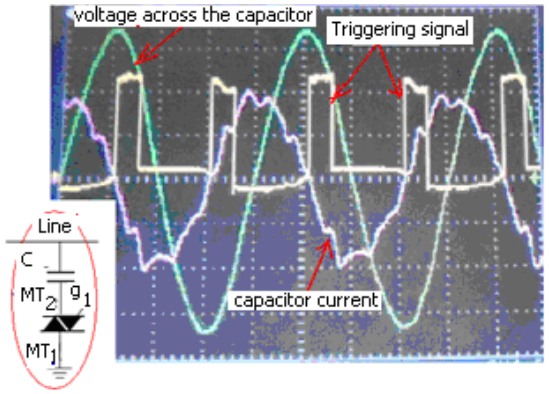

Fig.7 experimental results

Fig.7 illustrates the capacitor voltage, capacitor current and triggering pulse, captured during the experimental work. A single leg of a 3-Ø triac switched capacitor (shown in Fig.7 with in a circle). The capacitor current shows harmonics, it will be eliminates by introducing a small value of inductor in series with capacitor.

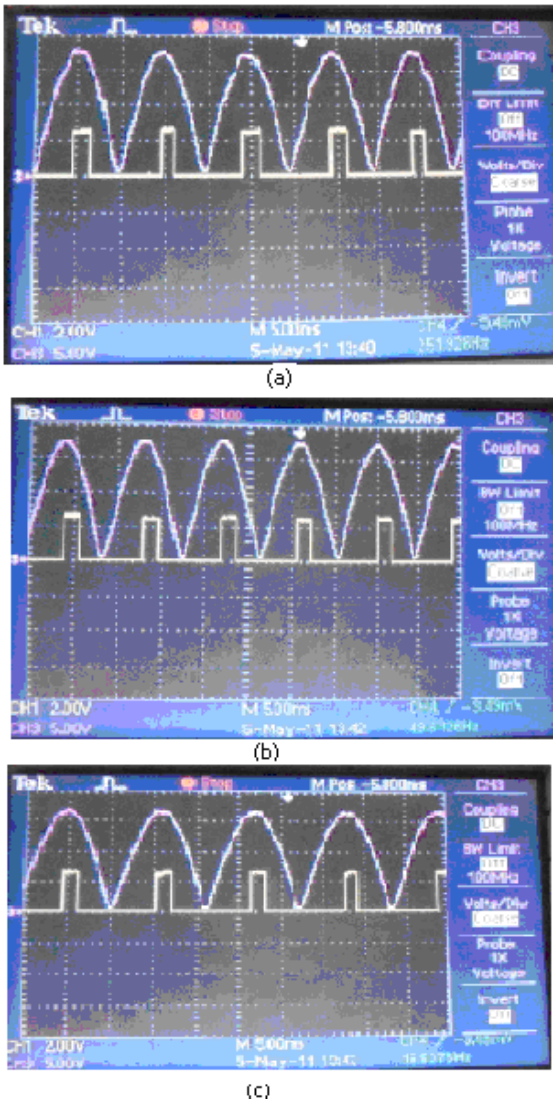

Fig.8 experimental results of self-synchronizations with a frequency of (a) -50 Hz (b)- 55 Hz (c) -45 Hz

5 Conclusions

The proposed triggering circuit has been constructing tested, as a voltage regulator of a 3-Ø self-excited induction generator. The observations are

- TRIAC switch goes to OFF state suddenly (shown in Fig.9) after turn ON, in addition negative half-cycle capacitor current goes to zero values.
- A pure capacitor connection generates a harmonics and huge amount of capacitor currents are presents.

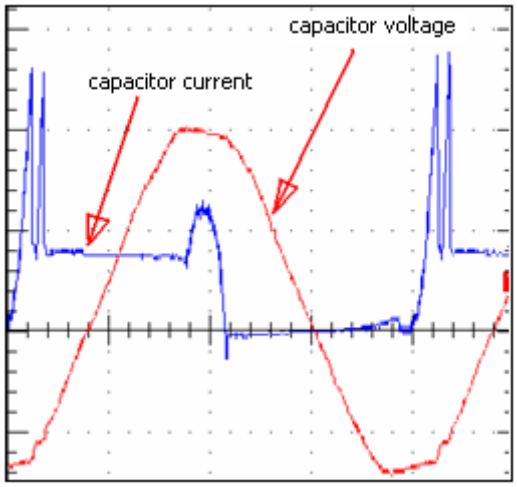

Fig.9 First stage test result of TRIAC switched capacitor

I would like to thanks my doctoral committee member's suggestions, to eliminate the problem shown in Fig.9, by modification of the triggering circuit shown in Fig.1.

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