

PI, PID and Fuzzy Logic Controlled Cascaded Voltage Source Inverter based Active Filter for Power Line Conditioners

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Abstract: - This paper presents a PI, PID and Fuzzy Logic Controller (FLC) based shunt active filter for power line conditioners (PLC) to improve the power quality in the distribution network. This active power filter is implemented with current controlled cascaded multilevel voltage source inverter (VSI). It is connected at the point of common coupling for compensating harmonic and reactive power by injecting equal but opposite harmonic compensating currents. The reference current extraction is based on sensing main currents only, which require current harmonics and reactive volt-ampere compensation. The PI or PID or fuzzy logic controller is used to estimate the peak reference current by controlling the dc-bus capacitor voltage of the cascaded inverter. The cascaded multilevel inverter switching signals are derived from triangular-sampling current controller; it gives a good dynamic performance under steady state and transient operations. The cascaded active filter system is validated through extensive simulation under steady state and transient conditions with different non-linear loads. These simulation results have been revealed that the cascaded active power filter performs perfectly in conjunction with PI or PID or FLC. A comparative assessment of these three different controllers is disclosed.

Key-Words: - Active Power Line Conditioners (APLC), PI and PID Controller, Fuzzy Logic Controller (FLC), Triangular-Sampling current controller, Harmonics, Power quality

1 Introduction

As in recent years, power quality and custom power have been most research topics because of widespread use of non-linear electronic equipments such as rectifiers, switched mode power supply (SMPS), incandescent lighting and motor drive applications etc.[1-2]. These non-linear loads create harmonic or distortion current and reactive power problems [3-5]. These harmonics induce the malfunctions in sensitive equipment, overvoltage by resonance, increase heating in the conductors, harmonic voltage drop across the network impedance and affect other loads connected at the same point of common coupling (PCC) [6-8]. Traditionally passive LC filters have been used to compensate the harmonic distortion and the reactive power; but passive filters are large in size, aging and tuning problems, resonate with the supply impedance and fixed harmonic compensation [9-10]. To solve these problems, many different configurations of static VAR compensators (SVCs) have been proposed. Unfortunately some SVC generates lower-order harmonics themselves and the

response time of SVC system may be too long to be acceptable for fast-fluctuating loads [11-14]. Recently active power line conditioners (APLC) or active power filters (APF) overcome these problems and formulated for compensating harmonics and reactive power simultaneously due to fluctuating loads [15-16]. This active power filter can be connected in series for compensate the voltage harmonics and in parallel for compensate the current harmonics, but the series active filter is not found in common practical applications. Most of the industrial usage required current harmonic compensation, so the shunt active filter is popular than series active power filter [17-19].

The controller is the most significant part of the APF and currently lot of research is being conducted in this area. [20-13]. Conventionally, PI and PID controllers have been used to extract the fundamental component from the distorted current(s) and simultaneously control DC-bus capacitor voltage of the cascaded inverter [24-15]. However, these controllers require precise linear mathematical model of the system, which is difficult

to obtain under parameter variations and load disturbances. Recently, Fuzzy Logic Controllers (FLC) is used in power electronic systems, adjustable motor drives and active power filter applications [26-29]. The advantages of FLC are over the conventional controllers are: It does not need accurate mathematical model; it can handle nonlinearity and is more robust than conventional controllers [20-32].

This paper presents a PI, PID and FLC based cascaded shunt active power filter for the harmonics and reactive power mitigation of the non-linear loads. The cascaded H-bridge active filter has been applied for power quality applications due to increase the number of voltage levels, low switching losses and higher order of harmonic elimination [33-35]. The cascade M-level inverter consists of (M-1)/2 H-bridges and each bridge has its own separate dc source. The cascaded multilevel voltage source inverter switching signals are generated using proposed triangular-sampling current controller; it provides a dynamic performance under transient and steady state operation. The proposed PI or PID or fuzzy logic controller is control the dc-bus capacitor voltage of the cascaded inverter and estimate the required peak reference current. The shunt cascaded APF system is validated through extensive simulation and investigated under steady state and transient conditions with different non-linear loads.

2 Design of Shunt APLC System

Shunt APF is connected in the distribution grid at PCC through filter inductance and operates in a closed loop.

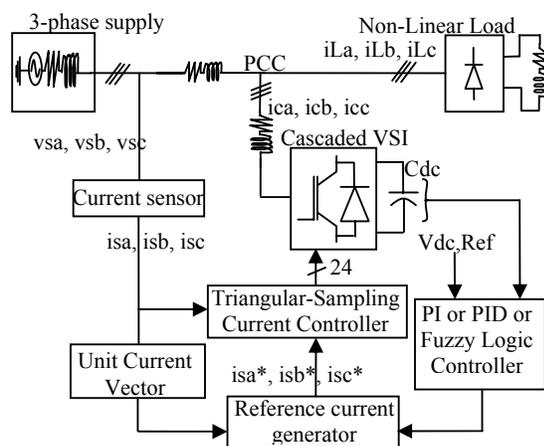


Fig 1 shunt active power line conditioners system

The shunt active power line conditioning system contains a cascaded multilevel inverter based active filter, RL-filters, a compensation controller (unit-current vector in conjunction with PI or PID or fuzzy logic controller) and switching signal generator (proposed triangular-sampling current controller) as shown in the Fig 1. The three phase supply source connected to the non-linear load (such as diode rectifier RL load). This nonlinear load current will have fundamental and harmonic current components, which can be represented as [26-27]

$$i_L(t) = \sum_{n=1}^{\infty} I_n \sin(n\omega t + \Phi_n) = I_1 \sin(\omega t + \Phi_1) + \left(\sum_{n=2}^{\infty} I_n \sin(n\omega t + \Phi_n) \right) \quad (1)$$

The instantaneous load power can be multiplied from the source voltage and current and the calculation is given as

$$p_L(t) = i_s(t) * v_s(t) = V_m \sin^2 \omega t * \cos \phi_1 + V_m I_1 \sin \omega t * \cos \omega t * \sin \phi_1 + V_m \sin \omega t * \left(\sum_{n=2}^{\infty} I_n \sin(n\omega t + \Phi_n) \right) = p_f(t) + p_r(t) + p_h(t) \quad (2)$$

This load power contains fundamental or real power $p_f(t)$, reactive power $p_r(t)$ and harmonics power $p_h(t)$. From equation (2) only the active (fundamental) power drawn by the load is

$$p_f(t) = V_m I_1 \sin^2 \omega t * \cos \phi_1 = v_s(t) * i_s(t) \quad (3)$$

From this equation, the source current drawn from the mains after compensation should be sinusoidal; this is represented as

$$i_s(t) = p_f(t) / v_s(t) = I_1 \cos \phi_1 \sin \omega t = I_{max} \sin \omega t \quad (4)$$

If the active power filter provides the total reactive and harmonic power, source current $i_s(t)$ will be in phase with the utility voltage and would be sinusoidal. At this time, the active filter must provide the compensation current:

$$i_c(t) = i_L(t) - i_s(t) \quad (5)$$

Therefore, the active power filter extracts the fundamental component of the load current; that can

be used for compensating the harmonic current and reactive power simultaneously. The source currents after compensation can be written as

$$i_{sa}^* = I_{max} \sin \omega t \tag{6}$$

$$i_{sb}^* = I_{max} \sin(\omega t - 120^0) \tag{7}$$

$$i_{sc}^* = I_{max} \sin(\omega t + 120^0) \tag{8}$$

This peak value of the reference current I_{max} has been estimated by regulating the DC-bus capacitor voltage of the cascaded inverter using PI or PID or fuzzy logic controller.

2.1. Power Converter

A cascaded multilevel inverter based active power inverter is constructed by the conventional of H-bridges. This cascaded active filter has been applied for power quality applications due to increase the number of voltage levels, low switching losses and higher order of harmonic elimination [33-35]. The three phase active filter comprises of 24-power transistors and each phase consists of two-H-bridges in cascaded method for 5-level output voltage [21-22], shown in Fig 2. Each H-bridge is connected a separate dc-bus capacitor and it serves as an energy storage elements to supply a real power difference between load and source during the transient period. The dc-bus capacitor voltage is maintained constant using proposed low pass filter conjunction with PI or PID or fuzzy logic controller.

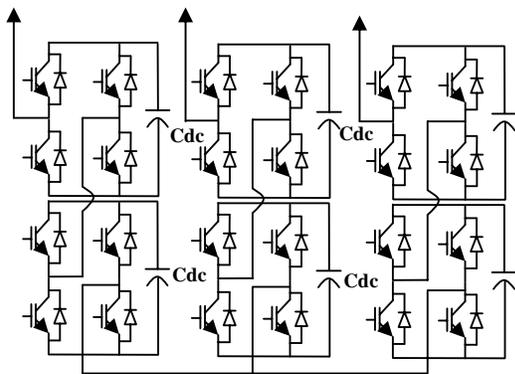


Fig 2 Design of cascaded multilevel VSI

The 24-IGBT switching operations are performed using proposed triangular sampling current controller; it has the highest rate for cascaded inverters. The current harmonics compensation is achieved by injecting equal but opposite current harmonic components at PCC.

3 Proposed Control Strategy

The block diagram of the proposed control system is shown in Fig 3. It consists of two parts; one is reference current generator and another is switching patterns generator. The reference current generates using unit-current vector output multiplies with estimated peak current by PI or PID or fuzzy logic control strategy. The cascaded multiple inverter switching patterns are generates using proposed triangular-sampling current controller. This section explains these control methodologies.

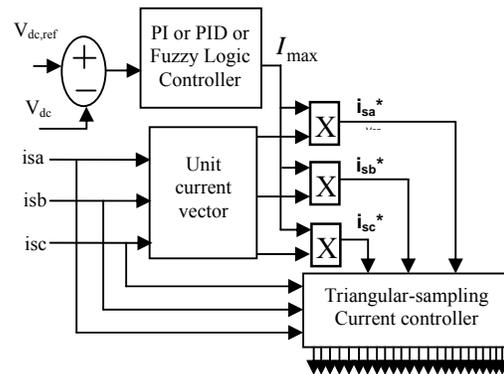


Fig 3 Block diagram of the proposed controller

3. 1. Unit-current Vector

The source currents are sensed from the supply grid and converted to the unit sine current(s) while corresponding phase angles are maintained. The unit-current vectors templates is represented as

$$\begin{aligned} i_a &= \sin \omega t, \\ i_b &= \sin(\omega t - 120^0), \\ i_c &= \sin(\omega t + 120^0) \end{aligned} \tag{9}$$

The amplitude of the sine current is unity in steady state and in the transient condition it may increase or decrease according to the loads; the frequency is in phase with the source voltages. This unit-current multiplies with peak value of estimated reference current by PI or PID or FLC to generate the desired reference currents.

3.2. PI-Controller

Fig 4 shows the block diagram of the Proportional Integral (PI) control scheme for the active power filter. The DC-bus capacitor voltage is sensed and compared with a reference voltage and also

calculating the error signal. The error signal $e = V_{dc,ref} - V_{dc}$ at the n^{th} sampling instant is used as input for PI-controller. The error signal passes through first order Butterworth design based Low Pass Filter (LPF) that suppresses higher frequency components and allows fundamental components only. The proportional and integral gains are estimates the magnitude of peak reference current I_{max} and control the dc-bus capacitor voltage of the inverter. Its transfer function is

$$H(s) = K_p + \frac{K_I}{s} \tag{10}$$

Where, $[K_p=0.7]$ is the proportional constant that determines the dynamic response of the DC-bus voltage control and $[K_I=23]$ is the integration constant that determines the settling time. This PI-controller is eliminating the steady state error in the DC-bus voltage of the cascaded multilevel voltage source inverter.

3.3 PID Controller

Fig 4 shows the block diagram of the Proportional Integrator Derivative (PID) control scheme of an active power filter. The error $e = V_{dc,ref} - V_{dc}$ at the n^{th} sampling instant is used as input for PID controller. The error signal passes through first order Butterworth design based LPF that suppresses higher frequency components and passing fundamental frequency components only.

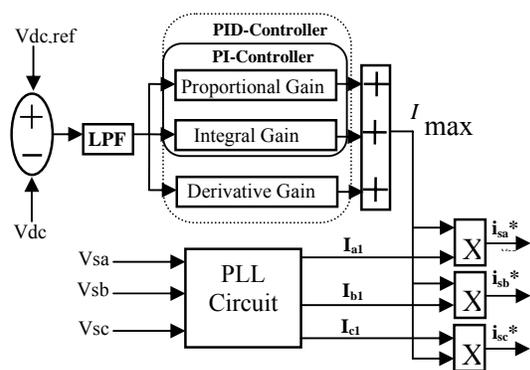


Fig 4 block diagram of the PI and PID Controller

The PID-controller is a linear combination of the P, I and D gain of the numerical values. Its transfer function can be represented as

$$H(s) = K_p + \frac{K_I}{s} + K_D(s) \tag{11}$$

Where, K_p is the proportional constant that determines the dynamic response of the DC-bus voltage control and K_I is the integration constant that determines the settling time and also the K_D is the derivative of the error representing the trends. The controller is tuned with proper gain parameters $[K_p=0.7, K_I=23, K_D=0.01]$ for estimate the magnitude of peak reference current I_{max} and control the DC-bus capacitor voltage of cascaded inverter. This peak reference current I_{max} multiplied with unit-current vector output and that determines the required reference current.

3.4. Fuzzy Logic Controller (FLC)

Fuzzy logic control is derived from fuzzy set theory introduced by Zadeh in 1965. In fuzzy logic concept, the transition is derived between membership and non-membership functions. Therefore, boundaries of fuzzy sets can be undefined and ambiguous, making it useful for approximate systems. FLC is an attractive choice when precise mathematical formulations are impossible to utilize.

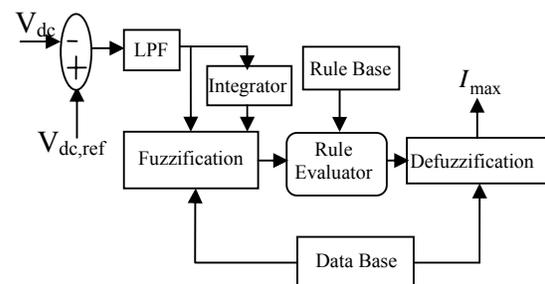


Fig 5 block diagram of Fuzzy logic controller

In order to implement the fuzzy logic control algorithm of an active power filter in a closed loop, the DC-bus capacitor voltage is sensed and then compared with the desired reference value. The compared error signal ($e = V_{DC,ref} - V_{DC}$) allows only the fundamental component using the Butterworth 50 Hz low pass filter. The error signal $e(n)$ and integration of error signal or change of error signal $ce(n)$ are used as inputs for fuzzy processing shown in Fig 5. The output of the fuzzy controller after a limit is considered as the magnitude of peak

reference current I_{max} . This reference current takes care of the active power demand of the non-linear load for harmonics and reactive power compensation.

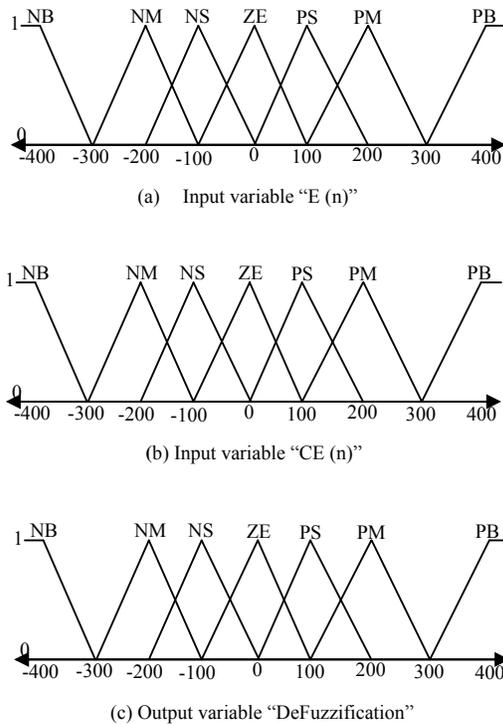


Fig 6 FLC membership functions (a) the input variables error $e(n)$ (b) change of error $ce(n)$ and (c) output variable defuzzification

The proposed fuzzy logic controller characteristics are; (1) Seven fuzzy sets for each input and output variables. (2) Triangular membership function is used for simplicity. (3) Implication using mamdani-type min operator. (4) Defuzzification using the height method. The linguistic control rules are derived from the triangular membership function that is shown in Fig 6.

Fuzzification:

Fuzzy logic uses linguistic variables instead of numerical variables. In a control system, error between reference signal and output signal can be assigned as Negative Big (NB), Negative Medium (NM), Negative Small (NS), Zero (ZE), Positive small (PS), Positive Medium (PM), Positive Big (PB). The triangular membership function is used for fuzzifications. The process of fuzzification convert numerical variable (real number) to a linguistic variable (fuzzy number).

Rule Elevator:

Conventional controllers like PI and PID have control gains which are numerical values. Fuzzy logic controller uses linguistic variables instead of the numerical values. The linguistic variables of error signal $e(n)$ change of error signal $ce(n)$ and output I_{max} represents degree of membership functions. The basic fuzzy set operations needed for evaluation of rules are AND(\cap), OR(\cup) and NOT($-$)

AND -Intersection: $\mu_{A \cap B} = \min[\mu_A(X), \mu_B(x)]$

OR -Union: $\mu_{A \cup B} = \max[\mu_A(X), \mu_B(x)]$

NOT -Complement: $\mu_A = 1 - \mu_A(x)$

Defuzzification:

The rules of fuzzy logic generate demanded output in a linguistic variable, according to real world requirements, linguistic variables have to be transformed to crisp output (Real number). The choices available for defuzzification are numerous. So far the choice of strategy is a compromise between accuracy and computational intensity

Database:

The Database stores the definition of the membership function involved by fuzzifier and defuzzifier. Storage arrangement is a compromise between available memory and microprocessor stages of the digital controller chip.

Rule Base:

The Rule base stores the linguistic control rules required by rule evaluator (decision making logic). The rules used in this paper are shown in Table 1.

Table 1 Rule base table

$ce(n) \backslash e(n)$	NB	NM	NS	ZE	PS	PM	PB
NB	NB	NB	NB	NB	NM	NS	ZE
NM	NB	NB	NB	NM	NS	ZE	PS
NS	NB	NB	MN	NS	ZE	PS	PM
ZE	NB	NM	NS	ZE	PS	PM	PB
PS	NM	NS	ZE	PS	PM	PB	PB
PM	NS	ZE	PS	PM	PB	PB	PB
PB	ZE	PS	PM	PB	PB	PB	PB

The FLC is estimated the magnitude of peak reference current I_{max} , that current takes response of the active power demand of the non-linear load and losses in the distribution system. The peak reference current multiply with output of unit-current vector and has determined the reference current.

3.5. Triangular-sampling current controller

The proposed triangular-sampling current controller for active power filter line currents can be executed to generate the switching pattern of the cascaded voltage source inverter. There are various current control methods proposed; but the triangular-sampling current control method has the highest rate for cascaded active power filters. These inverters features are quick current controllability, the switching operation induced the suppression of the harmonics, the average switching frequency of each inverter is equality and unconditioned stability. The PI or PID or fuzzy logic controller is estimates the magnitude of peak reference current I_{max} and that current multiples with unit-current vector to determine the reference currents ($i_{sa}^*, i_{sb}^*, i_{sc}^*$). This reference current compares with actual source currents (i_{sa}, i_{sb}, i_{sc}) using the proposed current controller method to generate the switching signals. The five-level cascaded voltage source inverter systems of the current controller are utilized independently for each phase. Each current controller directly generates the switching signal of the three A, B, C phases. The A-phase actual source current (i_{sa}) and reference current (i_{sa}^*) as shown in Fig 7 similarly derived the B and C phase currents.

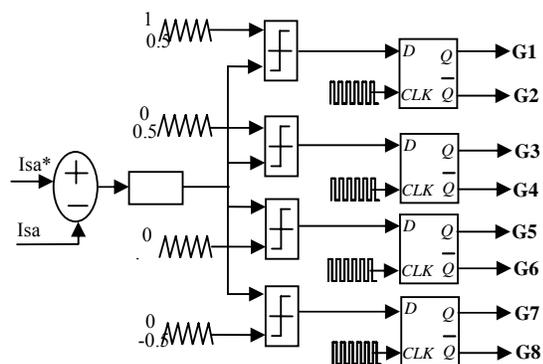


Fig 7 Triangular-sampling current controller

To determine the switching frequency by means the error current [desired reference current compare with the actual source current] multiplied the proportional gain (K_p) and compared with triangular-sampling signal. The four triangular signals are generated same frequency with different amplitude for cascaded inverter. Thus the switching frequency of the power transistor is equal to the frequency of the triangular-sampling signal. Then,

the output signal of the comparator is sampled and held D-Latch at a regular interval T_s synchronized with the clock of frequency equal to $1/T_s$. Note that 4-external clock applied to each converter and T_s is set as 30 ns, because each phase in one converter does not overlap other phase. Therefore the harmonic currents are reduced as if the switching frequency were increased.

4 Simulation Result and Analysis

The performance of the proposed PI, PID and fuzzy logic control based cascaded active power filter is evaluated through Matlab/Simulink power tools. The system is modelled and validated under steady state and transient conditions with different non-linear loads. The system parameters values are consider as in Table 2.

Table 2 system parameters

Parameters	Values
Line to line source voltage (V_m)	440 V
System frequency (f)	50 Hz
Source impedance: Source resistor (R_s)	0.1 Ω
Source inductor (L_s)	0.5 mH
Non-Linear Load: Diode rectifier	6-diode
Load resistor (R_L)	20 Ω
Load inductor (L_L)	100 mH
Filter: Inductor (L_F)	1 mH
Resistor (R_F)	1 Ω
Dc-bus capacitance (C_{DC})	2100 μ F
Reference voltage ($V_{DC,ref}$)	150 V
Power Converter	24-IGBTs/diode

Case1: PI-Controller

The diode rectifier RL load connected the ac main grid and cascaded active filter joint in parallel at the PCC for inject the current harmonics and reactive power. The simulation result of the six-pulse rectifier load current or source current before compensation is shown in Fig 8 (a); it contain fundamental and harmonic components. The triangular-sampling current controller generates the required gate switching pulses to operate the cascaded inverter. These cascaded active filter provides the harmonic filter current or compensation current that is shown in Fig 8(b). The source current after compensation is presented in Fig 8(c) that indicates the current is sinusoidal.

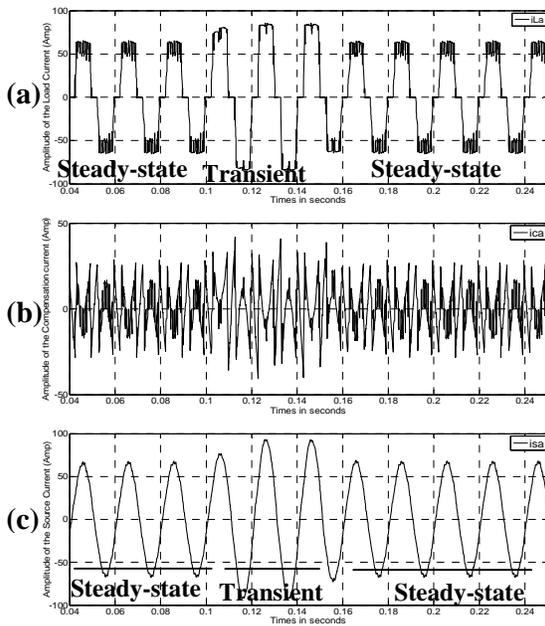


Fig 8 Simulation result for PI-controller based cascaded active filter (a) source currents before compensation or load current (b) Compensation current (c) Source current after active filter

Case2: PID-Controller

PID controlled cascaded inverter based active power filter is modelled and validated; simulation waveforms are verified similarly PI-controller. The three phase diode rectifier RL load current is shown in Fig 9 (a). The cascaded active filter provides compensation current for compensating the current harmonics by injecting equal but opposite harmonic currents at the point of common coupling. After compensation the distorted source current is becomes sinusoidal that is presented in Fig 9(b). These figures are focused in A-phase only other phases is just phase shifted by 120^0

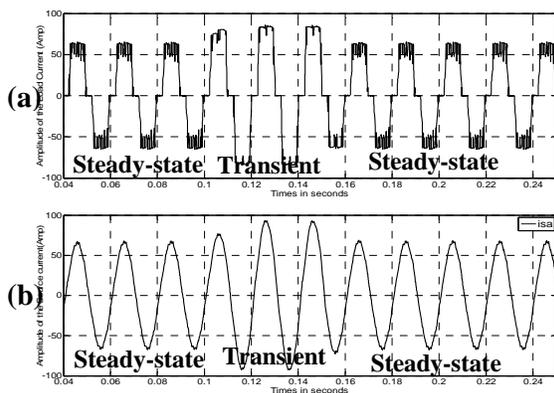
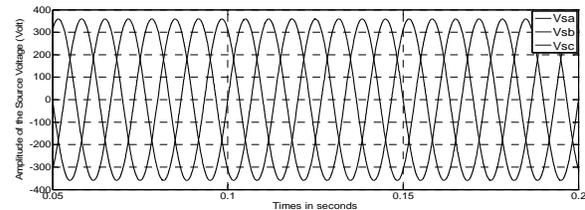


Fig 9(a) load current (b) Source current

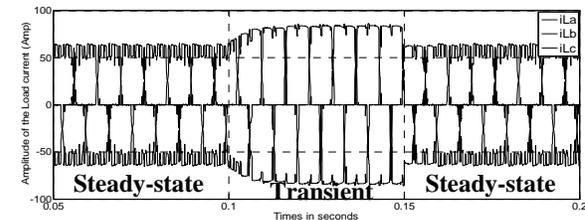
Case3: Fuzzy Logic-Controller

The proposed fuzzy logic controlled cascaded multilevel inverter based active power filter system is modelled and tested. The diode rectifier load connected the ac main and the cascaded active filter connected in parallel at the PCC for injecting the current harmonics and the reactive power. The Fig 10(a) shows simulation of the 3-phase balanced supply voltage.



3(a) source currents before compensation

This simulation result of the six-pulse diode rectifier load current or source current before compensation is shown in Fig 10 (b).



10(b) source currents before compensation

The DC-bus capacitor voltage is sensed and compared with a reference voltage; that compared error current is used as input for fuzzy logic controller. The FLC control the dc-bus capacitor voltage and estimate the magnitude of peak reference current. The peak reference current multiplied with unit-current vector current and determined the reference current, that is shown in Fig 10 (c).

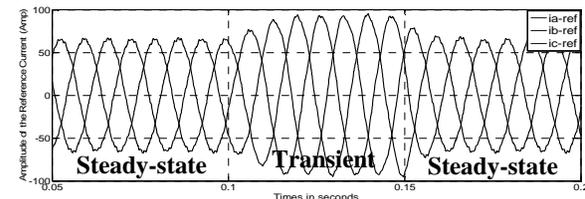
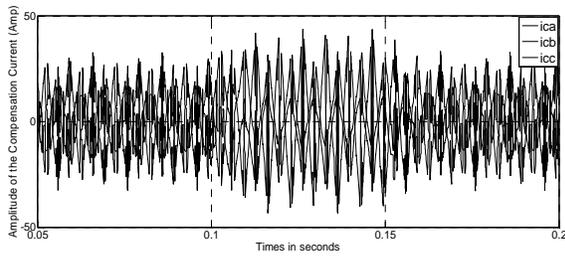


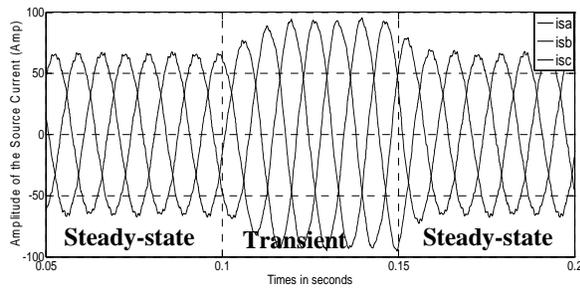
Fig 10 (c) references current

The active filter must provide the harmonic filter current or compensation current as $i_c(t) = i_L(t) - i_s(t)$ that is shown in Fig 10(d).



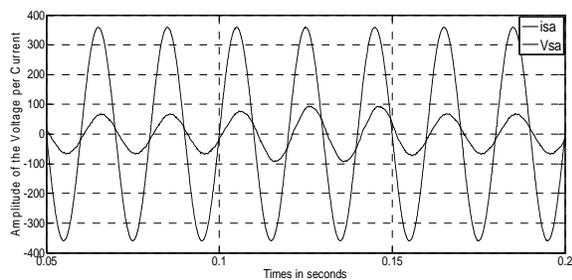
10 (d) Compensation current

Consequently current harmonics is achieved by injecting equal but opposite harmonic components at the PCC, there by cancelling the original distortion and improving the power quality on the connected power distributed system. The simulation result of source current after compensation is presented in Fig 10(e) that indicates the current is sinusoidal.



10 (e) Source current after active filter

The proposed APF system is achieved power factor correction that is shown in Fig 10(f). From the simulation we can realise a-phase voltage is in-phase with a-phase current.



10 (f) unit-power factors

The DC-bus capacitors voltage of the cascaded multilevel inverter is controlled by fuzzy logic controller. The fuzzy logic controller maintains the capacitors voltage with small ripple in steady and dynamic conditions that is shown in Fig 10(g); it serves as an energy storage element to supply a real power to operate three-phase cascaded voltage source inverter.

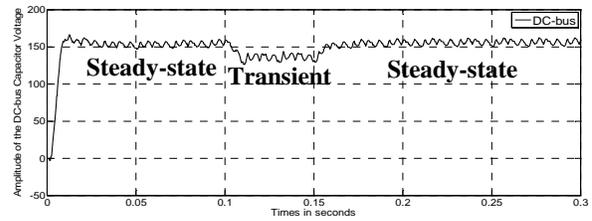


Fig 10 (g) DC-bus capacitor voltages

The Fast Fourier Transform (FFT) is used to measures the order of harmonics with the fundamental frequency 50 Hz at the source current. This order of the harmonics plotted using PI, PID and fuzzy logic-controller based cascaded active power filter systems in the supply current. The Fig 11 is plotter under FLC controller based cascaded active power system in steady state conditions.

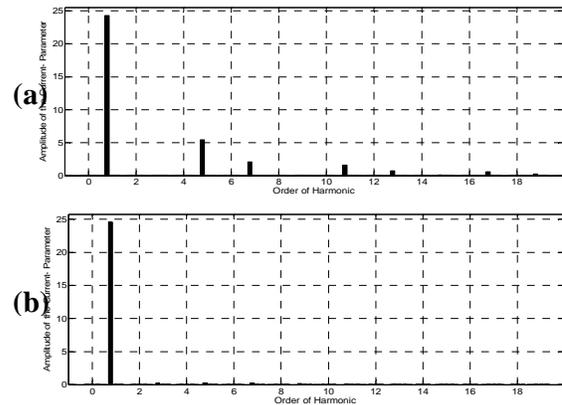


Fig 11 Order of harmonics (a) the source current without active filter (THD=25.38 %), (d)FLC based cascaded APF(THD=2.53 %)

The total harmonic distortion (THD) measured from the source current on the distribution side. The PI, PID and fuzzy logic controller based cascaded compensator filter made linear source current to the supply. The total harmonic distortion measured and compared that is presented in Table 2.

Table 2 THD measured without APF and with APF

THD conditions	Source Current(I _s) without APF	Source Current(I _s) with APF		
		PI controller	PID controller	Fuzzy logic controller
Steady state	25.38%	2.61%	2.58%	2.53%
Transient	25.32%	2.59%	2.59%	2.48%
Power factor	0.8772	0.9733	0.9721	0.9829

The simulation is done various non-linear load conditions. The PI or PID or fuzzy logic control based compensating cascaded active filter made balance responsibility even the system is non-linear load. FFT analysis of the active power filter brings the THD of the source current less than 5% into adopted with IEEE 519-1992 and IEC 61000-3 standards under non-linear load conditions.

5 Conclusions

This paper has been shown that the cascade multilevel inverter based active filter is suitable for power line conditioning in the power distribution network. The cascaded inverter provides lower costs, higher performance and higher efficiency than the traditional PWM-inverter for power line conditioning applications. A low pass filter conjunction with PI or PID or fuzzy logic control schemes has been presented for controlling the DC side capacitor voltage of the cascaded inverter and estimate the required peak reference current. The proposed PI, PID and fuzzy logic controller based APLC system is validated through extensive simulation and compared under steady state and transient condition with different non-linear loads. These simulation results reveal that the cascaded active power filter effectively filtered the current harmonics and compensated reactive volt amperes power. A comparative assessment of these three different controllers is done. The measured total harmonic distortion of the source currents is compliance with IEEE 519-1992 and IEC 61000-3 harmonic standards.

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