Sensitivity of Compact Fluorescent Lamps during Voltage Sags: An Experimental Investigation

HUSSAIN SHAREEF, AZAH MOHAMED, KHODIJAH MOHAMED
Department of Electrical, Electronic and Systems Engineering
Universiti Kebangsaan Malaysia
Faculty of Engineering and Built Environment, Bangi, 43600, Selangor
MALAYSIA
shareef@eng.ukm.my, azah@eng.ukm.my, khodjah_muhd@yahoo.com

Abstract: - The aim of this paper is to analyze the sensitivity of various compact fluorescent lamps (CFLs) which are used in residential and commercial applications during voltage sags. Laboratory tests were performed on different CFLs commonly available in the market. The tests are based on recent testing standards and utilizing a modern industrial power corruptor. For predefined malfunction criterion of zero illuminance condition, sag depth and duration are varied to construct individual voltage immunity curves. Experimental results show that all CFLs are sensitive to voltage sags and vary in a wide range. It also proves that some brands of CFLs having similar power rating are sensitive to both sag magnitudes and its duration. Finally a method to improve the sensitivity of CFLs to voltage sags is implemented. This technique increases the holdup time of the dc bus voltage by connecting additional dc capacitance at the rectifier output of the CFL's ballast circuit.

Key-Words: - Voltage sag, ride through capability, ballast, CFL, voltage tolerance curves

1 Introduction

Compact fluorescent lamps (CFLs) have recently emerged as cost-competitive, energy efficient alternatives to replace conventional incandescent lamps in their existing fittings. Recently, power companies and government have been encouraging the use of CFLs due to its energy efficiency. The use of CFLs is expected to save up to 10% of a household's electricity usage. Beside from energy efficiency, CFLs are susceptible to power system disturbances such as voltage sag. During sag, the voltage suffers a sudden reduction of voltage between 10-90% of the nominal voltage that lasts between 10 milliseconds and 1 minute [1]. Voltage sag may cause lamps to extinguish or flicker that will likely to cause nuisance and damage in some cases. However, there is a little available information related to the sensitivity of CFLs due to voltage sags or temporary outages.

A number of studies on CFLs have concentrated on the internal electronic ballast design to enhance their performance [2]-[5]. Several researchers have performed direct harmonic simulation as well as field experiments to investigate the possible effects of CFL harmonics on local distribution network [6]-[13]. Some literature discusses flicker generation in CFLs mainly due to fluctuations in their supply voltage [14]-[16]. Moreover, there are few works on the sensitivity of CFLs in the presence of power system disturbances such as interharmonics and phase jumps which are not normally associated with flicker [17].

The extensive use of CFLs with electronic ballasts demands a comprehensive analysis, including not only their effects on harmonic emissions and flicker sensitivity, but also their performance during the other power quality problems such as voltage sags in electric distribution systems. To the best of the author's knowledge, such an analysis has not yet been presented for CFLs. A few contributions have focused on the effect of voltage sag on other types of lamps namely, high pressure sodium lamps, metal halide lamps, and conventional fluorescent lamps [18]-[21].

In this paper, after a brief introduction about the operation of compact fluorescent lamps, laboratory tests are performed on various CFLs. It is based on recent testing standards and modern testing equipment. These tests are carried out to observe the light intensity variation of the CFLs during voltage sags. Moreover, to evaluate the voltage tolerance levels of the tested CFLs for the identified zero illuminance failure condition, the test results are also compared with the design goals of ITIC and SEMI F47 standards from Information Technology Industry Council and Semiconductor Equipment and Materials International respectively. In addition, a method is implemented to improve the sensitivity of the electronically ballasted FLs to voltage sags.

2 Compact Fluorescent Lamp Operation

The operating principle of CFLs is the same whether the form is circular or convoluted as in compact fixtures.

When a voltage is applied across the ends of a sealed glass tube containing mercury vapor, it causes the vapor to ionize. This vapor radiates light in the ultra violet region of the spectrum, which is converted to visible light by a fluorescent coating on the inside of the lamp. However, it requires a high voltage pulse across the tube to start the process and some form of limiter to prevent the current increasing to a level where the lamp can be destroyed. The current limiter used in CFLs is commonly known as electronic ballast. Electronic ballasts replace the starting and bulk inductive elements of the conventional electromagnetic ballasts. The electronic ballast improves the performance of the lamp by operating at a higher frequency above the 50Hz determined by the mains supply. This eliminates lamp flickering because the gas in the tube does not have time to de-ionize between current cycles which also leads to lower power consumption, and longer tube life. Moreover, since the inductor required to ionize the tube is smaller, resistive loss and the system size is reduced [22]. Fig. 1 depicts a block diagram of typical low-wattage electronic ballast. The first block contains the protection, filtering and current peak limiting components. Block 2 is the full diode bridge rectifier to convert the ac line into a dc stage. Block 3 is the smoothing capacitor. It provides the dc link voltage of the resonant inverter for the tube in Block 4.

Under normal operating conditions, over a half-cycle, the capacitor voltage decays to a value given by [23]:

$$\Delta V = \frac{I_0 T_{50}}{2C_{dc}} \qquad (1)$$

where

ΔV is the capacitor voltage decay
I_0 is the load current
T_{50} is the 50-cycle period
C_{dc} is the capacitance of the filter capacitor

Therefore the capacitor is essentially charged close to the peak of the ac mains peak voltage plus $\Delta V/2$ which is ideal for the resonant inverter circuit to operate efficiently. However, during the event of voltage sag of N cycles, the dc link capacitor discharges to $2N\Delta V$. Depending upon the minimum voltage value set by the design of the ballast, the resonant inverter will deliver sufficient amount of current and voltage to the lamp until the capacitor voltage reaches the designed minimum operating value of the resonant inverter. The time to reach this voltage at rated load is defined as the holdup time, T_h, which is represented mathematically as [24]:

$$T_h = \frac{C_{dc}\left(V_{norm}^2 - V_{\min}^2\right)}{2P} \qquad (2)$$

where

C_{dc} is the capacitance of the filter capacitor
V_{norm} is the peak nominal voltage
V_{min} is the peak minimum voltage set by the ballast design
P is the rated power of the lamp

Since the rated load powers are low, the directives governing the injection of harmonics are not particularly strict [6], and therefore power factor control circuits are not generally included in low-wattage CFLs' electronic ballasts. The diac is for starting the resonant inverter. The resonant inverter normally runs at 10-40 kHz. The most commonly used resonant inverter circuits for low-wattage CFLs are voltage fed half-bridge quasi-resonant circuits and current fed half-bridge resonant circuits [22].

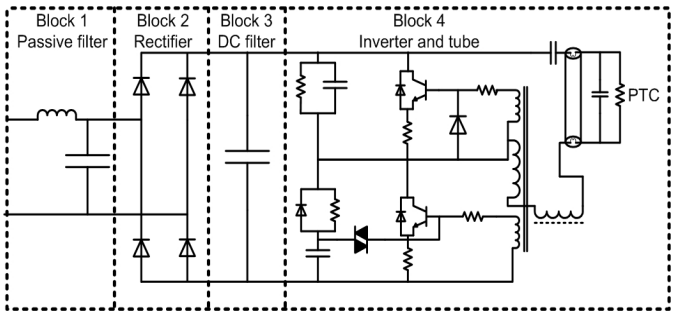


Fig.1: Block diagram of an electronic ballast

3 Lamp Testing

This section illustrates the design of the experiment for CFL testing and the procedures followed to obtain the results on the performance of CFLs during voltage sags.

3.1 Experimental Setup

The methodology that is used in the testing is generally based on the guideline published in the IEC Standard 61000-4-11 [1]. Four 8 Watt CFLs from different manufacturers and three CFLs with various power ratings from the same manufacturer are tested to study the effect of voltage sags on the performance of the lamps. The specifications of the tested CFLs are shown in Table 1.

The experimental set up consists of five components namely, sag generator, light meter, equipment under test (EUT), data acquisition system, and a personal computer to analyze the signals. In this case, an industrial power corruptor (IPC) from the Power Standards Lab is used. It is a voltage sag generator combined with built-in data

acquisition system that is capable of producing and interrupting voltages up to 480V and current at 50A in single or three phase systems. Since the main objective of this study is to detect and determine light output variations of the CFLs during voltage sags, it is important that the design of the test system must be fast enough to capture the light intensity variation of the test lamps accurately.

Table 1: Technical Data for Tested CFLs

Manufacturer and type	Rated voltage	Rated Power	Rated current	Rated light flow & light color	Rated Life Span
GE Edison Tiny FLE8HX E27	220-240 V, 50-60 Hz	8 W	65 mA	430 lm, 6500K	6000 h
Hitachi, EFH8E E27	220-240 V, 50-60 Hz	8 W	60 mA	-	4 years, 4h/day
Osram, DULUXSTAR COMPACT 8W/865	220-240 V, 50-60 Hz	8W	71mA	400lm	6000 h
Philips Genie 8W ES E27	220-240 V, 50-60 Hz	8 W	60 mA	415 lm, 6500K	3 years, 5.5h/ day
Philips Genie 14W ES E27	220-240 V, 50-60 Hz	14 W	100mA	790 lm, 6500K	3 years
Philips Essential 23W ES E27	220-240 V, 50-60 Hz	23 W	165mA	1420 lm	3 years, 5.5h/ day

The test system shown in Fig. 2 has been built to perform the voltage sag disturbances and evaluate the resultant light output levels from the lighting source. The lamp under test is enclosed in a prefabricated lighting chamber which eliminates stray light and reduces reflections by its internal matt black surface. This point source method measures the light directly produced by the lamp with a light detector at the opposite end of the chamber. The detector head photocurrent is converted to a voltage and it is more than capable of detecting flicker in the human visible range of 0-35Hz [17]. The conversion process of light detector current into an appropriate level of voltage is performed by the processor in the photometer. However, since the photometer does not have its own built in data acquisition system, the converted voltage waveform is therefore fed to the data acquisition system channels available in the IPC for post processing and analysis.

3.2 Testing Procedure

A series of test results on CFLs is obtained by following the pre-defined procedure given below.

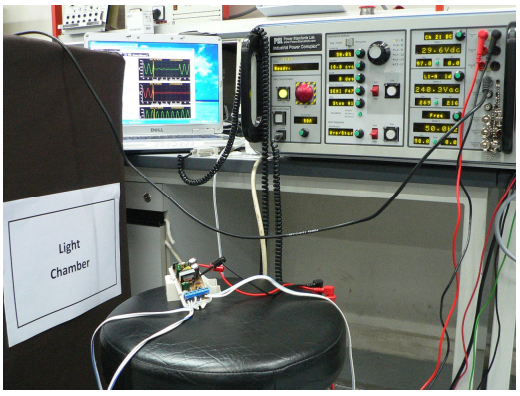
1) Using the terminal blocks available at the back of IPC, the conductors from mains panel and conductors to the CFL under test are connected and the IPC is powered on.

2) The CFL is switched on and allowed to reach its full brightness. Steady state condition in the light output can be assured by observing the illuminance meter reading.

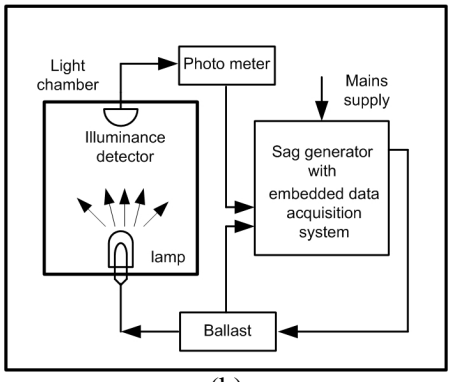
3) Starting from nominal voltage, voltage sags are initiated in steps of 2.5% down to zero volts. The sag initiation angle and the duration are kept constant. The initial sag duration and phase angle are set to 1 cycle and 0° respectively. The critical sag depth for the pre-defined zero illuminance malfunction criteria is determined by repeated testing for at least 3 times for a particular sag magnitude and duration. If a malfunction condition is observed, a quick inspection for proper operation of CFL is conducted before initiating the next sag. For each triggered sag event, the different voltage and current waveforms supplied to the CFL are recorded along with real time light output measurements. Observations such as visible or audible influence on the CFL are also noted.

4) The duration of sag is adjusted in steps of 1 cycle and the measurements outlined in step 3 are repeated.

A flowchart of the aforementioned procedure is shown in Fig. 3.



(a)



(b)

Fig.2: Experimental setup (a) actual (b) schematic

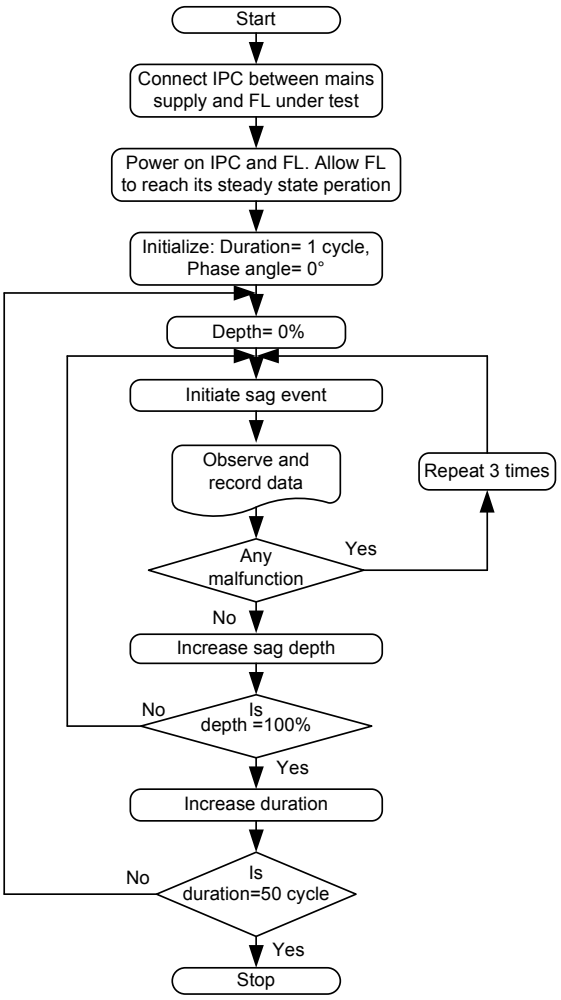


Fig.3: CFL testing procedure

4 Results and Analysis

Numerous test results are analyzed and discussed in this section. First the effect of voltage sag on individual lamps is analyzed. As each CFL potentially has its own standard of voltage acceptability, individual voltage immunity curves are plotted and compared with the ITIC and SEMI F47 standards.

4.1 Analysis of 8 Watt CFLs

In order to understand the sensitivity of similar wattage CFLs from different manufactures to voltage sags, signals obtained from the photometer, dc bus, supply voltage and current are analyzed.

4.1.1 GE Edison's CFL

Fig. 4 illustrates the waveforms obtained from the photometer and supply voltage for the GE Edison's lamp. It shows the effect of varying the sag depth starting from 37.5% to 32.5% remaining voltage for 2 cycles, on light output variation of the lamp. The lamp turn off condition starts to occur for sag having 35% remaining voltage at 2 cycles. Furthermore, for different depths of voltage sags, the decay time of light output variation remains almost the same between 0 ms and 20 ms. It also shows the amount light radiation from the lamp does not reach zero illuminance level in one cycle although the lamp is turned off condition is observed for 2 cycles.

In order to observe the effect of voltage sag duration, waveforms of light output variation at constant sag magnitude are observed. Fig. 5a illustrates the performance of the GE Edison's CFL, when the duration of sag having 37.5% remaining voltage is varied from 1 to 10 cycles just before the lamp starts to malfunction. A careful observation on Fig. 5a reveals that the minimum light output that appears across the tube does not drop completely to zero illuminance level but reverts back to the normal brightness as soon as the supply voltage is stabilized. Note that the sag duration does not have an effect in the rate of decay of light output during the sag as each plot takes almost the same data points during the sag. A similar observation is found for the effect of varying the voltage sag duration at 35% remaining voltage as shown in Fig. 5b. However, it can be seen from Fig. 5b that, starting from 2 cycles, the lamp always turn off completely.

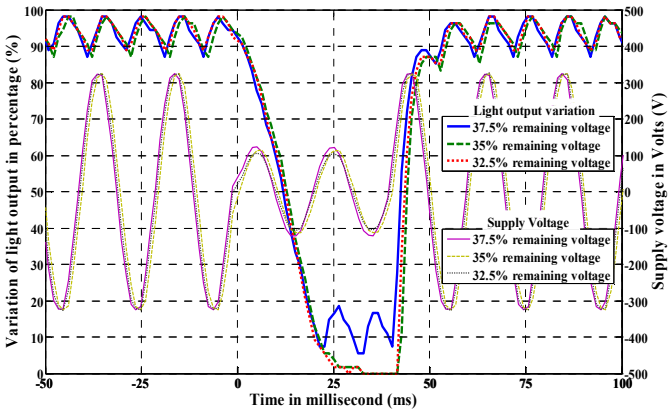
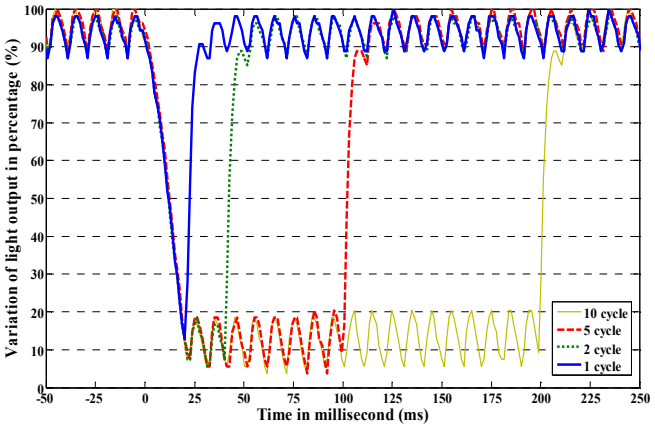
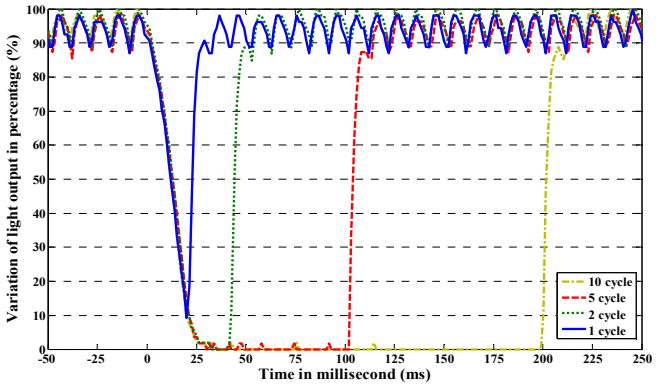


Fig.4: Effect of sag depth on the light output at 2 cycles for GE Edison's CFL



(a)



(b)

Fig.5: Effect of sag duration on the light output for GE's CFL. (a) at 37.5% remaining voltage (b) at 35% remaining voltage

4.1.2 Philips's CFL

The second CFL that is tested for sensitivity to voltage sag is a Philips's CFL. Similar to the GE Edison's CFL, this lamp also experienced zero illuminace condition due to voltage sag disturbances. Fig. 6 shows the variation in light output where it first starts to malfunction for voltage sag lasting for 2 cycles. From Fig. 6, it can be clearly seen that the Philip's CFL is much more immune to voltage sag depth when compared to the GE Edison's CFL. Observe that this CFL just reaches zero illuminance malfunction condition at a sag depth of 22.5% remaining voltage nearly around 30 ms.

Analysis conducted to observe the effect of variation of sag duration on the performance of the lamp at sag depth of 25% remaining voltage, shows that the light output variation does not completely drop down to zero even if the sag duration is varied between 1 to 50 cycles and therefore the lamp is considered to operate properly. However, when the sag depth is increased to 22.5% remaining voltage the lamp starts to extinguish for any sag duration starting from 2 cycles. Therefore, it can be concluded that CFLs from GE Edison and Philips have similar characteristics although the Philips CFL is more immune to sag magnitude.

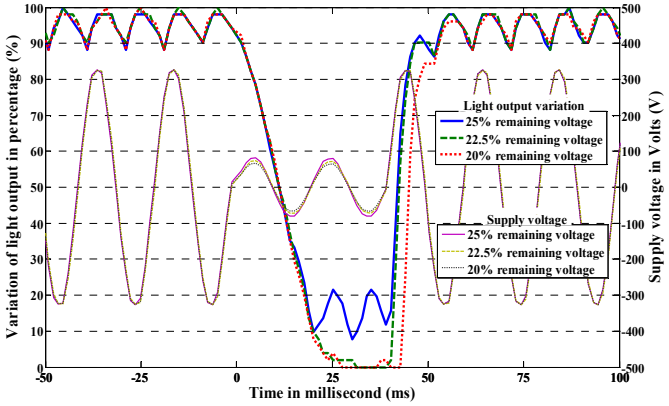


Fig.6: Effect of sag depth on the light output at 2 cycles for Philip's CFL

4.1.3 Osram's CFL

A similar analysis is conducted with CFL from Osram having same power rating of 8 Watt. It is found that this CFL is much more sensitive to voltage sags than that of the CFL presented before. In this case, the knee points appear at 12.5% and 30% remaining voltage for one cycle and two cycles, respectively. Fig. 7 shows the light output variation for different depths of voltage sag that last for 1 cycle. Observe that when the sag depth is 12.5% remaining voltage the CFL starts to malfunction just around 20 ms while in case of longer sags that last for more than 2 cycles this CFL seems to extinguish at 30% remaining voltage. The effect of sag duration at 30% remaining voltage for Osram's CFL is shown in Fig. 8. It can be seen from Fig. 8 that for sag duration of 20 ms, the light output does not decrease to zero illiminance level as observed for deeper sag shown in Fig. 7.

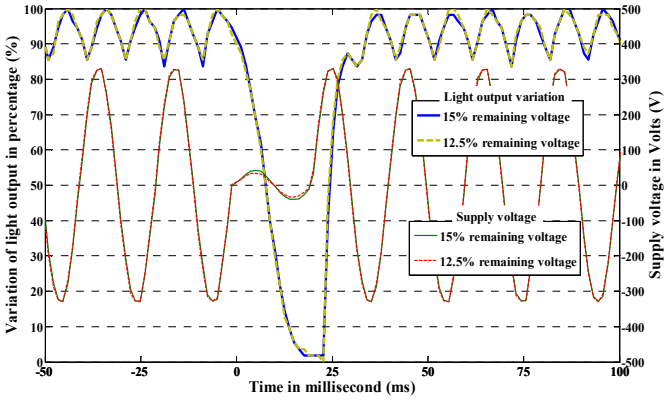


Fig.7: Effect of sag depth on the light output at 1 cycle for Osram's CFL

4.1.4 Hitachi's CFL

The last 8 Watt CFL tested is a Hitachi CFL. Like the Osram's lamp, this CFL is also sensitive to both sag depth and duration. In this case, the knee points appear at 22.5%, 25% and 27.5% remaining voltage for 2 cycles, 5 cycles and 30 cycles, respectively. From this analysis it can be concluded that the CFLs from Osram and Hitachi are sensitive to both voltage sag magnitude duration.

The overall immunity level of the tested 8 Watt CFLs to voltage sags are presented in Fig. 9 as typical voltage tolerance curves along with the SEMI F47 and ITIC voltage acceptability standard.

The upper region of these curves represents proper operation region while the lower region indicates zero illuminance conditions for CFLs' operation. From Fig. 9, the lamp from Osram is found to be the most sensitive 8 Watt CFL selected for the testing in terms of sag duration. The lamp turn off condition is initiated for voltage sags as short as 1 cycle. All other 8 Watt lamp

starts to malfunction for sags that last at least for 2 cycles. GE Edison's CFL failed to light up if the encountered sag depth is less than 35% remaining voltage and hence it is the most sensitive 8 Watt lamp considering sag magnitude. Furthermore, it is important to note that all of the CFL that have been tested do not satisfy the design goals of SEMI F47 and ITIC standards.

In order to analyze the relationship between light output variation and the ballast's dc bus voltage, a comparison of these variations for a sag that leaves 30% remaining voltage for 5 cycles are made in Fig. 10. From Fig. 10a, it can be seen that the decay rate of light output for all CFLs are almost the same. However for Osram's CFL, it seems that it decease little faster than the others. If one analyzes the variation of dc bus voltage of the ballast circuit of these lamps as shown in Fig 10b, the co relationship between light output and dc bus voltage can be clearly noted where fastest decrease in dc bus voltages seems to occur for the same CFL. The reason for this is due to the different size of dc filter capacitor used in Block 3 of ballast circuit shown in Fig. 1. Filter capacitors used in the 8 Watt Philips, Osram, Hitachi and GE Edison CFLs are 2.2 µF, 1.5 µF, 2.2 µF, 2.7 µF, respectively.

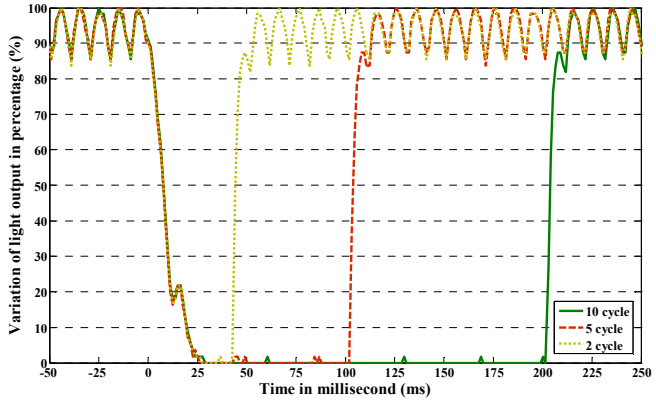


Fig.8: Effect of sag duration on the light output at 30% remaining voltage for Osram's CFL

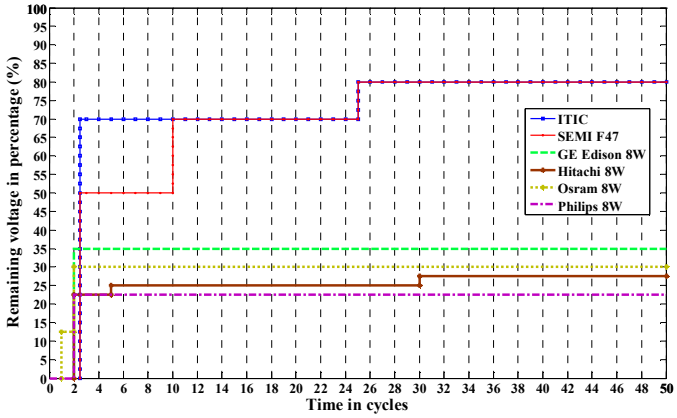
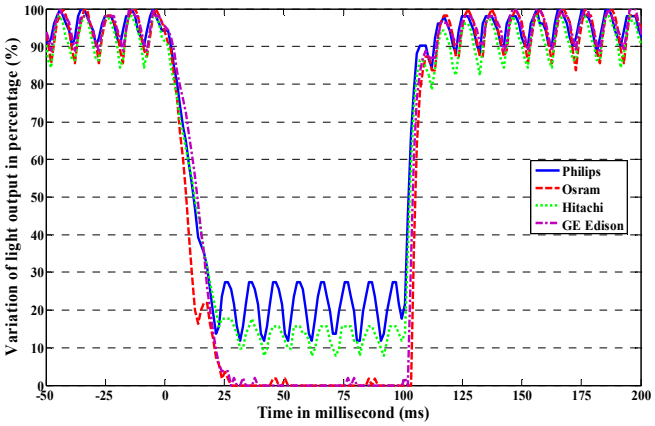
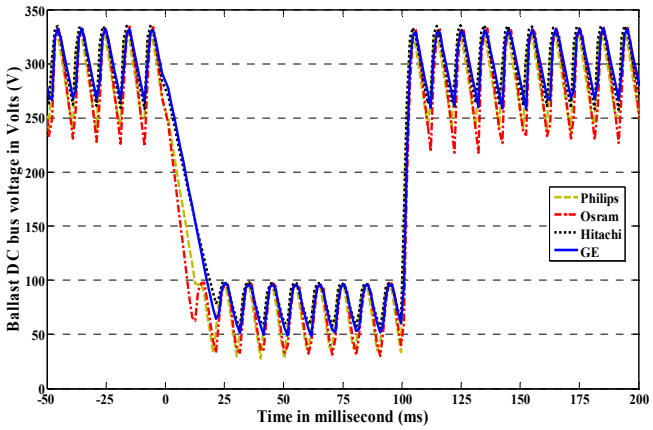


Fig.9: Voltage tolerance curves of various 8 Watt CFLs



(a)



(b)

Fig.10: Sensitivity of different branded CFLs at 30% remaining voltage lasting 5 cycles (a) on the light (b) dc bus voltage

4.2 Analysis of Different Wattage CFLs

Three lamps with different power ratings namely 8, 14, and 32 Watt CFLs from Philips are chosen for this study. Fig.11 shows the sensitivity of studied lamps for the same zero illuminance malfunction condition. The results of Fig. 11 shows that different wattage lamps have different immunity level for voltage sags although they are produced by the same manufacturer with similar CFL design.

When the immunity level of the tested lamps is compared in terms of sag magnitude, it is can be noted that the 8 Watt lamp is least sensitive one while the 32 watt lamp is the most sensitive to voltage sag. Moreover, all three lamps seems to extinguish completely only when the sag duration is longer than 2 cycles. None of the tested lamps from Philips seems to turn off completely for any sag event which last less than 2 cycles.

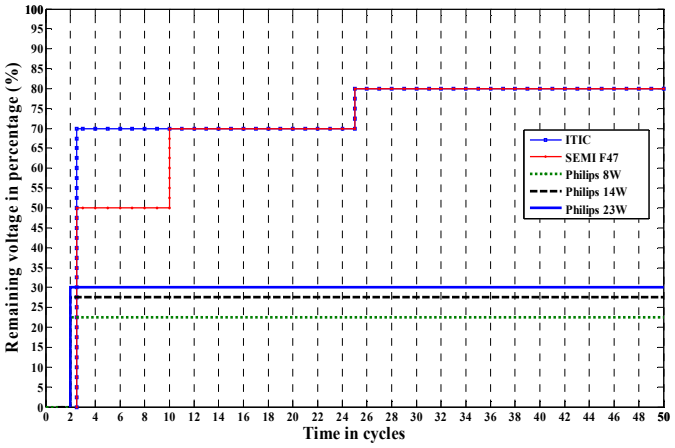


Fig.11: Voltage tolerance curves of different wattage CFLs

4.3 Results of Sensitivity Improvement Method

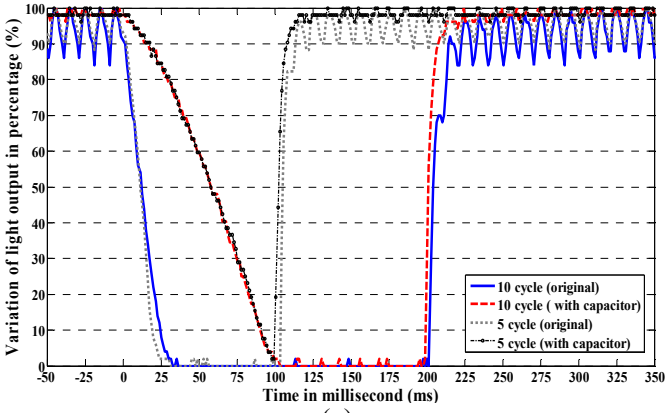
As described in Section 2 and from the previous analysis, it is evident that there is a parameter that can be adjusted to alleviate the sensitivity of the CFLs during voltage sags. According to (2) the holdup time, T_h, can be increased by increasing the capacitance of the dc link capacitor, C_{dc}. Therefore, one way to improve the voltage sag ride through capability of CFLs is to add more capacitance to the dc bus which is at rectifier dc output. In order to increase holdup time and delay the rate of voltage decay at the rectifier output, a 2.2 µF/ 400V capacitor is used. The value of the additional capacitor is chosen randomly to illustrate its effect. It is then connected in parallel to the existing capacitor in the original ballast design of CFL. Once connected the experiment procedure presented in Section 3 is repeated.

Fig. 12a shows the effect of increasing the capacitance value at the rectifier dc output for 8 Watt GE Edison CFL. By comparing the time where it starts to switch off as in the original case and with added capacitor for sag depths of 10% remaining voltage that last for 5 cycles and 10 cycles , it can be noted that the time to reach the turn off condition can be delayed. With the addition of these capacitors, it can now ride through for any sag or interruption whose duration is less than or equal to 5 cycles.

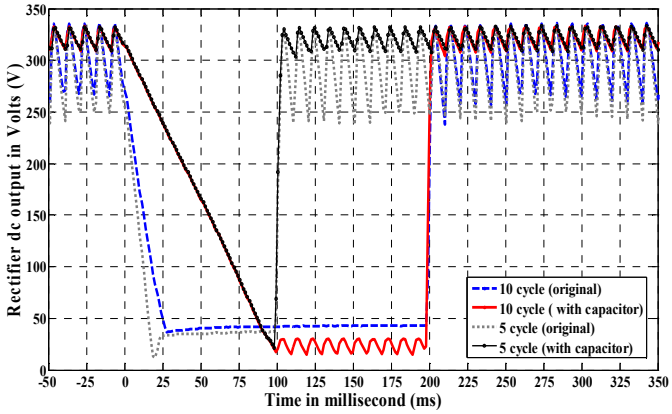
Fig. 12b shows the variation of dc link voltage before and after connecting the additional capacitor for the same CFL and sag events presented in Fig 12a. From Fig 12b it can be noted that the dc link voltage also have the similar pattern as light output variation shown in Fig 12a. For other CFLs, similar observation was noted and the effect of adding extra capacitor at dc bus is shown Figs. 13 to 15. These figures show the variation of light output and dc link voltage variation for sags having 10% remaining voltage with 5 cycle and 10 cycle duration.

Therefore, from this analysis and comparisons, it is possible to conclude that by adding extra capacitance at the rectifier dc output of the electronic ballasts of CFLs, voltage sag ride through capability of these CFLs can be improved. Another effect of increasing the dc link capacitor of the ballast is the reduction of light output fluctuation in steady state operation of the lamp. A simple comparison of the waveforms before and after the addition of dc bus capacitor shown in Fig. 12a clearly shows this improvement.

However this improvement in immunity level of the CFLs does not come without any drawback. This modification in the ballast circuit cause high inrush current during the recovery period of the sag event. Fig. 16 shows the current drawn from the mains by the 8 Watt GE Edison CLF during a voltage sag that leaves 5% remaining voltage for 6 cycles.



(a)



(b)

Fig.12: Effect of increasing dc link capacitance at the rectifier dc output on (a) light output (b) dc link voltage for GE 8 Watt CFL

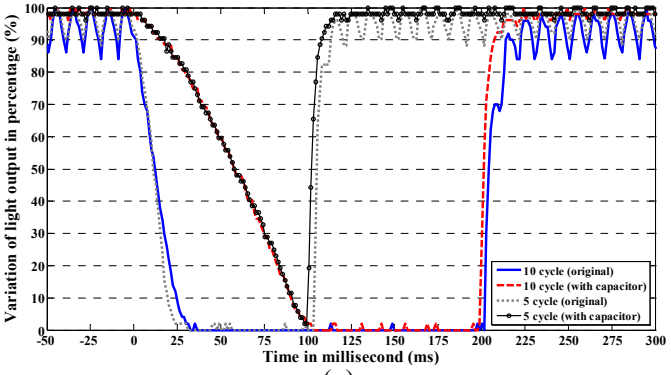
5 Conclusion

An extensive experimental study has been performed to determine the effect of voltage sag on low-wattage CFLs. From the results of the test data, voltage tolerance curves are constructed to describe the sensitivity of various CFLs to voltage sags. It may be concluded that the voltage tolerance level of the CFLs used in the test

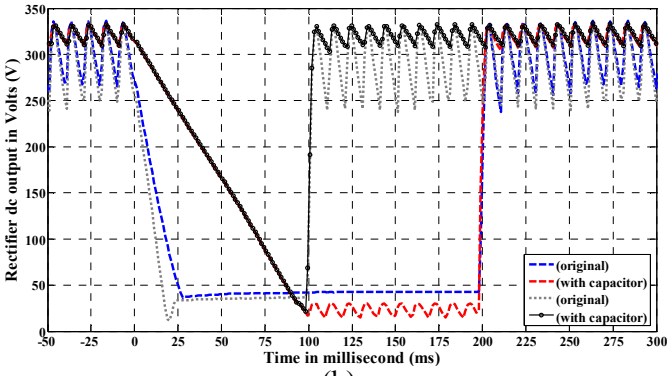
varies over a wide range. When the voltage immunity levels of the tested CFLs are compared with the ITIC and SEMI F47 standard, none of the CFL satisfies their design goals.

By comparing variations in the light output of the lamps, it is possible to conclude that the light intensity of the lamp not only depends on the voltage sag depth but also on the duration of the sag event depending upon the design of the ballast used in the lamp. CFLs from Osram and Hitachi are more sensitive to sag duration unlike lamps from GE Edison and Philips. Moreover, investigations of ballast dc bus voltage and light output variations of CFLs show that the light output of the CFLs depend on the dc bus voltage decay rate which consequently rely on the energy stored in the filter capacitor used in the ballast. The experimental results on different wattage CFLs show dissimilar voltage tolerance level to voltage sags albeit all carries same trade mark.

The experimental results on different CFLs with electronic ballasts also show that the installation of additional capacitors at the dc link can enhance CFLs' immunity level to voltage sag. However it is not recommended to install a large capacitor at the dc bus of the electronic ballast for the purpose of enhancing voltage sag ride through capabilities without incorporating proper inrush current control circuitry.

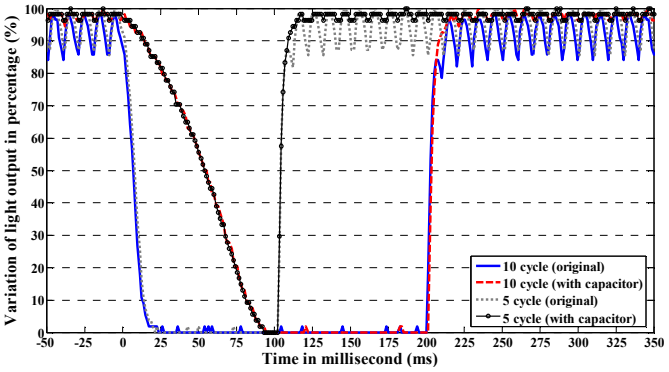


(a)

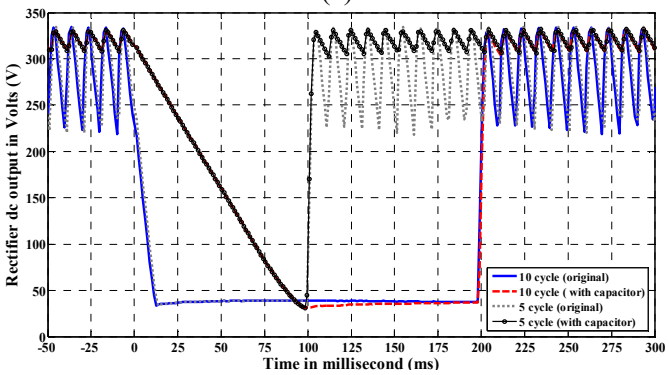


(b)

Fig.13: Effect of increasing dc link capacitance at the rectifier dc output on (a) light output (b) dc link voltage for Philips 8 Watt CFL

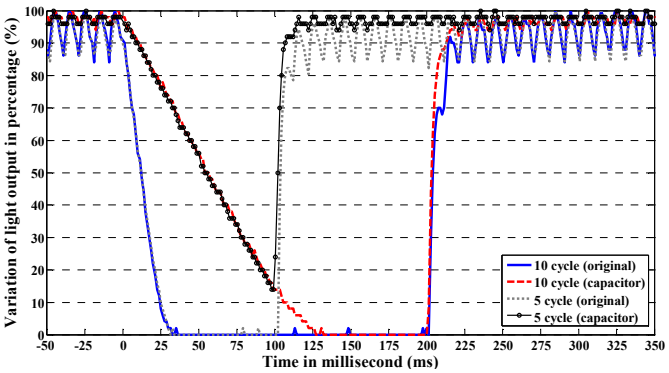


(a)

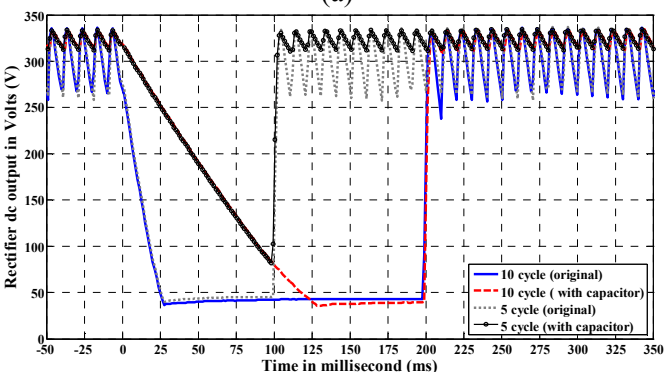


(b)

Fig.14: Effect of increasing dc link capacitance at the rectifier dc output on (a) light output (b) dc link voltage for Osram 8 Watt CFL



(a)



(b)

Fig.15: Effect of increasing dc link capacitance at the rectifier dc output on (a) light output (b) dc link voltage for Hitachi 8 Watt CFL

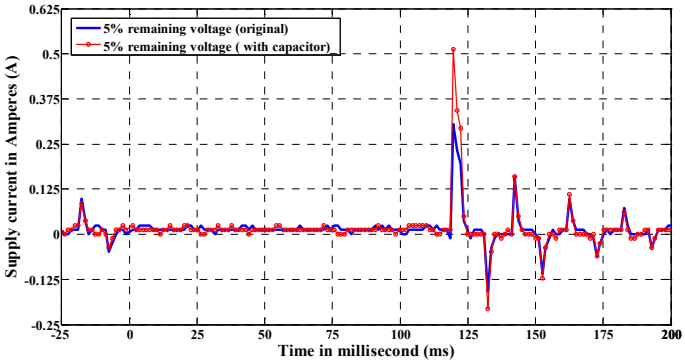


Fig.16: Effect of increasing dc link capacitance at the rectifier dc output on the inrush current for GE 8 Watt CFL

References:

[1] IEC, *Testing and Measurement Techniques – Voltage Dips, Short Interruptions, and Voltage Variation Immunity Tests*, IEC 61000-4-11, 2004.

[2] A.R. Seidel, F.E. Bisogno, T.B. Marchesan, R. Nd. Prado, Practical Comparison among High-Power-Factor Electronic Ballasts with Similar Ideas, *IEEE Transaction on Industry Applications*, Vol. 41, No.6, 2005, pp. 1574- 1583.

[3]V.G. Krizhanovski, D.V. Chernov, M.K. Kazimierczuk, Low-Voltage Electronic Ballast Based on Class E Oscillator, *IEEE Transaction on. Power Electronics*, Vol.22, No. 3, 2007, pp. 863-870.

[4] F.T. Wakabayashi, F.D. Dantas, F.A.S. Gonçalves, J.O.P. Pinto, C.A. Canesin, Measuring the Equivalent Resistance of Electrode Filaments of Tubular Fluorescent Lamps, during Dimming Operation, *WSEAS Transactions on Circuits and Systems*, Vol. 3, No. 3, 2004, pp. 437-443.

[5] J.T. Hwang, D.H. Kim, M.S. Jung, D.H. Kim, 550V SiP Compact Fluorescent Lamp Ballast IC, *32nd European Conference on Solid-State Circuits*, Montreux, 2006, pp. 576-579.

[6] S. J. Cunill, M. Salichs, Study and Characterization of Waveforms from Low-Watt (≤25 W) Compact Fluorescent Lamps with Electronic Ballasts, *IEEE Transaction on Power Delivery*, Vol.22, No. 4, 2007, pp. 2305 - 2311.

[7]J. Drapela, P. Mastny, Z. Prochazka, Interharmonics-Flicker Curves of Lamps and Compatibility Level for Interharmonic Voltages, *5th WSEAS/IASME International Conference on Electric Power Systems, High Voltages, Electric Machines*, Tenerife, 2005, pp. 579-584.

[8] Z. Wei, N.R. Watson, L.P. Frater, Modelling of Compact Fluorescent Lamps, *13th International Conference on Harmonics and Quality of Power*, Wollongong, 2008, pp. 1–6.

[9]I. Chatzakis, G.A. Vokas, F.V. Topalis, The Influence of Replacement of Incandescent Lamps with Compact Fluorescents to the Harmonic Distortion in Non-Interconnected Island Grids, *7th WSEAS International Conference on Electric Power Systems, High Voltages, Electric Machines*, Venice, 2007, pp. 219-226.

[10] R.R. Verderber, O.C. Morse, W.R. Alling, Harmonics from Compact Fluorescent Lamps, *IEEE Transaction on Industry Applications*, Vol.29, No. 3, 1993, pp. 670 - 674.

[11] R. Arseneau, M. Ouellette, The Effects of Supply Harmonics on the Performance of Compact Fluorescent Lamps, *IEEE Transaction on Power Delivery*, Vol.8, No. 2, 1993, pp. 473 - 479.

[12]M.D.Teixeira, G. Paulillo, A.R. Aoki, D.L. Archanjo, Harmonic Distortions Produced by Compact Fluorescent Lamps in Distribution Networks, *4th WSEAS International Conference on Applications Of Electrical Engineering*, Prague, 2005, pp. 1-7.

[13] D. Matvoz, M. Maksic, "Impact of Compact Fluorescent Lamps on the Electric Power Network, *13th International Conference on Power Electronics and Drive Systems*, Wollongong, 2008, pp. 1–6.

[14] W.N. Chang, C.J. Wu, S.S. Yen, The Influence of Voltage Flicker on Residential Lamps, *International Conference on Power Electronics and Drive Systems*, Singapore, 1997, pp. 392-396.

[15] S. Chen, C.M. Lo, M.K. Foo, K.T. How, Testing of Fluorescent Lamps for Its Flickering Susceptibility Towards Interharmonic Voltages, *International Conference on Power Engineering*, Singapore, 2007, pp. 326-331.

[16]M.J. Ouellette, R. Arseneau, The Effects of Undervoltage on the Performance of Compact Fluorescent Systems, *Annual Meeting. Industry Applications Society*, New York, 1992, pp. 1872 - 1879.

[17]L. Frater, N. Watson, Light Flicker Sensitivity of High Efficiency Compact Fluorescent Lamps, *Australasian Universities Power Engineering Conference*, Perth, 2007, pp. 1-6.

[18]D.S. Dorr, A. Mansoor, A.G. Morinec, J.C. Worley, Effects of Power Line Voltage Variations on Different Types of 400-W High-Pressure Sodium Ballasts, *IEEE Transaction on Industry Applications*, Vol. 33, No. 2, 1997, pp. 472-476.

[19]F.J. Diaz, F.J. Azcondo, F. Ortiz, A. Ortiz, M. Maana, C. Renedo, Effects of Voltage Sags on Different Types of Ballasts for 150-W HPS Lamps, *9th International Conference on Electrical Power Quality and Utilisation*, Barcelona, 2007, pp. 1-6.

[20] S. Saksena, S.G. Karady, Effects of Voltage Sags on Household Loads, *IEEE General Meeting, Power*

Engineering Society, New York, 2005, pp. 2456-2461.

[21]P. Pohjanheimo, M. Lehtonen, Equipment Sensitivity to Voltage Sags-Test Results for Contactors, PCs and Gas Discharge Lamps, *10th International Conference on Harmonics and Quality of Power*, Rio de Janeiro, 2002, pp. 559- 564.

[22]A. Vitanza, R. Scollo, A. Hayes, Electronic Fluorescent Lamp Ballast, *STMicroelectronics Application Note AN527/1294*, 1999.

[23]N.K. Medora, A. Kusko, M. Thompson, Impact of Line Voltage Sag on Switch Mode Power Supply Pperation, *3rd IEEE Conference on Industrial Electronics And Applications*, Singapore, 2008, pp. 2178-2183.

[24] J. Fernandez, M. Sebastian, M. Hernando, P. Villegas, J. Garcia, Helpful Hints to Select a Power-Factor-Correction Solution for Low- and Medium-Power Single-Phase Power Supplies, IEEE *Transaction on Industrial Electronics*, Vol. 52, No. 1, 2005, pp. 46-55.