

Five level parallel inverter for DTC – SVM of induction motor

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Abstract: - Direct Torque Control is a control technique used in AC drive systems to obtain high performance torque control. The conventional DTC drive contains a pair of hysteresis comparators, a flux and torque estimator and a voltage vector selection table. The torque and flux are controlled simultaneously by applying suitable voltage vectors, and by limiting these quantities within their hysteresis bands, de-coupled control of torque and flux can be achieved. However, as with other hysteresis-bases systems, DTC drives utilizing hysteresis comparators suffer from high torque ripple and variable switching frequency. The most common solution to this problem is to use the space vector with multilevel inverter depends on the reference torque and flux. The reference voltage vector is then realized using a voltage vector modulator. Several variations of DTC-SVM with low cost multilevel inverter or parallel inverter (five level) have been proposed and discussed in the literature. The work of this project is to study, evaluate and compare the various techniques of the DTC-SVM with parallel inverter applied to the induction machines through simulations. The simulations were carried out using MATLAB/SIMULINK simulation package. Evaluation was made based on the drive performance, which includes dynamic torque and flux responses, feasibility and the complexity of the systems. It is better technology in electric vehicles.

Key-Words: - Multilevel inverter, DTC-SVM, Converter, Electric Vehicles, Reliability, SVPWM, 5 Level parallel Inverter.

1 Introduction

MULTILEVEL inverters have been developed to overcome harmonics in output, and improve the shape of output to reach sinusoidal waveform. By using PWM inverters have been developed to overcome shortcomings in solid-state switching device ratings. But here multilevel cost is very high. My proposed structure is overcome this problem, and also decrease the on time of every thyristor /Gto. So the reliability and lifetime of circuit will be increase. Most discussed in the literature are three level to several multilevel with suitable new PWM method for proposed circuits.

Centered, Proposed structure has almost half of Gtos compare with previous structure. Previous structures

of 7 level inverter are shown in fig 1. Fig 1a is diode clamped inverter and Fig 1b is an H-Bridge inverter configuration and Fig 1c is capacitor clamped inverter. Proposed inverter (parallel) is shown in Fig 2. Compare to this circuits parallel inverter have only 6 Gtos per phase, but previous circuits have 12 Gtos per phase for 7 level inverter.

Here, we develop new PWM method for this circuit for decrease on time period of every Gto. So the life time will be increase. The switching Strategies are shown in Table1. In this paper shown results for various levels of multilevel inverter by using matlab Simulink.

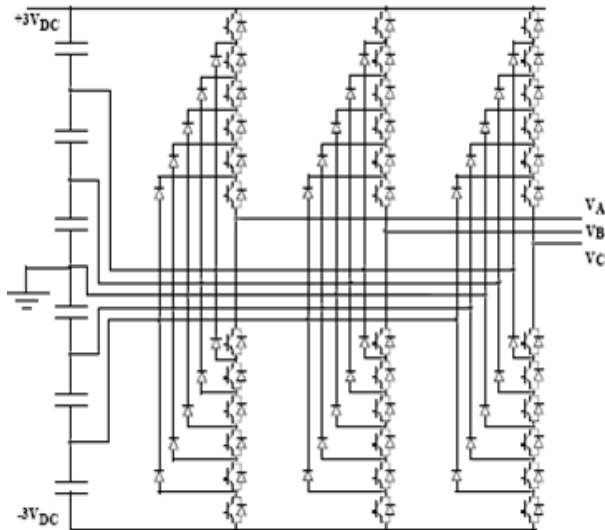


Fig 1a: 7 level diode clamped inverter.

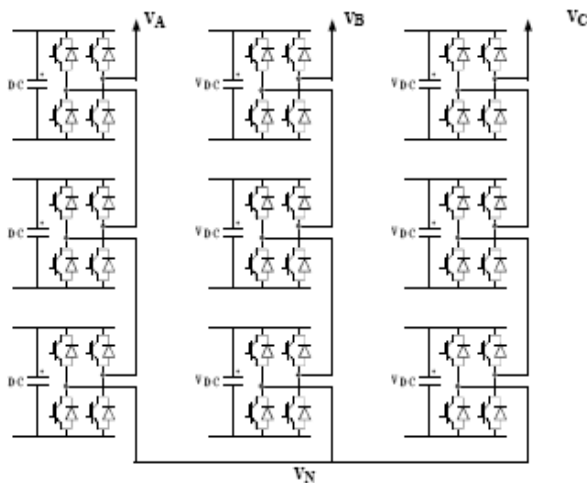


Fig 1b: 7 level H-Bridge inverter.

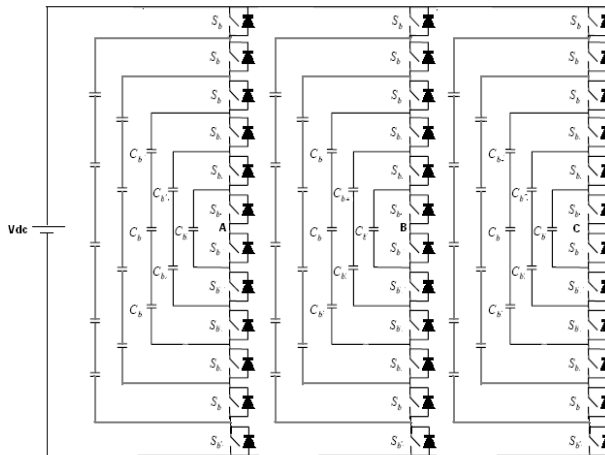


Fig 1c 7 level flying capacitor inverter

Fig 1: 7 level inverter.

Here in 7 level inverter, three type of multilevel configurations have the number of Gtos are 12. But in fig 2 the number of Gtos is 6 of 7 level inverter.

The view of the structure is parallel connections of Gtos, so in my view, it is called as parallel multilevel inverter.

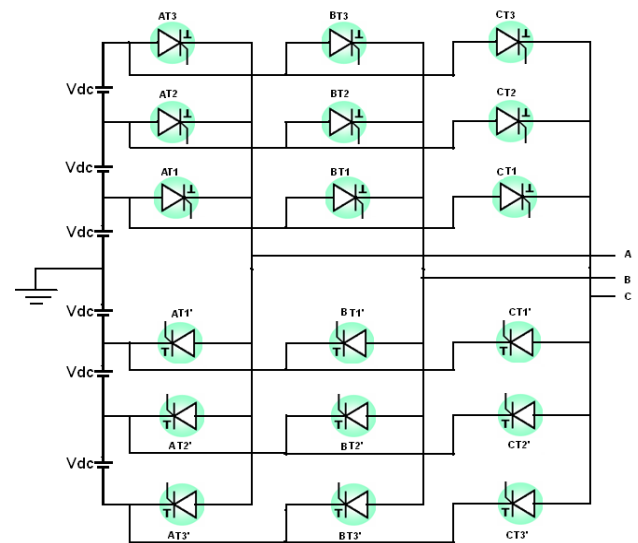


Fig 2: 7 level parallel multilevel inverter.

For m level parallel inverter have $m-1$ Gtos per phase and total number of sources is $m-1$ ($m \leq 3$). It is only odd number of m this is shown in Fig3. In Fig 2, at first, only AT1 is on then after some time AT2 is on and same time AT1 will off, after some time At3 will on and at the same time AT2 will off. Again some time At3 will off and same time AT2 will on and some time AT2 will off and same time AT1 will on. This is for half symmetric wave.

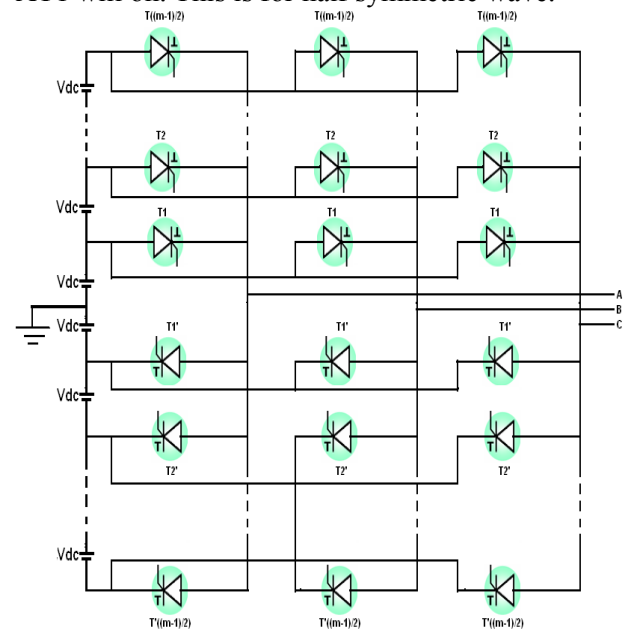


Fig3: m level parallel inverter.

2 Modulation Strategies

This new switching strategies are shown in Table 1. And new SPWM technique is shown in Fig 4. From this fig we are used only 3 carrier waves for 7 level inverter. Generally for m level inverter the number of carrier waves is (m-1)/2. The output magnitude is controlled by using modulation index (m_i), and frequency is controlled by controlling only reference wave frequency or frequency ratio mf.

Index m_a and frequency ratio is defined as

$$m_a = \frac{2 * A_r}{(m-1) * A_c}$$

$mf = f_c / f_r$

Where A_c = magnitude of carrier wave signal.

A_r = magnitude of reference wave signal

m = level of inverter

f_r = reference wave frequency

f_c = carrier wave frequency.

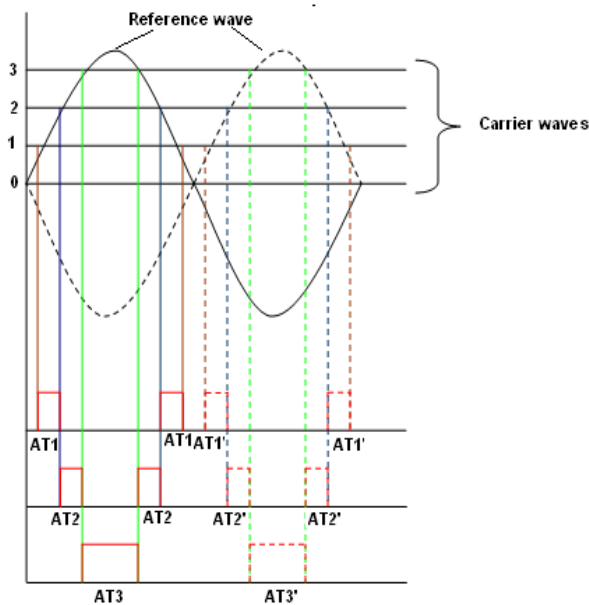


Fig4: New SPWM for 7 level parallel inverter.

In Fig4, T3, T3' is on only one time and remaining switches are on twice per one complete cycle for 7 level parallel inverter. Generally we use triangle waves for carrier waves in this new SPWM technique then 1 represent PWM signal in table. This is shown in Table2. In this table PWM represent gate signal 1 or on state for Gtos and 0 for off state. Generally PWM signals have zeros and ones, in parallel inverter switches except T3& T3' are on if PWM is 1, and if PWM is zero then

immediately lower switch will goes to on state. This is shown in Table2. Here some switches have two modes.

T1	T2	T3	T1'	T2'	T3'	Vo(Ph)
0	0	0	0	0	0	0
1	0	0	0	0	0	+V
0	1	0	0	0	0	+2V
0	0	1	0	0	0	+3V
0	1	0	0	0	0	+2V
1	0	0	0	0	0	+V
0	0	0	0	0	0	0
0	0	0	1	0	0	-V
0	0	0	0	1	0	-2V
0	0	0	0	0	1	-3V
0	0	0	0	1	0	-2V
0	0	0	1	0	0	-V
0	0	0	0	0	0	0

Table 1: Switching Strategies for 7 level parallel inverter.

T1	T2	T3	T1'	T2'	T3'	VPh
0	0	0	0	0	0	0
pwm	0	0	0	0	0	+V
0/ pwm	pwm	0	0	0	0	+2 V
0	0/ pwm	pwm	0	0	0	+3 V
0/ pwm	pwm	0	0	0	0	+2 V
pwm	0	0	0	0	0	+V

0	0	0	0	0	0	0
0	0	0	pwm	0	0	-V
0	0	0	0/ pwm	pwm	0	-2V
0	0	0	0	0/ pwm	pwm	-3V
0	0	0	0/ pwm	pwm	0	-2V
0	0	0	pwm	0	0	-V
0	0	0	0	0	0	0

Table2: New PWM/SPWM technique for 7 level parallel inverter.

This new SPWM technique is developed by using logic gates. This is shown in Fig5 for 7 level parallel inverter.

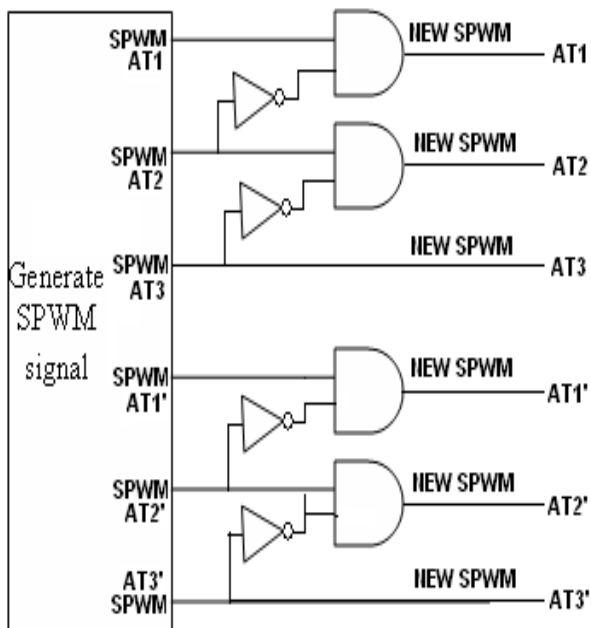


Fig5: New SPWM generation circuit.

In this paper I present out puts of 3 to 21 level parallel inverter with $m_i=1$, by using matlab Simulink.

3 Parallel Inverter for DTC of Induction Motor

Induction motor torque control has traditionally been achieved using Field Oriented Control (FOC). This involves the transformation of stator currents into asynchronously rotating d-q reference frame that is typically aligned to the rotor flux. In this reference frame, the torque and flux producing components of the stator current are decoupled. A PI controller is then used to regulate the output voltage to achieve the reputed stator current and therefore torque. This PI controller limits the transient response of the torque controller.

Direct Torque Control (DTC) uses an induction motor model to achieve a desired output torque. By using only current and voltage measurements, it is possible to estimate the instantaneous stator flux and output torque. An induction motor model is then used to predict the voltage required to drive the flux and torque to demanded values within a fixed time period. This calculated voltage is then synthesized using space vector modulation (SVM).

The stator flux vector, and the torque produced by the motor, T_{em} , can be estimated using and respectively. These only require knowledge of the previously applied voltage vector, measured stator current, and stator resistance.

As shown in Fig 6, the voltage required to drive the error in the torque and flux to zero is calculated directly. The calculated voltage is then synthesized using Space Vector Modulation. If the inverter is not capable of generating the required voltage then the voltage vector which will drive the torque and flux towards the demand value is chosen and held for the complete cycle.

$$\overline{\psi_s} = (\overline{V_s} - r_s \overline{I_s}) dt$$

$$T_{em} = \frac{3}{2} \frac{P}{2} (\overline{\psi_s} \times \overline{I_s})$$

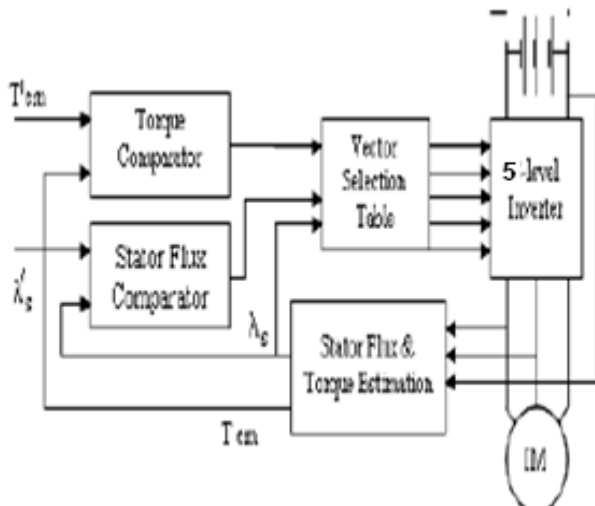


Fig 6.a General block diagram of 5 level DTC

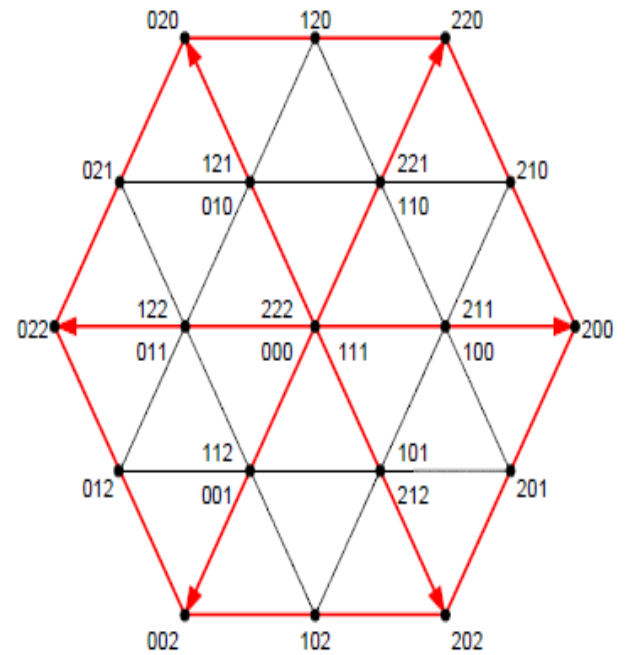


Fig 7: space vector modulation for 5 level parallel inverter

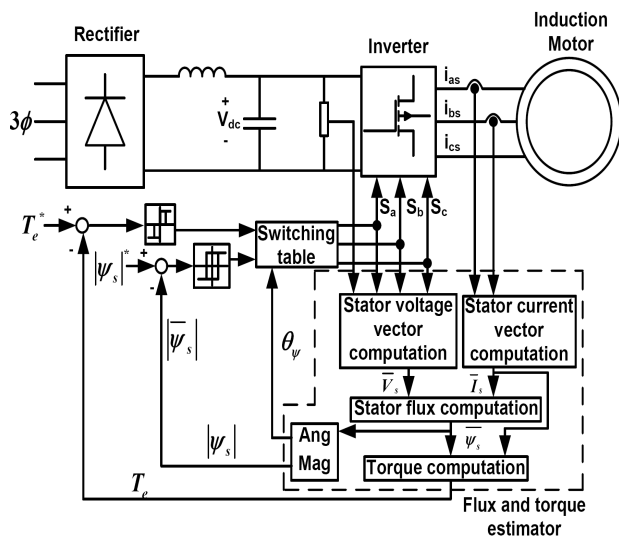


Fig 6.b Basic DTC induction motor scheme

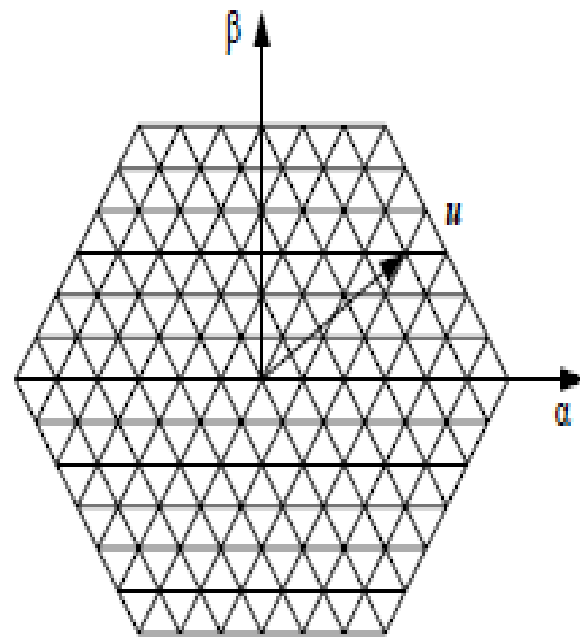


Fig 7.b space vector modulation for m-level parallel inverter

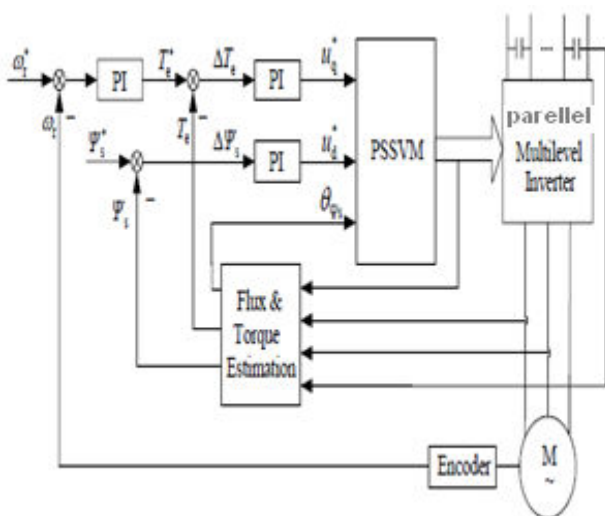


Fig 6.c System diagram of PSSVM-DTC

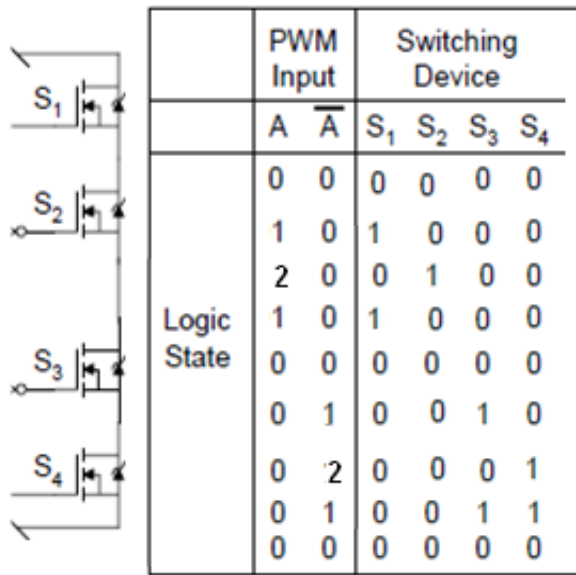


Fig 7.c: pulse generation for five level parallel inverter.

4 Simulation Results

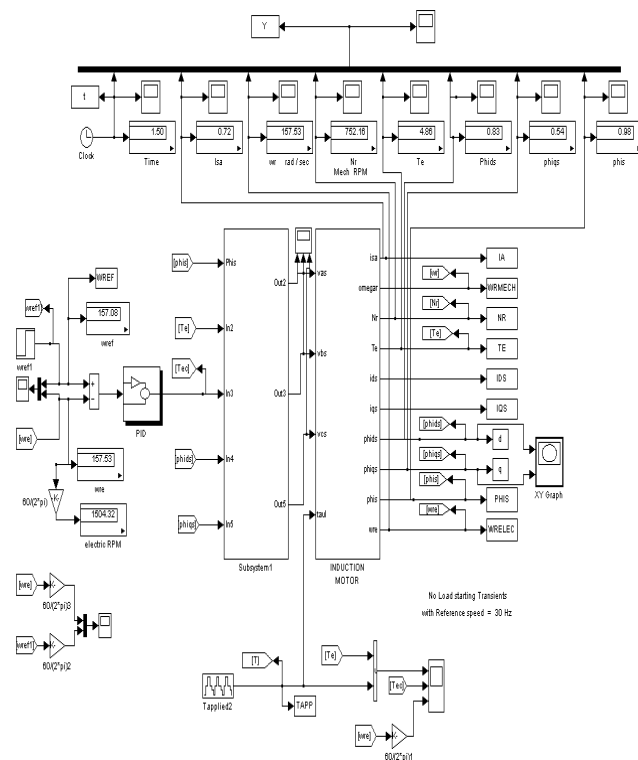


Fig 8.a Inverter fed induction motor (dct-svm)

FIVE LEVEL INVERTER(SVM) FED INDUCTION MOTOR

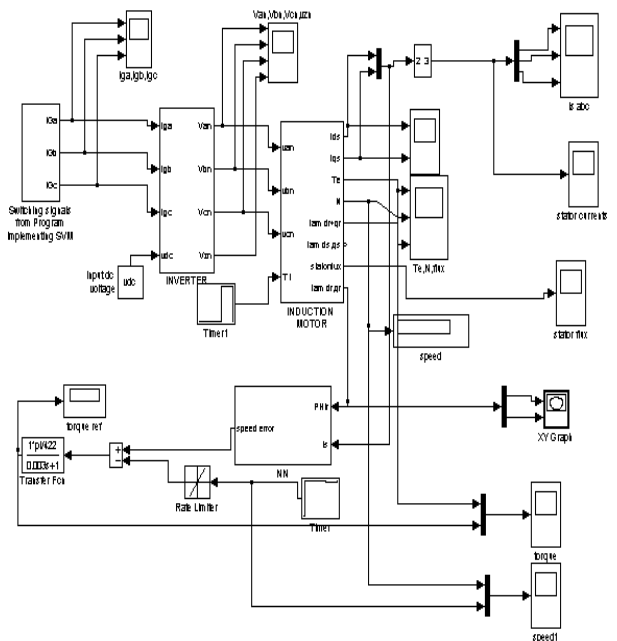


Fig. 8.a diagram of general DTC and fig 8.b diagram of DTC-SVM with five level parallel inverter(5 level low cost inverter) using SIMULINK/MATLAB.

Fig. 9 (a) and (b) show the simulation results for load stator currents for general and DTC-SVM with five level parallel (low cost multilevel inverter) respectively for a reference speed of 1440 rpm. As shown, reduces steady-state ripple in stator current.

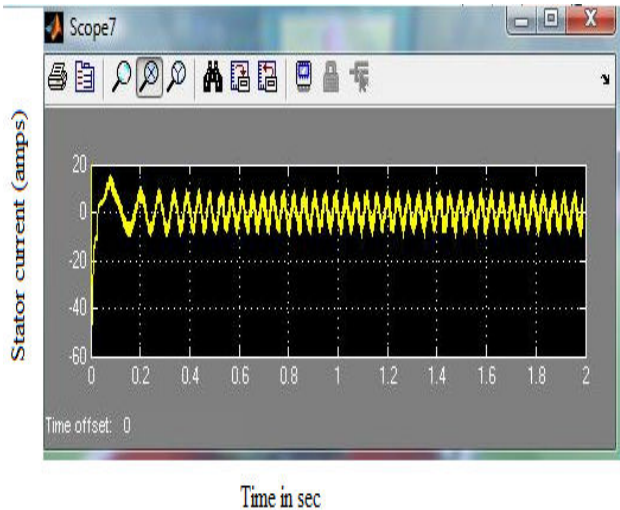


Fig (a)

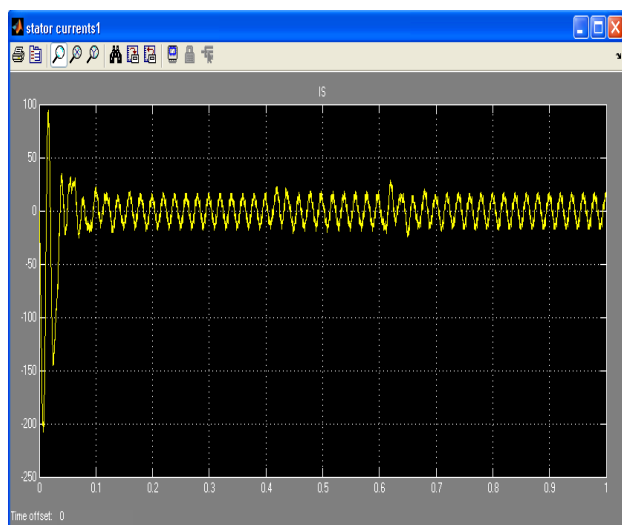


Fig (b)

Fig. 9 Simulation results for stator current of (a) general DTC (b) DTC-SVM with five level parallel (low cost multilevel inverter) for 1440 rpm

Fig. 10 (a) and (b) show the stator flux response for general and DTC-SVM with five level parallel (low cost multilevel inverter) respectively for a reference speed of 1440 rpm. The classical DTC uses a constant flux command of 0.742 Wb, whereas SVM method uses an optimized value, which 0.989 Wb.

The SVM method reduces the flux ripple to a considerable lower amount.

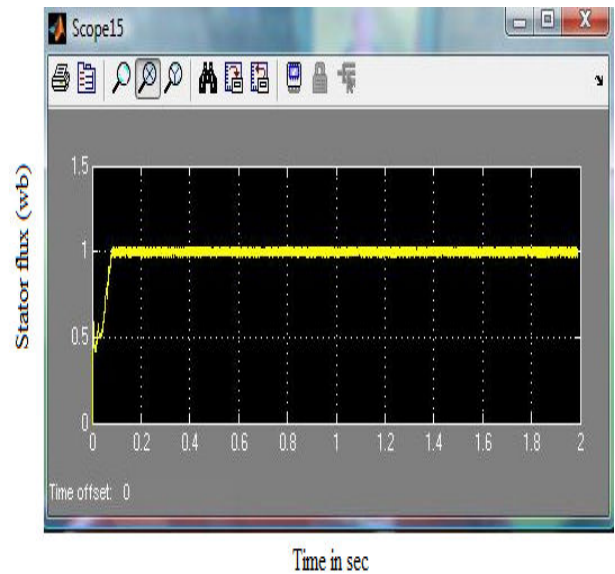


Fig (a)

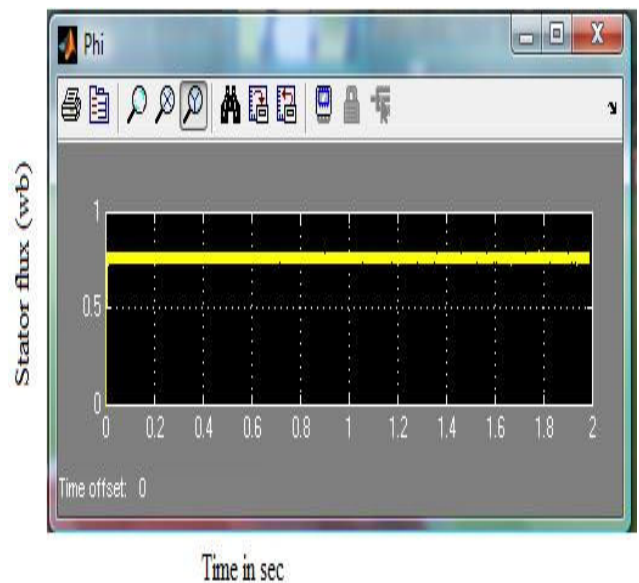


Fig (b)

Fig. 10 Simulation results for flux response of (a) general DTC (b) DTC-SVM with five level parallel (low cost multilevel inverter) for 1440 rpm

Fig.11 (a) and (b) show the 3-phase stator current for general and DTC-SVM with five level parallel (low cost multilevel inverter) respectively for a reference speed of 1440 rpm. An on load torque applied at 2 second. The enlarged view of Fig.11 (a) and (b) at a torque load condition is presented. The proposed method (DTC-SVM with five level inverter) is able to reduce ripples in 3-phase stator current as well.

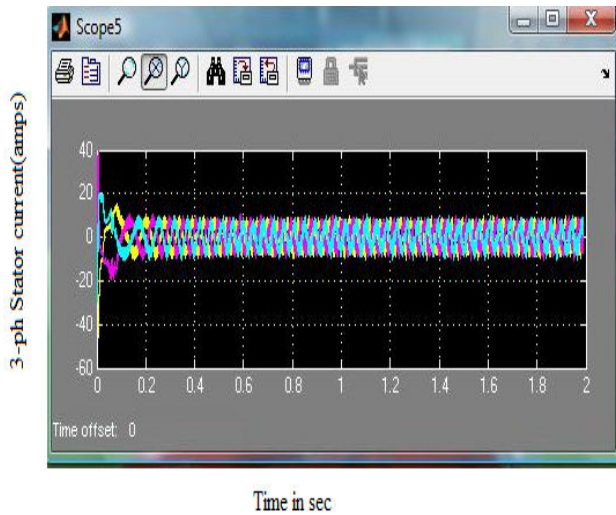


Fig (a)

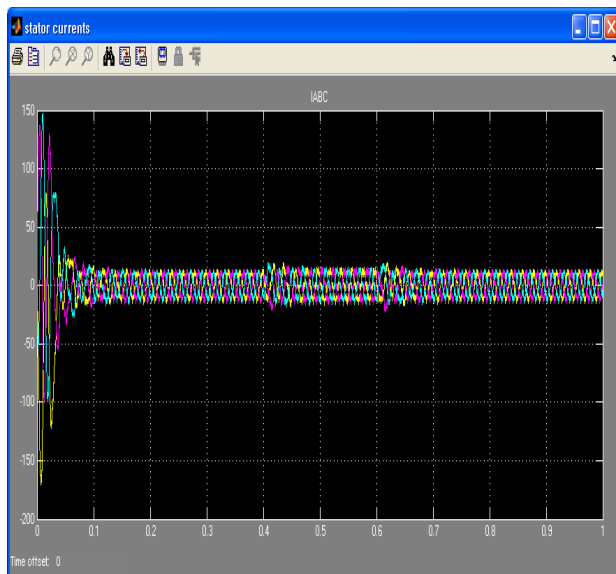


Fig (b)

Fig. 11 Simulation results for stator current of (a) general DTC (b) DTC-SVM with five level parallel (low cost multilevel inverter) for 1440 rpm

Fig.12 (a) and (b) Show the speed for general and DTC-SVM with five level parallel (low cost multilevel inverter) respectively for a reference speed of 1440 rpm. It is observed that, the transient and steady state ripples are less in DTC-SVM.

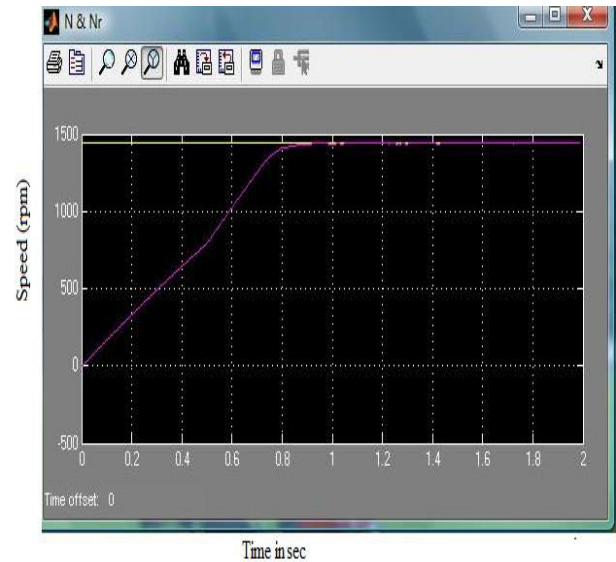
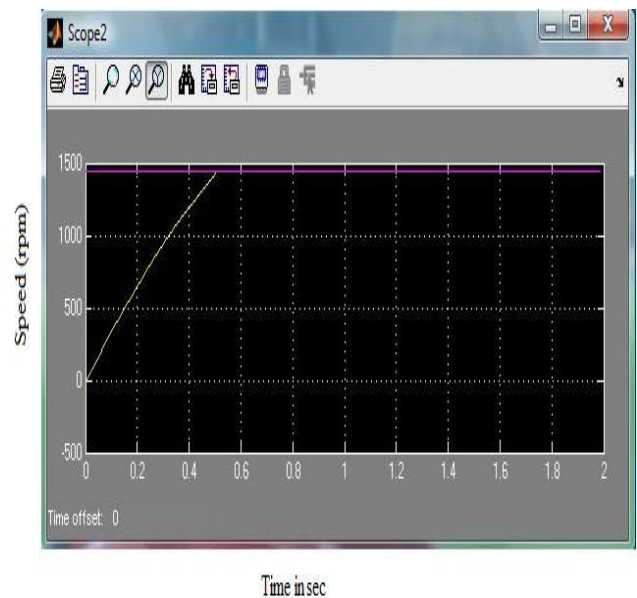


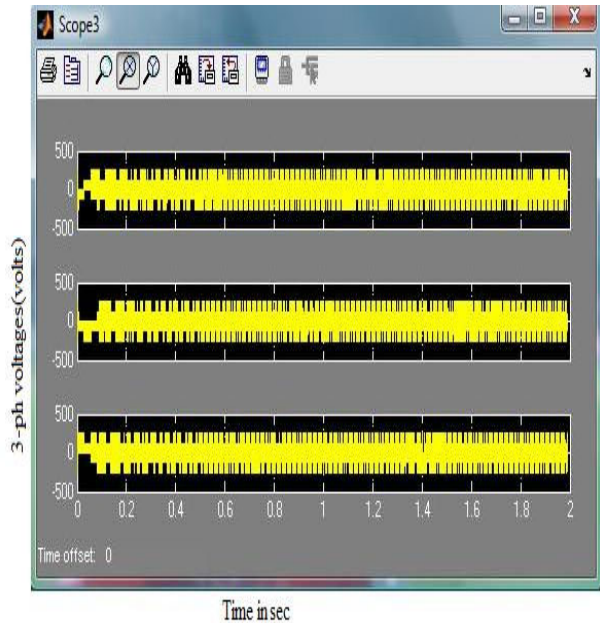
Fig (a)



Fig(b)

Fig. 12 Simulation results for Speed of (a) general DTC (b) DTC-SVM with five level parallel (low cost multilevel inverter) for 1440 rpm & on load

Fig.13 (a) and (b) Show the 3-phase output voltages for general and DTC-SVM with five level parallel (low cost multilevel inverter) respectively for a reference speed of 1440 rpm. It is observed that, in on load condition the output voltage ripples are reduced in DTC-SVM



Fig(a)

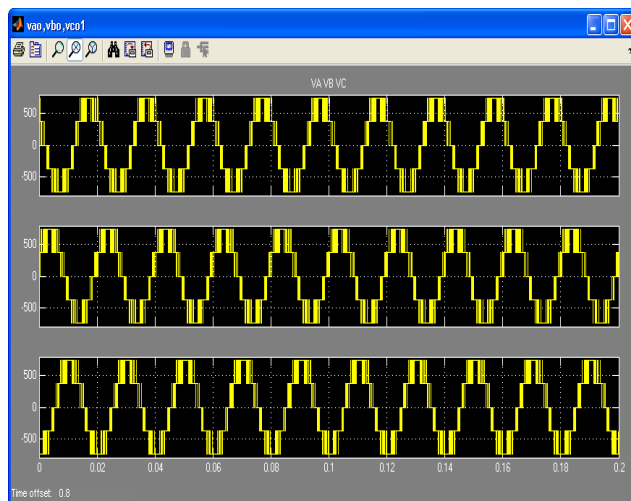


Fig (b)

Fig. 13 Simulation results for 3-phase voltages of ((a) general DTC (b) DTC-SVM with five level parallel (low cost multilevel inverter) for 1440 rpm

Fig. 14 (a) and (b) show stator flux trajectory for general and DTC-SVM with five level parallel (low cost multilevel inverter) respectively for a reference speed of 1440 rpm. The smoother flux trajectory for the proposed one confirms the ripple reduction in torque, flux, stator current and speed response.

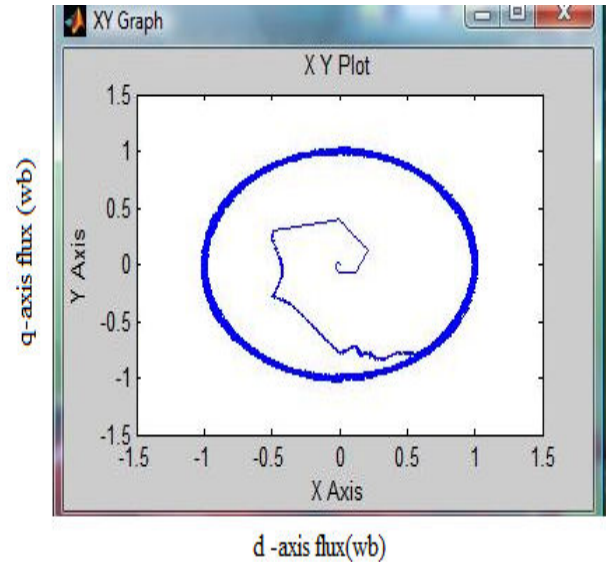


Fig (a)

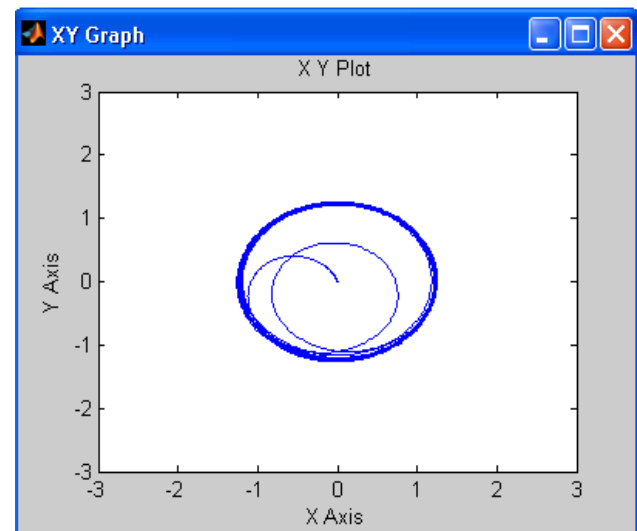


Fig (b)

Fig. 14 (c) and (d) show electric torque response for general and DTC-SVM with five level parallel (low cost multilevel inverter) respectively a reference speed of 1440 rpm.

A step change in load torque from 20 N-m to 5 N-m is applied at 1.5 second. In addition to the inherent disadvantages of general DTC, the constant reference flux causes higher ripple at lower torque level. The proposed (DTC-SVM with five level parallel inverter) method causes lower ripple at lower torque level. In addition to the torque ripple minimization ($\sim 1/12^{\text{th}}$), this method is also able to eliminate the torque under-shoot and over-shoots.

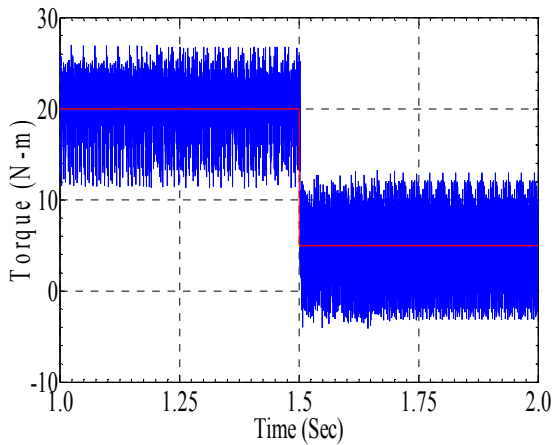


Fig (c)

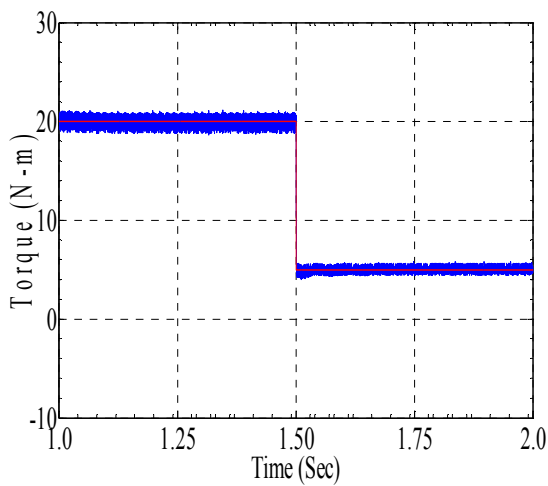


Fig (d)

Fig. 14 Simulation results for torque response of (c) general DTC (d) DTC-SVM with 5 level parallel inverter for 1440 rpm & on load

5- Level parallel inverter

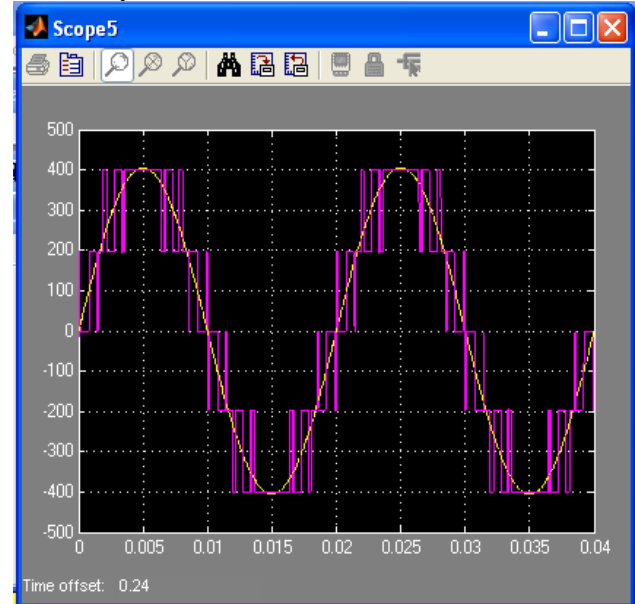


Fig 15.1: phase voltage of 5 level inverter ($m_i=1$; $m_f=21$; $A_r=1$). THD is 28.21%

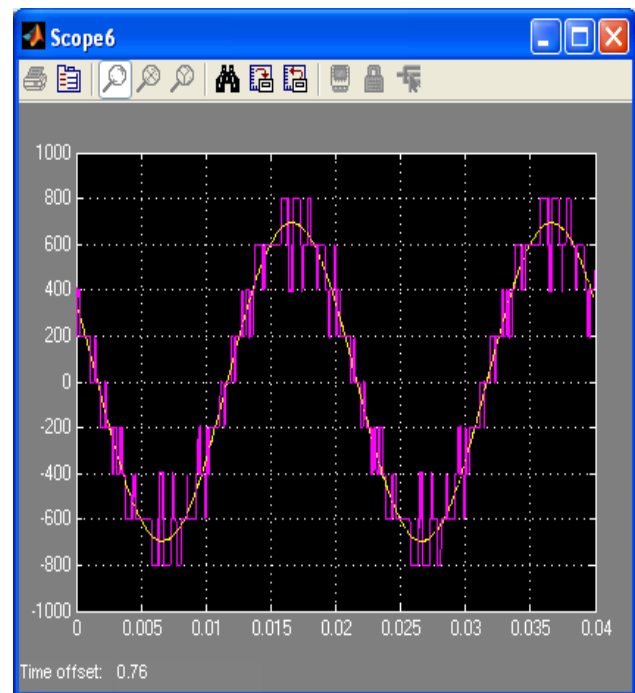


Fig 15.2: line voltage of 5 level inverter ($m_i=1$; $m_f=21$; $A_r=1$).

Comparison parallel inverter with different types of inverters:

Inverter Configuration	Parallel Inverter	Diode Clamped Inverter	Flying Capacitor Inverter	H-Bridge (Cascaded) Inverter
Main Switching Devices	$(m-1)$	$2(m-1)$	$2(m-1)$	$2(m-1)$
Main Diodes	$(m-1)$	$2(m-1)$	$2(m-1)$	$2(m-1)$
Clamping Diodes	0	$(m-1)(m-2)$	0	0
DC Bus Capacitors	$(m-1)$	$(m-1)$	$(m-1)$	$(m-1)/2$
Balancing Capacitors	0	0	$(m-1)(m-2)/2$	0
Number of Carrier Waves	$(m-1)/2$	$(m-1)$	$(m-1)$	$(m-1)$

Here out of DC bus bars, this parallel inverter is most economical and efficient for both inverter applications and AD drives. In this table blue color configurations are most economical.

5 Conclusion

This technology is better for multilevel inverter from construction and life time point of view, and also low THD values. From table 3, we observe except DC Bus Capacitors, parallel inverter is better than remaining configurations. So, cost will be reduce and achieve good performance by using this parallel inverter. From figure5, we observe that the on time period of main switching devices is low, so life time of this inverter is increase, here not possible that misfire. It is very suitable for electric vehicles.

This paper has proposed a new SPWM and new SVPWM control method for a five-level parallel inverter. It operates the five-level inverter effectively as a three-level inverter. This allows for a significant reduction in the rating requirements of the clamping diodes, which would result in a lower cost implementation of this topology. The paper also extends the parallel topology to the use of a charge pump circuit as a method to obtain the required independently referenced gate drive power supplies. This charge pump circuit eliminates the need for individual power transformers for each of the gate drive supplies which significantly reduces the cost and size of these required supplies. With these proposed methods, a low power motor drive was constructed using inexpensive high-volume low-voltage power MOSFETs and other low cost discrete components. Thus the paper demonstrates the possibility of basing a low power motor drive around inexpensive power MOSFET switches that previously could not be used due to voltage limitations. While the proposed converter was constructed using discrete power devices, it should be noted that the two-level control principle and four-level charge pump make this topology attractive for integration into a single device package much like a standard six-pack arrangement. With the lower voltage rating requirement of the main switches, and the familiar and standard two-level control principles, this topology could become even more economical than a standard two-level inverter depending on what future device dies are developed and manufactured. This is important since the trend of integration into standard packages and automated manufacturing focus attention on performance and total cost while making the actual topology inside the package of lesser importance.

References:

- [1] Jose Rodriguez, Jih-Sheng Lai, and Fang Zheng Peng, "Multilevel Inverters: A Survey of Topologies, Controls, and Applications", *IEEE Transactions on Industrial Electronics*, Vol. 49, No. 4, August 2002. pages 724-738.
- [2] Leon M. Tolbert and Thomas G. Habetler, "Novel Multilevel Inverter Carrier-Based PWM Method", *IEEE Transactions on industry applications*, Vol. 35, No.5, sep/oct 1999. pages 1098 – 1107.
- [3] Zhong Du, Leon M. Tolbert, John N. Chiasson, and Burak Ozpineci, "A Cascade Multilevel Inverter Using a Single DC Source", 0-7803-9547-6/06/\$20.00 © 2006 IEEE pages 426-430.
- [4] Remus Teodorescu, Frede Blaabjerg, John. K. Pedersen, Ekrem Cengelci, and Prasad N. Enjeti, "Multilevel Inverter by Cascading Industrial VSI", *IEEE Transaction on industrial electronics*, Vol.49, No.4, August 2002. pages 832-838.
- [5] Xiaoming Yuan, Lvo Barbi, "A New Diode Clamping Multilevel Inverter", 0-7803-5160-6/99/\$10.00 © 1999 IEEE. pages 495-501.
- [6] Madhav D. Manjrekar, Peter K. Steimer, and Thomas A. Lipo, "Hybrid Multilevel Power Conversion System: A Competitive Solution for High-Power Applications" *IEEE Transaction on Industry Applications*, Vol. 36, No. 3, May/June 2000. pages 834-841.
- [7] Miguel Lopez G, Luis Moran T, Jose Espinoza C and Juan Dixon R, "Performance Analysis of a Hybrid Asymmetric Multilevel Inverter for High Voltage Active Power Filter Applications", 0-7803-7906-3/03/\$17.00 ©2003 IEEE, pages 1050-1055
- [8] Jamal Al-Nasseir, Christian Weindl, Gerhard Herold and Joerg Flotthmesch, "A Dual-use Snubber Design for Multi-Level Inverter Systems", 1-4244-0121-6/06/\$20.00.©2006 IEEE, pages 683-688
- [9] Gui-jia Su and Donald J.Adams, "Multilevel DC Link Inverter for Brushless Permanent magnet Motors with Very Low Inductance", *IEEE IAS*

annual Meeting, September 30 – October 5, 2001.

- [10] Ying Cheng Mariesa L. Crow, “A Diode – Clamped Multi-level Inverter For the StatCom/BESS”, 0-7803-7322-7/02/\$17.00 © 2002 IEEE pages 470-475
- [11] L. Li D. Czarkowski, Y.Liu P. Pillay, “Multilevel Selective Harmonic Elimination PWM in Series-Connected Voltage Inverters”, 0-7803-4943-1/98/\$10.00 (c) 1998 IEEE.
- [12] Leon M. Tolbert and Thomas G. Habetler, “Novel Multilevel Inverter Carrier-Based PWM Methods”, *IEEE IAS 1998 Annual Meeting*, St. Louis, Missouri, October 10-15, 1998, pp. 1424-1431.
- [13] J. Song-Manguelle and Prof. A. Rufer, “Multilevel Inverter for Power System Applications: Highlighting Asymmetric Design Effects From a Supply Network Point of View”, 0-7803-7781-8/03/\$17.00 © 2003 IEEE.
- [14] S.Mariethoz, A. Rufer, “Resolution and efficiency improvements for three-phase cascade multilevel inverters”, *35th Annual IEEE Power Electronics Specialists Conference 2004*. pages 4441-4446.
- [15] Nam S. Choi, Jung G. Cho and Gyu H. Cho, “A General Circuit Topology Of Multilevel Inverter”, 0-7803-0090-4/91/0700-0096\$01.00 © 1991 IEEE. pages 97-103.
- [16] Nikolaus P. Schibli, Tung Nguyen, and Alfred C. Rufer, “A Three-Phase Multilevel Converter for High-Power Induction Motors”, *IEEE Transactions on Power Electronics*, Vol. 13, No. 5, September 1998. pages 978-986.
- [17] Yiqiang Chen, Bakari Mwinyiwiwa, Zbigniew Wolanski, and Boon-Teck Ooi, “Unified Power Flow Controller (UPFC) Based on Chopper Stabilized Diode-Clamped Multilevel Converters”, *IEEE Transactions on Power Electronics*, Vol. 15, No. 2, March 2000. pages 258- 267.
- [18] Xiaoming Yuan, and Ivo Barbi, “Fundamentals of a New Diode Clamping Multilevel Inverter”, *IEEE Transaction on Power Electronics*, Vol. 15, No. 4, July 2000. pages 711-718.
- [19] Siroj Sirisukprasert, Jih-Sheng lai, and Tian-Hua Liu, “Optimum Harmonic Reduction with a Wide Range of Modulation Indexes for Multilevel Converters”, 0-7803-6401-5/00/\$10.00 © 2000IEEE. pages 2094-2099.
- [20] Giri Venkataramana, and Ashish Bendre, “Reciprocity-Transposition-Based Sinusoidal Pulsewidth Modulation for Diode-Clamped Multilevel Converter”, *IEEE Transaction on Industrial Electronics*, Vol.49, No. 5, October 2002. pages 1035-1047.
- [21] B.P. McGrath, D.G. Holmes, M. Manjrekar, and T.A. Lipo, “An Improved Modulation Strategy for a Hybrid Multilevel Inverter”, 0-7803-6404-X/00/\$10.00 (C) 2000.
- [23] Leon M. Tolbert, Fang Z. Peng, and Thomas G. Habetler, “Multilevel Inverters for Electric Vehicle Applications”, *WEPT’98*, Dearborn, Michigan, October 22-23, 1998.
- [24] Zhong Du, Burak Ozpineci, and Leon M. Tolbert, “Modulation Extension Control of Hybrid Cascaded H-bridge Multilevel Converters with 7-level Fundamental Frequency Switching Scheme”, Prepared by the Oak Ridge National Laboratory, Managed by UT-Battelle for the U.S. Dept. of Energy under contract DE-AC05-00OR22725.
- [25] J. Song-Manguelle, and A. Rufer, “Asymmetrical Multilevel Inverter for Large Induction Machine Drives”, *International Conference on Electrical Drives and Power Electronics*, Slovakia, 3-5 October 2001. pages 101-107.
- [26] Domenico casadei, Francesco Profumo, Giovanni, Angleo Tani. ” FOC and DTC: Two Viable Schemes for Induction Motor Control”, *IEEE Transaction on Power Electronics*, vol.17, no. 5, September 2002.
- [27] Hamid Reza Keyhani, Mohammad Zolghadri, Abdollah Homaifar. “An extended and Improved Discrete Space Vector Modulation Direct Torque Control for Induction Motor”, *35th Annual IEEE Power Electronics Specialists Conference 2004*.



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