Semiconductor Devices and Their Use in Power Electronic Applications

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Abstract: - Power semiconductor devices are the key electronic components used in power electronic systems. The solid-state power electronic revolution started with the invention of the thyristor or Silicon Controlled Rectifier (SCR) in 1956, and many power semiconductor devices have been produced since then. Advances in semiconductor technology have improved the efficiency of electronic devices which resulted in reduced cost, weight and size of power electronic systems. Power Integrated Circuits (PIC) have been developed as a result of recent advances in integration technology, which led to a significant improvement in reliability of power modules. This has extended the use of power converters for portable, aerospace and automotive applications. Thyristors and Insulated Gate Bipolar Transistors (IGBT's) have been used extensively in power electronic circuits. Power diodes are some of the important devices for inverter and freewheeling applications. Diode reverse recovery under high di/dt operating conditions may result device and circuit failure.

In this paper, detailed study and progress made in power semiconductor devices, their characteristics, packaging, thermal issues and different high power application are given.

Key-Words: - Power Semiconductors Devices, Thermal Effects, Device Packaging, Power Applications.

1 Introduction

Power level requirements and switching frequency are continually increasing in the power electronic industry. This demands larger discrete devices and larger multi chip modules or   series / parallel combination of these, with faster switching speed. Today, MOSFETs, IGBTs and Thyristors are the main devices used in many applications including power conversion and motor drives. Diagram 1 shows the family structure of power semiconductor devices, and diagram 2 shows the ratings of these devices. Due to their widespread use in industry and the inherently high operating stress conditions, assessment of their failure mechanisms and reliability is a key issue.

Power semiconductor packaging is complicated by several factors. These include:

− Large currents that flow into and out of the silicon chips and package,
− The high voltages between terminals,
− The amount of power which is dissipated as heat and
− The large temperature excursions that devices and packages can undergo during operation.

The reliability of any electronic package depends to a large extent on its construction. Electronic packages for discrete devices and power modules are composed of multilayer, dissimilar materials, which are joined together by different methods including solder and adhesive. The physical properties of various power semiconductor devices are shown in table 1. The difference in the coefficient of thermal expansion (CTE) causes these materials to expand and contract at different rates on heating and cooling. This is the main cause for the

bond thermal stresses observed after die attachment in surface mounted devices, as well as for thermal fatigue observed in intermediate soldered joints between the insulating substrate and the base plate in conventional power modules. Therefore, a key consideration in the packaging of devices is that bonds between different materials are able to sustain the mechanical and thermal stresses over its service life. Otherwise it fractures prematurely, terminating the functionality of the whole package.

In designing multi chip power modules, one must consider few critical issues such as package parasitic inductance and current sharing between chips within the module. Parasitic inductance is an immediate concern since it can have a significant influence on the switching losses due to voltage overshoot. Another area of concern is the uneven distribution of current between parallel chips within the modules and between parallel-connected power modules.

Conventionally, high power electronic packages are of a stack configuration with several silicon chips connected in parallel. The chips are soldered onto insulating substrates made of typically heat conductive ceramic (usually aluminium oxide Al2O3 or aluminium nitride ALN). These are sandwiched between two thin copper layers, and the entire assembly of the die and the direct copper bonded (DCB) is soldered to a copper base plate. Some surface mounted technologies use a thermally conductive epoxy to attach semiconductor die directly onto the lead frame. Typical example of this technology is the Smartpack module [1]. The entire structure is overmoulded in an epoxy resin (moulded encapsulation) that forms the package itself and provide the electrical insulation needed, thus avoiding the use of intermediate substrates. Recently, direct mounting on metallised Ceramic heat-sink has been proposed for low power semiconductor devices (CeramTec).

Any electronic package undergoes three types of thermal loading during its lifetime:

- Processing: Problems arising during processing may include some defects in the silicon chips themselves.
- Testing: Every product undergoes testing.
- Operation in the field: Service environment may include thermal cycling.

The block diagram in figure 1a shows a summary of the main sources of failures. Details of these failure types are given in the following section.

2 Failure Mechanisms

2.1 Failure mechanisms relating to the silicon chip

A considerable diffusion of heavy metals into the wafers can occur during the high temperature steps required for fabrication of power devices. This contamination can cause an increase in the recombination and generation rates of free charge carriers. Accordingly, both the on-state voltage and leakage current are increased.

Local carrier lifetime measurement on processed silicon wafers can be made by using the electrolytic metal tracer method. The principle is related to optical beam induced current (OBIC) in that hole–electron pairs are photo generated by a scanning laser beam, which diffuses through the semiconductor and are separated and collected in a space charge zone. The space charge region is created within the silicon wafer by contacting it with electrolytic cells on both sides and by biasing it to some suitable voltage. This method can be used for metal contamination monitoring as well as for the characterisation of defects introduced during the manufacturing process [2].

2.2 Oxide defects

During service, there is a possibility of degradation of the oxide film with time—time dependant dielectric breakdown. Since the gate oxide film of an MOS device is very thin, application of high voltages leads to breakdown, both electrical overstress and electrostatic discharge easily causing damage. Oxide film degradation depends largely on the intrinsic defect density in the gate oxide film. The oxide breakdown voltage and intrinsic defect density are affected by the gate electrode materials, film thickness, defects in the substrate, oxidation method and contamination. They are also affected by the three-dimensional structure of the gate area that is based on the design and fabrication process.

2.3 Ion migration

Contamination by alkali mobile ions introduced during the manufacturing process greatly affects the reliability of the devices. Application of an electric field may cause movement within the passivation oxide film, collection in the field region, gate oxide or around the PN junction, resulting in failures due

to parasitic MOS, Vth shift and breakdown voltage degradation.

2.4 Current crowding / filamentation

Current crowding may result from many sources including crystal defects and processing non-uniformities. When the power dissipated exceeds the rate at which the heat energy can be dissipated, a localised hot spot and thermal runaway may result causing a non-uniformity in the current density and enough local power dissipation to cause substantial temperature rise of the filament and finally melting the semiconductor and chip failure.

2.5 Back metal delamination

Stresses are inherently introduced into both the deposited layers and the underlying active chip area during back metal deposition. In order to prevent peeling during the manufacturing and/or during service, several design issues need to be considered. These include deposition conditions, surface conditions and correct layer thickness.

2.6 External impacts

Power semiconductor devices may experience sudden catastrophic failure during operation due to the interaction with cosmic rays. Burn out of the device starts with a local nuclear event and under certain circumstances the generated carriers can undergo a self supporting strong carrier multiplication [3, 4 and 5].

2.7 Operating conditions

Operating temperature
Low temperature operation of semiconductor devices in general causes the device to switch faster than high temperature with the result that inductive overshoot voltages rise and switching times and losses are usually reduced in magnitude. It is recommended that for low temperatures the circuit stray inductance is reduced, but if cannot be achieved, it is recommended to reduce di/dt's. The most likely device to fail at low temperature is the diode due to snappy recovery [6]. Diode losses increase considerably with temperature due to increases in Qrr and Irr which results in a rise in energy losses [7].

2.8 Operating frequency

The total losses are the sum of the conduction losses and the switching losses. The later, increase with the increase of frequency [8]. This causes an increase of temperature with the frequency.

2.9 Short circuit conditions

It is one of the most severe stress conditions on the device, since a large current flows through the device and if it continues over a long period of time, inevitably leads to its destruction. The challenge is to delay the failure of the device, so that detection and prevention can be done in time. A major advantage of IGBT circuits is that no passive dI/dt and dV/dt snubbers are required. dI/dt is limited only by the parasitic circuit inductance. Causes of short circuits:

– Chip failure due to thermal overload—wear out processes—fatigue.
– Chip failure due to operation outside specification–safe operating area.
– Chip failure due to current asymmetries.
– Chip failure due to cosmic ray impact.
– Dielectric insulation failure–over voltage or/and ageing processes—partial discharges.

2.10 The encapsulation

2.10.1 Cracking of wire bond

Wire bonding is the most common method for connecting the pads on the chip to those on the package. Thermal mismatch between the wire bond and chip generates a significant thermo-mechanical stress in the bonding zone. This results in fatigue crack propagation during thermal cycling. Also current pulsing results in a small flexing of the wire bond, resulting in a second-order fatigue failure, that of cracking at the heel of the wire. Reliability of this joint depends on bond-wire length and the loop height.

2.10.2 Partial discharge and insulation failure

This is also known as "The Corona Effect". It is a major cause of premature ageing of electrical insulation. It usually originates from a sharp point at the insulator edge or within the filling gel. Single or multiple root partial discharges may occur causing cumulative damage due to power dissipation in the surrounding material.

The lifetime of the electrical insulation is reduced proportionally to both the applied voltage gradient and its frequency [9, 10, 11and 12]. The voltage gradient is usually high because of thin insulation to minimise thermal resistance.

2.10.3 Delamination

Delamination of conducting layers may include copper tracks on the DCB substrate or layers of solder due to incorrect thickness or the presence of voids.

DCB-substrates, the heart of power modules have been increasingly used in power electronics. Al_2O_3 and AlN -DCB have become the preferred industry power substrates due to their performance and competitive prices. The high thermal conductivity of Al_2O_3 (24 W/m K) and that AlN (180 W/m K) combined with the high thermal capacity and heat spreading capability of thick copper (typically 0.2–0.3 mm) make the DCB the most popular material choice for power chip onboard assemblies. The critical area is the interface between the copper pattern and the ceramic. The difference in their thermal co-efficient of expansion [$\alpha_{th}(C_u)$=17 ppm/$_K$; $\alpha_{th}(Al_2O_3)$=7.1 ppm/$_K$; $\alpha_{th}(AlN)$=4.1 ppm/$_K$] leads to stress within the interface and in long term may destroy it. The key point in reducing this failure mode is to reduce this thermally induced stress. This could be achieved by etching defined holes at the edge of the copper pads, which can result in significant increase in the thermal cycling resistance.

2.10.4 Solder fatigue

Thermo-mechanical stresses are set up in the solder joint during thermal cycling as a result of thermal mismatch between the base plate and the ceramic tile. Fatigue occurs by multiple site fatigue crack initiation followed by growth within the solder layer adjacent to the base plate. Detailed study of the effect of solder fatigue on thermal performance and estimation of fatigue life time are given in Ref. [13]. Scanning acoustic microscopy (SAM) is an imaging technique for non-destructive internal sample inspection allowing the detection of voids, cracks and delamination in the package. Its principle is based on the reflection of ultrasonic waves at the internal interfaces in the sample. The core element of the microscope is the ultrasonic transducer that works as a generator and receiver of high frequency vibrations. The transducer emits a very short and focused acoustic pulse that travels through the coolant (usually water) and reaches the surface of the sample. A portion of the pulse is reflected at the surface and is received by the transducer as a first, strong echo pulse. However, a part of the sound wave penetrates into the sample and reflects at each subsequent internal interface, losing energy at each reflection. The technique is mainly used for assessing the quality of large area solder joints interconnected in modules during module manufacturing but also as a tool for monitoring the aging of solder joints in reliability tests.

3 Current sharing

When paralleling IGBT chips, it is desirable to have all the devices within the module to switch together and conduct equal amounts of current in order to avoid the risk of thermal runaway. To ensure this, devices must have "identical" output and transfer characteristics. Measures that can be addressed to minimise current missharing between chips is to match V_{th} and $V_{ce(sat)}$ to within 5%. In many applications in power electronic systems, successful paralleling of IGBT modules require care and adequate de-rating of the individual module [14 and 15].

Depending on the application the system designer has to consider a number of issues to ensure that the system is reliable. These issues include:
−   module characteristics
−   gate drive circuitry
−   thermal paths and circuit layout

The first step is to determine the optimum number of modules to be connected in parallel to obtain the required current rating for the system. Due to variations in module characteristics and circuit layout it cannot be assumed that the parallel connection of N modules each with a current rating of I amps will have a combined current rating of NI amps. For this reason it is necessary to de-rate the modules. The principle of de-rating module can be applied to an entire range of IGBT modules.

3.1 Static current sharing

When two or more IGBT modules are connected in parallel a current imbalance occurs due to the difference in the dynamic and static characteristics of the individual IGBT modules. In the steady state condition it is principally the difference in the output characteristics, which causes the current to divide unequally between the modules. This is illustrated in Figure 2, which shows that the device having the lower $V_{CE(sat)}$ (Q1) carries the largest portion of the total current.

If two modules of the same family type but with different $V_{CE(sat)}$ characteristics are connected in parallel the combined current rating is not twice the nominal current rating of the module (this assumes the current in neither module exceeds the nominal current rating). The reduction in effective current capability is known as the current de-rating factor. This is defined as:

$$\delta = 1 - \frac{I_T}{n_p \times I_M}$$

(1)

Where,
δ =De-rating factor,
I_T= total current sustainable by the parallel combination of modules,
I_M= nominal dc current rating of a single module,
n_p= number of modules in parallel.

Rearranging equation (1) we obtain:

$$I_T = (1 - \delta)n_p I_M \tag{2}$$

Thus knowing the de-rating factor for a number of modules in parallel, one can determine the total current that can be sustained by the parallel system. For a system of n_p parallel connected modules where none of them is to exceed the rated current, the worst case situation is when one of the devices is conducting the maximum rated current I_M and the remaining (n_p- 1) devices are each conducting some minimum current I_{min}. In this case the total current is given by:

$$I_T = I_M + (n_p - 1)I_{min} \tag{3}$$

Following on from the de-rating factor, it is possible to define in a similar way the amount of missharing between devices when connected in parallel. In this analysis the missharing factor is a measure of the maximum current difference compared to the maximum allowable current:

$$m = \frac{I_M - I_{min}}{I_M} . \tag{4}$$

Where
m = missharing factor
I_M= maximum allowable current for a single module operating alone
I_{min}= minimum current for a single module operating in a parallel connection.

We can express (4) as follows:

$$\frac{I_{min}}{I_M} = (1 - m) \tag{5}$$

From (1), (3) and (5) we have

$$\delta = m(1 - \frac{1}{n_p}) \tag{6}$$

The missharing factor m is an important module characteristic for parallel connected IGBTs and it is related to the spread in IGBT output characteristics ($DV_{CE(sat)}$) for a given device type. It is a function of saturation voltage $V_{CE(sat)}$,junction temperature, device design and technology. Figure 3 (which is a plot of equation (6)) illustrates the de-rating factors for the Dynex DIM800DDM17 IGBT module for up to 5 modules in parallel.

Note that de-rating is more severe at lower temperatures. For a worst case design it is advisable to use de-rating factors applicable at 25°C junction temperature. The total system current can be estimated for up to 5 modules in parallel by reading off a de-rating factor from Figure 3 and using equation (2). For example to estimate total current for a system of four DIM800DDM17 connected in parallel; read off from Figure 3 the de-rating factor at 25°C for 4 devices in parallel is 30%. Then from equation (2),

I_T = (1-0.3) x4x800 = 2240A

3.2 Dynamic Behaviour
In the static rating, a system of parallel-connected IGBT modules assumes that none of the devices in parallel combination carries current more than its rated value. A similar approach can be applied to parallel connected-IGBT modules in dynamic conditions. The main reason for current imbalance during switching (turn-on and turn-off) assuming ideal gate drive conditions and circuit layout is the difference in the transfer characteristics (collector current vs. gate-emitter voltage (V_{GE})) of the individual modules. Referring to Figure 4, if V_{GE} applied to each of the parallel modules is identical during the switching transitions, the current divides dynamically according to the transfer characteristics. The IGBT module with the "steeper" transfer characteristic carries the greater portion of the current and incurs the highest switching losses. The dynamic current rating (Ic_{-pk}) is related to the module rated junction temperature and hence to the total device losses. Thus the dynamic current rating depends on the specific application conditions.

If we define $Ic_{pk\ (max)}$ as the maximum allowable peak current for a single module operating alone in a specific application and $Ic_{pk(min)}$ as the minimum peak current for a single module operating in a parallel connection, then we can define the partial current DIc_{pk} as $Ic_{pk(max)} - Ic_{pk(min)}$ and the dynamic current mis-sharing factor by

$$j = DIc_{pk}/ Ic_{pk(max)} \tag{7}$$

Thus we can obtain the dynamic de-rating factor:

$$d \text{ (dynamic)} = j (1-1/n_p) \tag{8}$$

Where

d = dynamic de-rating factor
n_p = number of modules in parallel
j = dynamic mis-sharing factor.

The dynamic mis-sharing factor j is related to the transfer characteristics (Figure 4) i.e. the threshold voltage (V_{th}) and the gain (g_{fe}) of the IGBT as defined by the device manufacturers.

Figure 5 compares static and dynamic de-rating for DIM800DDM17 IGBT module at 25°C junction temperature and given operating conditions (in this case a PWM motor drive inverter). Note that the static de-rating factor is greater than the dynamic de-rating factor. This is true in general and so for most applications users need only consider the static de-rating factor.

3.3 External circuit influence on sharing

So far the effects of device characteristics on static and dynamic sharing have been considered. In practice the dynamic sharing is more sensitive to the external circuit factors, which also leads to parasitic oscillations. Figure 6 shows one example how unequal stray inductance in the gate-emitter loops produce dynamic imbalance due to unequal gate emitter voltages (V_{GE1} ¹ V_{GE2}) during switching transient. The use of separate gate resistors R_{G1} and R_{G2} (Fig.7) helps to restore the dynamic balance. IGBT modules have appreciable stray capacitance and can ring with stray circuit inductance especially during fast switching phase. These oscillations are avoided by careful circuit layout and reducing any stray inductance to practical minimum.

3.4 Temperature de-rating

The device thermal rating is another factor to consider when paralleling IGBT modules. This is quoted in terms of maximum junction temperature T_{jMAX}. The reliability of the device operation suffers adversely if operated beyond this temperature. The T_j of the device is calculated thus:

$$T_j = T_c + PR_{th\,j-c} \tag{9}$$

Where T_c is the device case temperature maintained by the thermal circuit (heat sinking); P is the power dissipated in the device and R_{thj-c} is the dc junction to case thermal resistance of the device. In steady state operation the power dissipation in the device is given by:

$$P = I_C V_{CE(sat)} = I_C(V_0 + r_0 I_C) \tag{10}$$

Where V_0 and r_0 are the parameters of the linearised output characteristics. $V_{CE(sat)}$ is temperature dependant and hence V_0 and r_0. If A is the temperature coefficient (TC) of r_0 and B is the TC of V_0 then

$$r_0 (T) = r_0(25°C)*(1+A(T-25°C)) \tag{11}$$

and

$$V_0 (T) = V_0(25°C)*(1+B(T-25°C)) \tag{12}$$

and from (10)

$$P(T) = I_C \quad V_0(25°C)×(1+B(T-25°C)) \quad + I_C^2 r_0(25°C)×(1+A(T-25°C)) \tag{13}$$

And hence the power dissipation is non-linear function of collector current.

When IGBT modules are paralleled, the mis-matched in $V_{CE(sat)}$ produces different partial currents and hence different power dissipation leading to different junction temperatures. The temperature de-rating is defined similar to current de-rating such that the total system current is adjusted to keep the junction temperatures of each device equal to or less than its rated value (e.g. 125°C). Thus:

$$\delta Tj = 1 - \frac{I_T}{n_p \times I_M} \tag{14}$$

Where,
Tj=Temperature de-rating factor,
I_T = total current sustainable by the parallel combination of modules,
I_M = nominal dc current rating of a single module,
n_p = number of modules in parallel.

Devices with positive TC have natural tendency to force share as they get hotter even they are not thermally coupled. This because a device with low value of $V_{CE(sat)}$ takes more current initially and heats up quickly. As the temperature increases, its V_{CE} also increases and thus forcing the current into the cooler device. This process continues until equilibrium is achieved.

4 Semiconductor Devices for Thermal Stress Relief

Electrical circuit breakers were developed to protect circuits against faults. They are required to control electrical power networks by switching circuits ON, carrying load currents and switching circuits OFF, to isolate them with manual or automatic operation.

Conventional circuit breakers, CCBs have been used for a long time for interruption of fault currents. Because of the thermal and electrical stresses inherent in opening and closing of conventional circuit breakers, such breakers have traditionally been very large and expensive devices, requiring expensive maintenance after a number of switching operations. Arcing which occurs across the contacts during interruption of fault current can damage contact electrodes and restricting nozzles [16]. For this reason conventional circuit breakers require frequent inspection and expensive maintenance. The problem of arcing becomes very acute for breaker applications where high switching frequency is required such as conveyor drives, industrial heaters, test beds etc.

In the last few decades a great progress has been achieved in the performance characteristics of conventional circuit breakers (CCBs) in respect of their voltage ratings, breaking capacities and speed of operation. In spite of that, the basic principle of conventional electromechanical circuit breaker technology has changed very little in more than 50 years. The main reason for its continuing popularity is its good reliability.

4.1 There are three basic requirements that a circuit breaker must meet:
1) It must conduct service load currents with minimal power loss.

2) It should be capable of fast transition to its blocking state without damaging itself in the process.

3) It must block any current from flowing when it is open, despite the high voltage across its terminals.

The conventional mechanical circuit breaker gives excellent results for the first and third of these requirements, but it could fail in the second due to transient conditions of the switching circuits.

4.2 Types of Traditional Circuit Breakers
1) Air-Break Circuit Breaker (CB): This type of breaker operation depends on the transfer of the arc to large splitter plates where the arc is extended in air until it collapses.

2) Air-Blast CB: It is constructed in such a manner that its contacts are of a fixed tubular construction with a moving rod pushed down through the middle to complete the contact. On opening, a blast of air is forced into the breaker to blow out the arc. An interlock is built into the system to ensure the breaker does not open when there is low air pressure. The main problem with this CB is the large size.

3) Sulphur Hexafluride (SF_6) CB: This type is similar in principle to the air-blast CB except that instead of compressed air, SF_6 gas is used. Because of the use of this gas a requirement is needed not to blow the gas out into the atmosphere but back into the system. This need for a gas tight construction, not only increases the difficulty of maintenance, but also increases the complexity and cost of the device.

4) Oil CB: The main contacts are immersed in oil to reduce the size and cool the arc. The main problem is the risk of explosion and fire.

5) Vacuum CB: The idea behind this type is that putting the contacts in vacuum, there is no ionisation gas to form arc plasma. The main problems are the production and maintenance of a high vacuum and the problem of contact bounce and welding together, as no oxide films forms in vacuum.

Looking at the various types of circuit breakers, the problems of arcing and maintenance immediately spring to mind. Also the size, cost and reliability are other important factors that need looking into. Engineers have speculated for many years about the possibility of replacing the existing conventional circuit breaker designs with new designs using semiconductor devices.

5 Solid-State Circuit Breakers

Over the last few years, power semiconductor devices have evolved to a point where a single device can carry few thousands of Amps and can block few thousands of Volts. The feasibility of using semiconductor devices for circuit breaker applications was examined by many workers [17, 18, 19].

Semiconductors switching devices have many advantages

which include fast switching operation (High frequency applications) and low maintenance. Due to the absence of moving parts there is no arcing, contact bounce or erosion. Recently, considerable progress has been made in the development of low power solid-state breakers for AC and DC applications [17, 18,19]. The main disadvantage of the solid-state breaker is the high thermal losses generated by the continuous load current.

Electronic switching devices, such as thyristors and GTO's, always have some voltage drop across their terminals resulting in heating through the I^2R Loss. At very high currents, the electromechanical breaker remains firmly established, with no short-term likelihood that the solid-state breaker replacing it. A hybrid form of switch has emerged which marries the advantages of both, see Figures (8) and (9).

6 Hybrid Circuit Breaker

The continuous current is handled by the conventional breaker, whereas the make and break processes are handled by power semiconductor devices (thyristors) connected in parallel with the breaker contacts. When switching on, the thyristors are fired first, these carry the inrush current and prevent arcing. As soon as the main contacts close, the contact resistance is lower than the resistance of the semiconductors, and consequently the current will commutate to the contact path. The continuous current is now carried by the breaker with negligible losses.

On disconnection, the thyristors are fired and the current will again pass through the thyristors because the resistance of this current path is lower that the resistance of the arc path. Again the arc will almost be eliminated and the thyristors will eventually block the voltage.

A single-phase hybrid model circuit breaker has been demonstrated using thyristors [20].
Similar work with using Insulated Gate Bipolar Transistors (IGBTs) instead of thyristors in the Hybrid Circuit Breaker (HCB) has been done and results are presented in figures (10 –16). The main power handling limitations here are the maximum current and voltage ratings of the devices in parallel with the conventional breaker.
Figures (8 and 9) shows the HCB circuit layout and block diagram of the whole system. Figures (10,11, and 12) shows the CB feeding different type of loads without the parallel IGBT, and the effect of arcing is clearly evident on the voltage waveform. Figures (13,14, and 15) shows the corresponding cases with IGBT in parallel with CB. It can be clearly seen that the arc has been eliminated and no noice present on the voltage waveform.

7 High Power Hybrid Circuit Breaker

For these applications, devices need to be connected in series (for high voltage) and in parallel (for high current).

In series operation of power semiconductor devices the important issue is to maintain equal blocking voltage sharing among devices in the series string during the steady state as well as during the transient state. Since voltage unbalance is due to device parameter spread and gate drive delays, careful selection of devices which has low parameter spread and synchronising gate drive signals will minimise the problems associated with series connection. In practical situations this is rather impossible and therefore different mitigation techniques have been developed for different power devices.
Successful paralleling of devices requires care and adequate de-rating due to variations in device characterics and layout as discussed before.

Further details of problems encountered in series and parallel applications are given in reference [21] and [22] respectively.

8 Thermoelectric Cooling using Semiconductor Devices

The growing thermal management problem in microelectronics industry due to the continuing push for higher packing densities of semiconductor devices in Giant Scale Integrated Circuits (GSI) has forced designers to search for new cooling methods.

The concept of thermal management in microelectronics circuits is changing, and the potential for solid-state cooling to solve heating problems is emerging. In the past many electrical and electronic circuits are cooled by forced air produced by electric fans. These are usually bulky, noisy, inefficient, and could be the source of failures in electronic circuits due to imported dust and other particles into the system which cause short circuits.

Recent advances in thermoelectric Peltier devices and associated capabilities to shrink thermoelectric modules enabled new solutions for microelectronic circuits cooling [23]. Two approaches for implementation for thermoelectric cooling are possible:

– Targeted (Hotspot) cooling; in this option only the hottest spots on the silicon chip is cooled (Sometimes well below ambient temperatures to increase clock speed). The coefficient of performance is not critical because small fraction of total chip power is handled.

– Management of entire chip load - thermoelectrically enhanced heat sink. In this case the energy efficiency (Coefficient of Performance – COP) is of paramount importance and industry is not receptive to designs that

greatly increase the total heat load that must be dissipated by the heat sink.

9 Conclusion

An overview of thermal issues and, failure mechanisms in power semiconductor devices are presented. Failures related to silicon chip, package structure, operating conditions and other external factors are discussed. The role of power semiconductor devices in thermal management is explored. The main advantage of using power semiconductor devices in circuit breaker applications is that the effect of arcing could be eliminated completely. This leads to major improvements which include:

- – Reduction of size and weight,
- – Reduction of pollution,
- – Improved speed of operation and
- – Improved efficiency

Peltier semiconductor devices can be used in many other applications for both heating and cooling systems.

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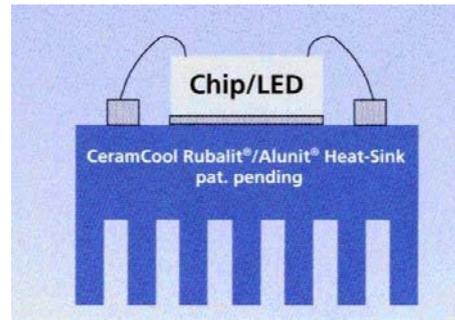
Fig. 1c: Ceramic Heat-Sink
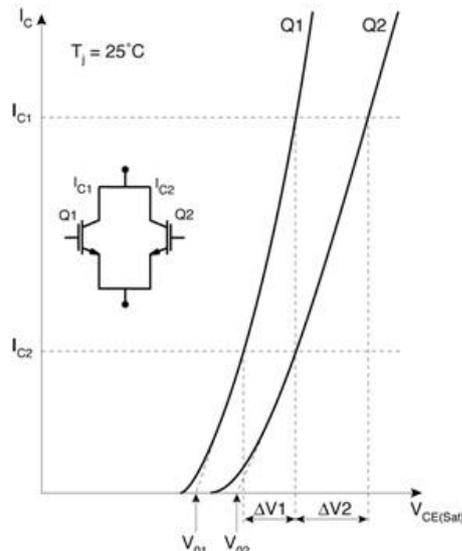
Fig. 2: IGBT module output characteristics
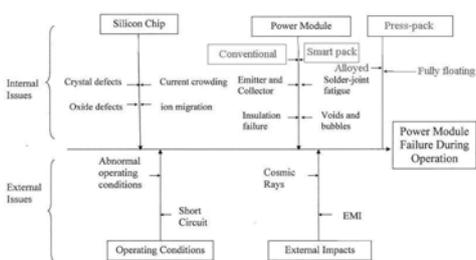
Fig. 1a: Potential Failure in Power Modules and Discrete Devices

Fig. 3: Static de-rating factor vs number of DIM800DDM17-A000 IGBT modules in parallel

Fig. 1b: Simplified model of a SmartPack
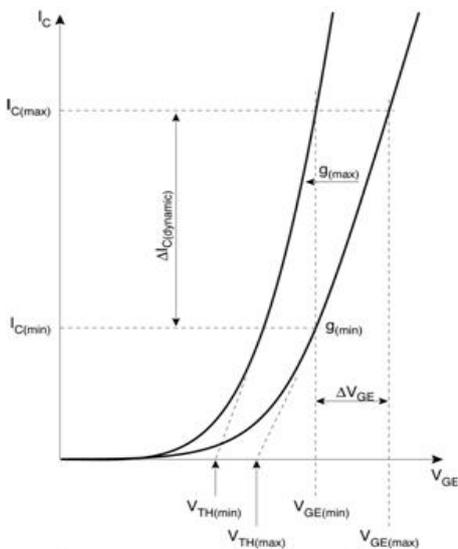
Fig. 4: IGBT module transfer characteristics

Fig. 5: Comparison of static and dynamic factors for DIM800DDM17-A000

Fig. 6: Static and dynamic collector current de-rating imbalance for two DIM800DDM17-A000 modules in parallel. Vertical scale 100A/div Horizontal scale 100us/div

Fig. 7: Use of R_{g1} and R_{g2} to restore dynamic balance
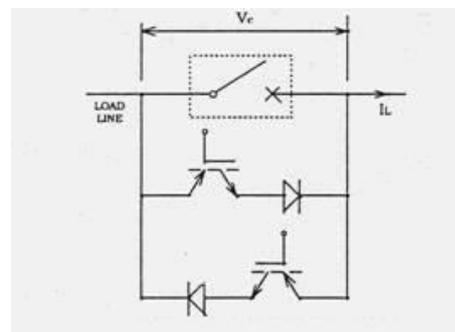
Fig. 8: Hybrid Circuit Breaker Configuration
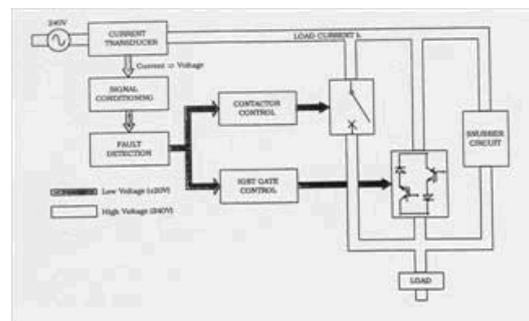
Fig. 9: Hybrid Circuit Breaker Configuration
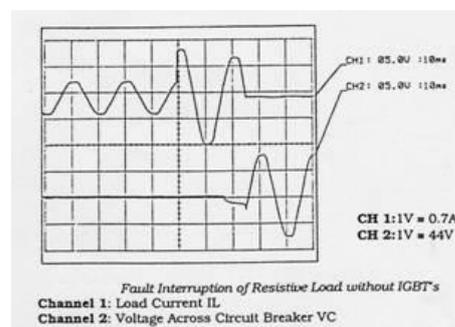
Fig. 10: Fault Interruption of Resistive load without IGBTs
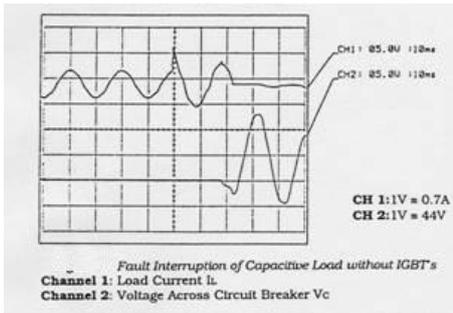
Fig. 11: Fault Interruption of Capacitive load without IGBTs

Fig. 12: Fault Interruption of Inductive load without IGBTs

Fig. 13 Fault Interruption of Resistive load with IGBTs
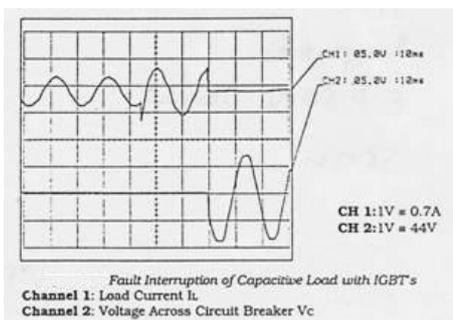
Fig. 14: Fault Interruption of Capacitive load with IGBTs

Fig. 15: Fault Interruption of Inductive load with IGBTs

Fig. 16: IGBT Gate Pulse on Fault Interruption
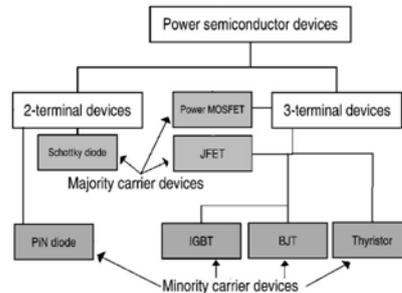
Diagram 1: Family structure of Power Semiconductor Devices
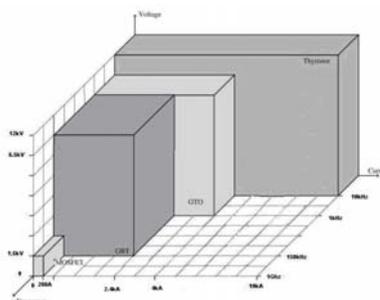
Diagram 2: Ratings of Power Semiconductor Devices

Material	E_g (eV) @300K	μ_n(cm²/V.s)	μ_p(cm²/V.s)	V_{sat} (cm/s)	E_c (V/cm)	λ.(W/cm.°K)	ε_r
Si	1.12	1450	450	10^7	3×10^5	1.3	11.7
3C – SiC	2.3	1000	45	2.5×10^7	2×10^6	5	9.6
6H – SiC	2.9	415	90	2×10^7	2.5×10^6	5	9.7
4H - SiC	3.2	950	115	2×10^7	3×10^6	5	10
GaAs	1.4	8500	400	2×107	4×105	0.54	12.9
GaN	3.39	1000	350	2×10^7	5×10^6	1.3	8.9
GaP	2.26	250	150		10^7	1.1	11.1
Diamond	5.6	2200	1800	3×10^7	5.6×10^7	20	5.7

Table 1: Physical properties of materials used for Power Semiconductor Devices