# Simulation of Meshes and Tori in an asymmetric Faulty Incrementally Extensible Hypercube with Unbounded Expansion 

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#### Abstract

The paper considers the problem of finding meshes and tori in a Faulty Incrementally Extensible Hypercube if any. We develop novel algorithms to facilitate the embedding job when the Incrementally Extensible Hypercube (IEH) contains faulty nodes. We present strategies for reconfiguring a mesh or tori in an IEH with unbounded expansion. These simulation approach shows a mesh or torus can be embedded into a faulty IEH $G_{n}(N)$ with load 1 , congestion 1 and dilation 3 such that $O\left(n^{2}-L \log _{2} m ل^{2}\right)$ faults can be tolerated. Furthermore, the technology can be apply in grid computing and cloud computing.


Key-Words: - Incrementally Extensible Hypercube (IEH), hypercube, mesh, torus, embedding, expansion

## 1 Introduction

Rapidly advancing technology has made it possible for a large number of processing elements to be interconnected in a variety of configurations. In the investigation of parallel computing, networks of processors are often organized into various configurations such as hypercubes, trees, rings, and meshes. These configurations can be presented as graphs. If the properties and structures of the underlying graph are used effectively, the computations and communication speeds can often be improved. Many parallel algorithms have been designed to solve different problems on various networks. It would be of interest to be able to execute these algorithms in other networks. Therefore, the problem of simulating one network by another is modeled as a graph embedding problem where nodes and edges in the graph represent the processors and communication links between processors. Organizing computations in a network of processors is also modeled as a graph embedding. So, graph embedding problems become the important applications in a wide variety of computational situations.

The problem of embedding an $n$-processor guest network $G$ into an $n$-processor host network $H$ is an important problem in distributed computing or parallel processing. Results on this problem not only demonstrate computational equivalence or non-equivalence) between networks of different topology, but also lead to efficient simulations of
algorithms originally designed for $G$ on host $H$. Embedding and their implications to distributed computing or parallel processing have been studied extensively recently.

An embedding of a graph $G=\left(V_{G}, E_{G}\right)$ into a graph $H=\left(V_{H}, E_{H}\right)$ includes a mapping of nodes of $V_{G}$ into nodes of $V_{H}$ and a mapping each edge of $E_{G}$ into a path of $H$. The graph $G$ and $H$ are referred as the guest and host graphs. Four common measures of quality of an embedding in parallel processing are dilation, expansion, congestion and load. The dilation measures the communication delay and is defined as the maximum length of paths mapping by edges of $E_{G}$. The processor utilization is measured by the expansion that is defined as the ratio of total number of nodes of $G$ to total number of nodes of $H$. The congestion of an embedding is the maximum number of edges of the guest graph $G$ that is mapped by a single edge of the host graph $H$. The congestion is a measurement of queuing delay of massages. To measure the processing time of tasks is referred as the load in an embedding. The load is the maximum number node of $G$ that is embedded in a single node of $H$.

From the computational perspective, hypercube multiprocessors have recently offered a cost effective and feasible approach to supercomputing through parallelism at the processor level by directly connection a large number of low-cost processors with local memories which communicate by message-passing instead of shared variables. Therefore, hypercubes are widely used
interconnection architectures in parallel machines. Hypercube has been the focus of researches in parallel computing because of its well-defined properties with the modularity, regularity, and low diameter, etc. These characteristics make it easy to design efficient parallel programs and share machines among users. Its important advantages are high data bandwidth and low message latency. Moreover, the hypercube may contain many other networks as its subgraphs such as rings, trees, meshes, etc. On the other hand, lots of interconnection networks can be mapped into the hypercube. It is apparent to demonstrate how all of the parallel algorithms, designed by those interconnection networks, can be directly implemented on the hypercube without significantly affecting the number of processors or the computation time.

A hypercube, also known as a binary $n$-cube or cosmic cube, contains $2^{n}$ processors (nodes), each of which is connected by fixed communication paths (links) to $n$ other nodes. The value $n$ is known as the dimension of the hypercube. In a hypercube, two nodes are connected if and only if their addresses differ by one and only one bit. Extensive research efforts have been focused on hypercube design aspects and hypercube applications such as data permutation and matrix operations. These have resulted in several commercial products, such as the Intel iPSC and the Connection Machine. However, the number of nodes of this network is restricted to be a power of 2 , that can be, in some situations, a significant drawback. In fact, to upgrade a hypercube it is necessary to double the number of processors, which can be unrealizable for budget limitations and for technical reasons. Several hypercube-like networks that can be constructed for any number of nodes have been proposed, such as Incomplete Hypercube[14], Supercube[28, 29], Flexible Hypercube[11], Incrementally Extensible Hypercube[31, 32], and so on.

The Incrementally Extensible Hypercube (IEH) graph is a new topology of interconnection networks and proposed recently. Unlike the hypercube, the IEH graph is incrementally extensible, that is, any number of nodes can construct it. Besides, it has the optimal ability of the fault tolerance and the diameter of logarithmic in the number of nodes. The difference between the maximum and the minimum degree of nodes in an IEH graph is at most 1 , so it is enough to say that the IEH graph is almost regular. However, the IEH graph does not have the drawbacks of the above-mentioned generalizations of the hypercube. The characteristics of IEH graphs are shown in [31].

Among the static interconnection networks used for SIMD[26] computers with an array of processors[2], one of the oldest and very popular architectures is a two-dimensional-mesh. Many important algorithms for solving various problems, e.g., matrix operations, simultaneous linear equations, graph-theoretic and image processing problems, etc., have been efficiently mapped in this mesh architecture.

In this paper, we study how algorithms that are designed for fault-tolerance Incrementally Extensible Hypercube can be implemented on Incrementally Extensible Hypercubes that contain faults. In the following discussion we will consider a parallel computer as a graph, in which the nodes correspond to processors and the edges correspond to communication links.

Also, we developed the methods for finding meshes or tori in an IEH graph. As the result, we can transit the parallel algorithms developed under the structure of meshes or tori to the IEH graph. This simulation approach enables extremely high-speed parallel computation in IEH graphs. Although IEH graphs are not absolutely asymmetric, it has the same power as the hypercube in terms of meshes and tori.

The remainder of this paper is organized as follows. Section 2 is devoted to some notations and definitions. The construction of the mesh in an IEH is addressed in Section 3. Section 4 develops the embedding algorithm to a faulty IEH with unbounded expansion. Section 5 concludes this paper.

## 2 Preliminaries

This section briefly describes notations and definitions of the IEH graph. The IEH graph of $n$-dimension is the composition of some $m$ different hypercubes of dimension $k$, where $0 \leq k \leq n$ and $l \leq m \leq n$. Let $G_{n}(N)$ be a $n$-dimensional IEH graph with $N$ nodes, and $N$ can be expressed by the binary string $N=b_{n} b_{n-1} b_{n-2} \ldots b_{l} b_{0}$, and $b_{i} \in\{0,1\}$. Suppose that hypercube $H_{i}$ is a part of the IEH graph $G_{n}(N)$, it is certain that the $i_{t h}$ bit of $N, b_{i}$ must be $l$. That is, an IEH graph $G_{n}(N)$ is composed of some different hypercubes which have lower dimension than $G_{n}(N)$ has. For example, $G_{3}(13)$ is an IEH graph contains 13 nodes, and it is composed by three different-sized hypercubes $H_{0}, H_{2}$, and $H_{3}$ because $13=1101$, and $b_{0}=b_{2}=b_{3}=1$.

Accordingly, the IEH graph is composed of some hypercubes, so there is a new type of connections beside the usual connections in a hypercube. These edges (or links) are used for
connecting two hypercubes are called Inter-Cube or $I C$ edges. For any given $N, 2^{n} \leq N<2^{n+1}$, the steps of finding IEH graphs are as follows.

Step 1 Build subcube graphs. Express $N$ as $(n+1)$ bits a binary number as $N=b_{n} b_{n-1} b_{n-2} \ldots b_{1} b_{0}$, where $b_{i} \in\{0,1\}$ and $b_{n}=1$ since $N \geq 2^{n}$. For each $b_{i}$, $b_{i} \neq 0$, construct a hypercube graph $H_{i}$ with $2^{i}$ nodes.

Step 2 Label the nodes. Note that each node has a $(n+1)$-bit binary label. Each hypercube $H_{i}$ is labeled as $11 \ldots 10 b_{i-1} b_{i-2} \ldots b_{1} b_{0}$. Obviously each hypercube of dimension $i$ (having $2^{i}$ nodes) have $i$ number of dashed and the individual nodes of the hypercube can be obtained by filling the dashes with 0 or $l$ in all possible ways. In other words, the binary representation of each node in $H_{i}$ has the same prefix of ( $n-i)$ l's followed by a single zero.

Step 3 Construct the incremental hypercube in steps by providing the inter-cube edges. Find the minimum $i$ such that $b_{i} \neq 0$. Set $j=i$ and $G_{j}=H_{i}$.

Set $i=i+1$.
While $i \leq n$ do
if $b_{i} \neq 0$ then
if $i-j=1$ then
each node $x$ in $G_{j}$ with label $11 \ldots b_{j} b_{j-1} \ldots b_{0}$ is connected to the node $11 \ldots 10 b_{j} b_{j-1} \ldots b_{o}$ of $H_{i}$.
else
each node $x$ in $G_{j}$ with label $11 \ldots l b_{j} b_{j-1} \ldots b_{0}$ is connected to $(i-j)$ different nodes of $H_{i}$ chosen in the following way:

Set $j=i$ and set $G_{j}$ to be the composite graph generated in the previous steps. Note that $G_{j}$ has now $\sum_{k=0}^{j} b_{k} 2^{k}$ nodes and the binary label of each node in $G_{j}$ has a prefix of $(n-j)$ l's.

$$
i=i+1
$$

Return $G_{n}$ as the desired incremental hypercube graph of $N$ vertices.

Figure 1 shows the example of $G_{3}(13) . G_{3}(13)$ consists of three subcubes. The three subcubes are 0 -subcube $\left(H_{0}\right), 2$-subcube $\left(H_{2}\right)$, and 3 -subcube $\left(H_{3}\right)$. Nodes 14 is the single node in $H_{0}$, Nodes $8,9,10$, and 11 are composed as a 2 -subcube $\left(H_{2}\right)$, and nodes $0,1,2,3,4,5,6$ and 7 are the elements of a 3 -subcube $\left(H_{3}\right)$. The edges $(8,14)$, $(10,14)$ are IC edges connected between $H_{0}$ and $H_{2}$ such that $H_{0}$ and $H_{2}$ are connected to be an IEH graph containing 5 nodes $\left(G_{2}(5)\right)$. In addition, the $H_{3}$ connects to $G_{2}(5)$ with these IC edges $(0,8),(1,9),(2,10),(3,11)$, and $(6,14)$.
Definition 1[19] The Hamming distance between two nodes with labels $x=x_{n-1} x_{\mathrm{n}-2} \ldots x_{0}$ and $y=$ $y_{\mathrm{n}-1} y_{\mathrm{n}-2} \ldots y_{0}$ is defined as
$H D(x, y)=\sum_{i=0}^{n-1} h d\left(x_{i}, y_{i}\right)$, where
$h d\left(x_{\mathrm{i}}, y_{\mathrm{i}}\right)=\left\{\begin{array}{l}0, \text { if } \mathrm{x}_{\mathrm{i}}=\mathrm{y}_{\mathrm{i}}, \\ 1, \text { if } \mathrm{x}_{\mathrm{i}} \neq \mathrm{y}_{\mathrm{i}} .\end{array}\right.$
Definition 2[19] Let $x=x_{n-1} \ldots x_{0}, y=y_{n-1} \ldots y_{0}$, then $\operatorname{Dim}(x, y)=\left\{i\right.$ in $\left.(0 \ldots n-1) \mid x_{i} \neq y_{i}\right\}$
Definition 3[1] If $G$ is a graph, the vertex set of $G$ is denoted by $V$ and the edge set of $G$ is denoted by $E$. A graph $G^{\prime}$ is said to be a subgraph of $G$ if $V^{\prime} \subseteq V$ and $E^{\prime} \subseteq E$.
Definition 4[16] $m_{1} \times m_{2}$ mesh or torus, denoted by $M_{m_{1} \times m_{2}}$, is a 2-dimensional mesh or torus, where $m_{1}=2^{r}, m_{2}=2^{s}$.
Definition 5[16] Any $m_{1} \times m_{2} \times \cdots \times m_{d}$ mesh or torus, denoted by $M_{m_{1} \times m_{2} \times \cdots \times m_{d}}$, in the $d$-dimensional space $R_{d}$, where $m_{i}=2^{p_{i}}$.
Definition 6[19] The Binary-Reflected Gray Code (BRGC) is defined recursively as follows.
$\mathrm{C}_{n+1}=\left\{0 \mathrm{C}_{n}, 1\left(\mathrm{C}_{n}\right)^{R}\right\}$, where $\mathrm{C}_{1}=\{0,1\}$ and $\mathrm{C}_{2}=\left\{0 \mathrm{C}_{1}, 1\left(\mathrm{C}_{1}\right)^{R}\right\}$
For example, a 2 -bit Gray Code can be constructed by the sequence, defined in definition 6 , and insert a cipher in front of each codeword in $\mathrm{C}_{1}$, then insert an one in front of each codeword in $\left(\mathrm{C}_{I}\right)^{R}$. We get the code $C_{2}=\{00,01,11,10\}$. Now, we can then repeat the procedure to built a 3 -bit Gray Code, and also get the code $C_{3}=0 C_{2} \cup 1\left(C_{2}\right)^{R}=\{000,001$, $011,010,110,111,101,100\}$.


Fig. 1 The IEH graph contains 13 nodes

## 3 Meshes and Tori Embedding

The section describes the representation used to solve that embeds a mesh and torus in an IEH.
Lemma $1 m_{1} \times m_{2}$ mesh or torus, denoted by $M_{m_{1} \times m_{2}}$, is a 2 -dimensional mesh or torus, where $m_{1}=2^{r}, m_{2}=2^{s}$ can be embedded in an $n$-dimensional hypercube where $n=r+s$.
Lemma 2 Any $m_{1} \times m_{2} \times \cdots \times m_{d}$ mesh or torus, denoted by $M_{m_{1} \times m_{2} \times \cdots \times m_{d}}$, in the $d$-dimensional space $R_{d}$, where $m_{i}=2^{p_{i}}$ can be embedded in an $n$-dimensional hypercube where $n=p_{1}+p_{2}+\ldots+p_{d}$. The numbering of the mesh or torus nodes is any numbering such that its restriction to each $i_{\mathrm{th}}$ variable
is a Gray sequence which is described in definition 2. Note that the assumption that all $m_{i}$ 's be power of 2 .

Our proposition is best illustrated by an example. Consider a $\mathrm{M}_{2 \times 2}$ mesh or torus i.e., $d=2, p_{1}=1, p_{2}$ $=1, n=p_{1}+p_{2}=2$. A binary number $H$ of any node of the 2-dimensional hypercube can be regarded as consisting of two parts: its first $l$ bit and its last $l$ bit, which we write in the form $H=X_{1} Y_{1}$, where $X_{i}$ and $Y_{i}$ are bits 0 or 1 . It is clear from the definition of an $n$-dimensional hypercube ( with $n=2$ ) that when the last $l$ bit is fixed, then the resulting $2^{p_{1}}$ nodes form a $p_{l}$-dimensional hypercube ( with $p_{l}=1$ ). Whenever we fix the first 1 bit we obtain a $p_{2}$-dimensional hypercube. The embedding then becomes clear. Choosing a 1 -bit $B R G C$ for the $x$
direction and $l$-bit $B R G C$ for the $y$ direction, the point $\left(x_{i}, y_{i}\right)$ of the mesh or torus is assigned to the node $X_{1} Y_{l}$ where $X_{1}$ is the 1 -bit $B R G C$ for dimension
of $p_{1}$ while $Y_{l}$ is the 1 -bit $B R G C$ for dimension of $p_{2}$. Herein, we illustrate the result of the mesh or torus in Figure 2.

mesh
$v=X_{n} \ldots X_{w-1} X_{w-2} \ldots X_{1} X_{0}$
$v^{\prime}=X_{w-1} X_{w-2} \ldots X_{1} X_{0}$
$v^{\prime} \in V^{\prime}$ can be embedded in $V$ denote as $v=0 \ldots 0 X_{w-1} X_{w-2} \ldots X_{1} X_{0}$
Theorem 1 A $M_{2^{r} \times 2^{s}}$ 2-dimensional mesh or torus can be embedded in an IEH $G_{n}(N)$ where $r+s=\left\lfloor\log _{2} N\right\rfloor$ with load 1 , dilation 1 , congestion 1 , and expansion 2.
Proof: This is trivial by lemma land the above simulation approach.
Theorem 2 Any $M_{m_{1} \times m_{2} \times \cdots \times m_{d}} d$-dimensional mesh or torus, where $m_{i}=2^{p_{i}}$ can be embedded in an IEH $G_{n}(N)$, where $\mathrm{p}_{1}+\mathrm{p}_{2}+\ldots+\mathrm{p}_{\mathrm{d}}=\left\lfloor\log _{2} N\right\rfloor$ with load 1 , dilation 1 , congestion 1 and expansion 2 .
Proof: It is trivial by lemma 2 and the above simulation approach.

This is the best illustrated by an example in Figure 3. That is a $\mathrm{M}_{2 \times 2}$ mesh or torus can be embedded in an IEH $G_{3}(13)$.
Lemma 3 A mesh or tori contains any number of nodes can be embedded into an IEH graph with load 1 , congestion 1 , and dilation 1 .


Fig. 3 Embedding of a $\mathrm{M}_{2 \times 2}$ mesh and torus in an IEH $G_{3}(13)$

## 4 Fault-Tolerant mapping Unbounded Expansion

In the previous section, we have constructed a mesh and a torus in an IEH graph. In the section, we consider a faulty IEH with unbounded expansion embedding.
Theorem 3 A mesh or a tori can be mapped into an IEH graph with unbounded expansion.
Proof: It is trivial by lemma 3.
The cardinality of $H_{i}$, denoted by $\left|H_{i}\right|$, is number of nodes in $H_{i}$. Similarly, $\left|G_{n}(N)\right|$ is number of nodes in the IEH graph $G_{n}(N)$.
Theorem 4 Suppose $G_{n}(N)$ is an IEH graph contains $N$ nodes, $H_{n}$ is the maximal hypercube exists in $G_{n}(N)$, then $\left|H_{n}\right|>\left(N-\left|H_{n}\right|\right)$. On the other hand, if $G_{n}(N)$ is divided into two parts, $H_{n}$ and $G_{m}\left(N-\left|H_{n}\right|\right)$,
$H_{n}$ contains more nodes than $G_{m}\left(N-\left|H_{n}\right|\right)$ does, where $0 \leq m<n$.
Proof: Let $G_{n}(N)$ be an IEH graph contains $N=\left(a_{n-1} a_{n-2} \ldots a_{0}\right)$ nodes. It is composed by hypercubes $H_{i}$ if $a_{i} \neq 0$ for $0 \leq i \leq n$. It is necessary that the most significant bit $a_{n-1}$ must be equal to $l$, so $H_{n}$ is a part of $G_{n}(N)$ Because $H_{n}$ is an $n$-dimensional hypercube, $\left|H_{n}\right|=2^{n}$. The rest part of $G_{n}(N)$ is $G_{m}\left(N-\left|H_{n}\right|\right)$ which is possibility composed by $H_{0}, H_{l}, \ldots$, and $H_{n-1}$ if it is greatest, so the maximal number of nodes in $G_{m}\left(N-\left|H_{n}\right|\right) \quad$ is $\left|H_{0}\right|+\left|H_{1}\right|+\left|H_{2}\right|+\ldots+\left|H_{n-1}\right|=2^{0}+2^{1}+\ldots+2^{n-1}=2^{n}-1$. As the result, $2^{n}=\left|H_{n}\right| \geqslant\left(N-\left|H_{n}\right|\right)=2^{n}-1$.
Theorem 5 For an IEH $G_{n}(N)$, the nodes of the subgraph $H_{n}$ has an IC edge at least.
Proof: By the construction of IEH and theorem 4, all
of nodes of $G_{m}(N)$, where $m<n$, has a unique IC edges connecting to $H_{n}$ at least. Therefore, the nodes of the subgraph $H_{n}$ of an IEH $G_{n}(N)$ have an IC edge at least.

## Algorithm Mesh_Mapping(x)

Input: $\quad x \quad / *$ the faulty node $* /$,

$$
\begin{aligned}
& M_{m_{1} \times m_{2} \times \cdots \times m_{d}}\left(m_{i}=2^{p_{i}}\right) \\
& G_{n}(N)\left(2^{n} \leq N<2^{n+1}\right) \\
& \forall p_{1}+p_{2}+\ldots+p_{d}=w, w \leq n \\
& p_{1}, p_{2}, \ldots, p_{d} \geq 1
\end{aligned}
$$

Output: $y \quad / *$ the replaceable node*/

$$
i=0 ; j=0 ; k=0
$$

Create a Queue $Q ; Q=\Phi$
if a node $x$ is faulty
then
\{
while $\left.i<\left(n+1-\angle \log _{2} m\right\rfloor\right)$ do
\{
search the node $y$
$H D(x, y)=1, \operatorname{Dim}(x, y)=\left\lfloor\log _{2} m\right\rfloor+i^{*} /$
if $y$ is not a virtual node and it is free
10. then
11. return $(y)$ /*replace $x$ with $y^{* /}$
12. remove all nodes in $Q$
13. exit()
14. else
15. enqueue( $\left.y,\left\lfloor\log _{2} m\right\lrcorner+i\right)$
$i=i+1$
$\}$
\}
while $Q$ is not empty do
\{
dequeue ( $a, b$ )
while $j<b$ do
\{
search the node $z$
/* $H D(a, z)=1, \operatorname{Dim}(a, z)=j^{*} /$
if $z$ is not a virtual node and it is free
then
return(z)
/*replace $x$ with $y^{* /}$
remove all nodes in $Q$
exit()
$j=j+1$
\}
\}
search the node $y / *(x, y)$ is an IC edge*/
34. if $y$ is not a virtual node and it is free
35. then
36. return $(y)$ /*replace $x$ with $y^{* /}$
37. exit()
38. while $k<\left\lceil\log _{2} m 7\right.$ do
39.
40. search the node $z$

$$
/ * H D(z, y)=1, \operatorname{Dim}(z, y)=k^{*} /
$$

41. if $z$ is not a virtual node and it is free
42. then
43. return $(z)$
/*replace $x$ with $y^{* /}$
44. exit()
45. $k=k+1$
46. \}
47. return("Failure")
48. end

Finding the replaceable node as follows:
node $\left.0=0 X_{n-1} X_{n-2} \ldots X_{\left\lfloor\log _{2} m\right.}\right\lrcorner \ldots X_{1} X_{0}$
node $\left.1=0 X_{n-1} X_{n-2} \ldots X^{\prime} \log _{2} m\right\lrcorner \ldots X_{1} X_{0}$
node $2=0 X_{n-1} X_{n-2} \ldots X^{\prime} \log _{2^{m} /+1} X_{\left\lfloor\log _{2} m\right\rfloor} \ldots X_{1} X_{0}$
node $\left.\left(n-\left\lfloor\log _{2} m\right\rfloor\right)=0 X^{\prime}{ }_{n-1} X_{n-2} \ldots X_{\left\lfloor\log _{2} m\right.}\right\lrcorner \ldots X_{1} X_{0}$
node $\left(n-\left\lfloor\log _{2} m\right\lrcorner+1\right)=1 X_{n-1} X_{n-2} \ldots X_{\left\lfloor\log _{2} m\right\lrcorner} \ldots X_{1} X_{0}$
node $\left(n-\left\lfloor\log _{2} m\right\lrcorner+2\right)=0 X_{n-1} X_{n-2} \ldots X^{\prime}\left\lfloor\log _{2} m\right\rfloor \ldots X_{1} X^{\prime}{ }_{0}$
node $\left(n-\left\lfloor\log _{2} m\right\lrcorner+3\right)=0 X_{n-1} X_{n-2} \ldots X^{\prime}\left\lfloor\log _{2} m\right\lrcorner \ldots X^{\prime}{ }_{1} X_{0}$ !
node $\left(n-\left\lfloor\log _{2} m\right\lrcorner+1+\left\lfloor\log _{2} m \_\right)=0 X_{n-1} X_{n-2} \ldots X^{\prime}\left\lfloor\log _{2} m\right\rfloor\right.$
$X^{\prime}{ }^{\prime} \log _{2} m{ }^{\prime}-1 . . . X_{l} X_{0}$
node $\quad\left(n-\left\lfloor\log _{2} m\right\rfloor \quad+1+\left\lfloor\log _{2} m\right\rfloor+1\right) \quad=$
$\left.0 X_{n-1} X_{n-2} \ldots X^{\prime}{ }^{\prime} \log _{2} m\right\rfloor+1 \ldots X_{I} X^{\prime}{ }_{0}$
node $\left(n-\left\lfloor\log _{2} m\right\rfloor+1+\left\lfloor\log _{2} m\right\rfloor+2\right) \quad=$
$\left.0 X_{n-1} X_{n-2} \ldots X^{\prime}{ }^{\prime} \log _{2} m\right\lrcorner+1 \ldots X^{\prime}{ }_{1} X_{0}$
$\vdots$
node $\left.\left(n-\left\lfloor\log _{2} m\right\rfloor \quad+1+2 * \log _{2} m\right\rfloor\right)=$
$0 X_{n-1} X_{n-2} \ldots X^{\prime} \log _{2^{m} \_+1} X_{\log _{2} m-} X^{\prime} \log _{2} m \not-1 \ldots X_{1} X_{0}$
node $\left.\left.\left(n-\angle \log _{2} m\right\lrcorner+1+2 *<\log _{2} m\right\lrcorner+1\right)=0 X_{n-1} X_{n-2} \ldots X^{\prime} \log _{2}$
$\left.{ }_{m \_+1} X \log _{2^{m}}\right\lrcorner X X_{\left.\log _{2} m\right\lrcorner 1} \ldots X_{1} X_{0}$
node $\left.\left(\left(n-\angle \log _{2} m\right\lrcorner+1\right) *\left(\left\langle\log _{2} m\right\lrcorner+1\right)\right)+(1+2+\ldots+n)=$
$1 X^{\prime}{ }_{n-1} X_{n-2} \ldots X_{\log _{2}{ }^{m} \_-1} \ldots X_{1} X_{0}$
node
$\left.\left.\left(\left(n-L \log _{2} m\right\lrcorner+1\right) *\left(L \log _{2} m\right\lrcorner+1\right)+(1+2+\ldots+n)+1\right)=Y_{n} Y$
$\left.{ }_{n-1} Y_{n-2} \ldots Y_{\left\lfloor\log _{2} m\right.}\right\lrcorner \ldots Y_{1} Y_{0}$
(The IC edge connects node 0 and node $\left.\left.\left.\left(\left(n-<\log _{2} m\right\lrcorner+1\right) *\left(\log _{2} m\right\lrcorner+1\right)+(1+2+\ldots+n)+1\right)\right)$
node $\left.\left(\left(n-\log _{2} m\right\lrcorner+1\right) *\left(\log _{2} m\right\lrcorner+1\right)+(1+2+\ldots+n)+$
$\left.\left\lfloor\log _{2} m\right\lrcorner\right)=Y_{n} Y_{n-1} Y_{n-2} \ldots Y_{\left\lfloor\log _{2} m\right\lrcorner} \ldots Y_{I} Y^{\prime}{ }_{0}$ $\vdots$
node $\left.\left(\left(n-L \log _{2} m\right\lrcorner+1\right) *\left(L \log _{2} m\right\lrcorner+1\right)+(1+2+\ldots+n)+L l o$
$g_{2} m \_\oint=Y_{n} Y_{n-1} Y_{n-2} \ldots Y^{\prime} \log _{2} m \not-1 \ldots Y_{1} Y_{0}$

For the $\operatorname{IEH} G_{3}(13)$ as Figure 3, where the $\mathrm{M}_{2 \times 2}$ has been mapped in it. We give a simple example in this section to explain the operations of the Mesh_Mapping algorithm when the faulty nodes exist. The procedure for handling this faulty node straightforward.

1. If the node 0 is faulty, it visits or signals the node 4 , to check whether it is free or not. If it is, it terminates.
2. If not, insert the node 4 to the queue, and search the node 8 , to check whether it is free or not. If it is, it terminates.
3. If not, insert the node 8 to the queue, and delete the node 4 from the queue, search the node 5 , to check whether it is free or not. If it is, it terminates.
4. If not, search the node 6 , to check whether it is free or not. If it is, it terminates.
5. If not, delete the node 4 from the queue, search the node 9 , to check whether it is free or not. If it
is, it terminates.
6. If not, search the node 10 , to check whether it is free or not. If it is, it terminates.
7. If not, search the node 14 , to check whether it is free or not. If it is, it terminates.
8. If not, return("Failure").

Therefore, the whole searching path is listed as $\{4(0100), 8(1000), 5(0101), 6(0110), \quad 9(1001)$, 10(1010), 14(1110)\}.

In Figure 4, we assume that the node 0000 is faulty. We can find the six nodes in the sequence for replacing the faulty node.

We illustrate the search tree of finding a replaceable node in an IEH graph $G_{3}(13)$ as shown Figure 5.

Figure 6 shows the representation for Figure 5. In Figure 6, we have mapped these replaceable nodes into these idle nodes of the IEH graph $G_{3}(13)$.

Now, Figure 7 shows Mesh_Mapping() algorithm applied to the graph of Figure 4.


Fig. 4: Embedding of a $M_{2 \times 2}$ mesh and torus in a faulty IEH $G_{3}(13)$


Fig. 5 The search tree for finding the searching path by Mesh_Mapping $(x)$ algorithm
Second


Fourth
Fig. 6 Mapping Figure 5 into IEH $G_{3}(13)$


Fig. 7 Summary of Mesh_Mapping( $x$ ) algorithm applied to Figure 4

Theorem 6 A mesh or a torus $M_{m_{1} \times m_{2} \times \cdots \times m_{d}}$ can be mapped into a faulty IEH $G_{n}(N)$ graph with dilation 3 , congestion 1 , load $l$, and unbounded expansion.
Proof: Every searching path is only one path according to the algorithm Mesh_Mapping, allowing us to obtain congestion 1 and load 1 . Herein, we allow unbounded expansion to obtain the replaceable node of the faulty node. When a node is faulty, it is a worse case in which the dilation $=1+2=3$ at most by algorithm Mesh_Mapping. Because these nodes and links of searching paths are not replicated from algorithm Mesh_Mapping, These costs associated with graph embedding are dilation 3 , congestion 1 , load 1 , and unbounded expansion.
Theorem 7 A searching path of algorithm Mesh_Mapping is including $1 / 2^{*} n^{2}+\left(n^{*}\left\lfloor\log _{2} m\right\rfloor\right)$ $+3 / 2^{*} n-\left\lfloor\log _{2} m\right\rfloor^{2}+1$ nodes.

Proof: We can embed $M_{m_{1} \times m_{2} \times \cdots \times m_{d}}$ into $G_{n}(N)$ by theorem 6. If a node is faulty, we can change a bit in the binary string sequence from bit $\left\langle\log _{2} m\right\lrcorner$ to bit $n$ and insert its corresponding node into the queue. In the worst case, we can get $\left(n-<\log _{2} m \_+1\right)$ different nodes. Then we delete the node from the queue. From the first node we can change a bit in the sequence from bit 0 to bit ( $\left.\left(\log _{2} m\right\rfloor-1\right)$, and we can get $\left\langle\log _{2} m \downharpoonleft\right.$ different nodes. We can also change a bit in the sequence from bit 0 to bit $\left\lfloor\log _{2} m\right\lrcorner$ from the second node of the queue, and we can also get $\left(\left\langle\log _{2} m \_+1\right)\right.$ different nodes. Until the queue is empty, the sum of all searched nodes is $\left(n-\left\lfloor\log _{2} m\right\rfloor\right.$ $\left.+1) *\left(\log _{2} m \downharpoonleft+1\right)\right)+(1+2+\ldots+n)$. The search path includes $\left(n-\left\lfloor\log _{2} m\right\rfloor+1\right) *\left(\log _{2} m\right\rfloor$
$+1))+(1+2+\ldots+n)$ nodes. We assume there is an IC edge connecting to the faulty node by theorem 4.3. Therefore, we can search $\left\lfloor\log _{2} m /\right.$ nodes in the worst case. We infer the edges of the replacing method exist and none of the nodes and the edges has a duplicate replacement. That is, the whole search path includes $\left.\left.\left(n-\left\lfloor\log _{2} m\right\rfloor+1\right) *\left(\log _{2} m\right\rfloor+1\right)\right)$ $+\left(1+2+\ldots+n-\left\lfloor\log _{2} m\right\rfloor\right)+\left\lfloor\log _{2} m\right\rfloor=1 / 2 *$ $n^{2}+\left(n *\left\lfloor\log _{2} m\right\rfloor\right)+3 / 2 * n-\left\lfloor\log _{2} m\right\rfloor^{2}+1$ nodes.
Theorem 8 There are $\left.O\left(n^{2}-L \log _{2} m\right\lrcorner^{2}\right)$ faults, which can be tolerated.
Proof: By theorem 7, the whole search path includes $1 / 2 * n^{2}+3 / 2 * n+\left((n+1) *\left\lfloor\log _{2} m\right\rfloor\right)-\left\lfloor\log _{2} m\right\rfloor$ ${ }^{2}$ nodes. That is, $\left.O\left(n^{2}-\log _{2} m\right\lrcorner^{2}\right)$ faults can be tolerated.

## 5 Conclusion

In [20], we consider the problem of embedding rings in IEH graphs. After [20], we consider the problem of embedding meshes in IEH graphs. According the result, we not only can map these parallel programs of rings, but also can map these parallel programs of meshes in an IEH. In [21], we consider the problem of embedding meshes in Supercubes. Because the IEH is an asymmetric Incrementally Extensible Hypercube, it fit in with the distributed system or cloud computing system more than the Supercube. Obviously, the IEH is superior to Supercube in terms of embedding meshes or tori under faults.
In this paper, we try to find the replaceable node of the faulty node. The main result of this paper is the fact that it is always possible to give solutions to the embedding of meshes and tori in a faulty IEH. After a mesh is mapped in an IEH, we develop new algorithms to facilitate the embedding meshes and tori in a faulty IEH. Our results demonstrate that $O\left(n^{2}-L \log _{2} m J^{2}\right)$ faults can be tolerated. Also, the methodology is proven and an algorithm is presented to solve them. These existent parallel algorithms in mesh architectures can be easily transformed to or implemented in IEH architectures with load 1 , congestion 1 , dilation 3 , and unbounded expansion. Although an IEH is asymmetric, it has the same power as the hypercube in terms of meshes. The technology can be apply in grid computing and cloud computing.

References:
[1] S. B. Akers, and B. Krishnamurthy, A Group-Theoretic Model for Symmetric

Interconnection Networks, IEEE Trans. on Computers, Vol. 38, 1989, pp. 555-565.
[2] J. R. Armstromg and F. G. Gray, Faultdiagnosis in n-Cube array of microprocessor, IEEE Trans. on Computers, Vol. C-30, No. 4, 1992, pp. 587-590.
[3] D. P. Bertsekas and J. N. Tsitsiklis, Parallel and Distributed Computation: numerical methods, Prentice Hall, Englewood Ciffs, New Jersey, 1989.
[4] L. Bhuyan and D.P. Agrawal, Generalized Hypercubes and Hyperbus structure for a computer network, IEEE Trans. on Computers, Vol. 33, 1984, pp. 323-333.
[5] C. Chartand and O. R. Oellermann, Applied and Algorithmic Graph Theory, McGRAW-HILL Inc., 1993.
[6] K. Day and A. E. Al-Ayyoub, Fault Diameter of k-ary n-cube Networks, IEEE Trans. on parallel and distributed systems, Vol. 8, No. 9, 1997, pp. 903-907.
[7] Q. Dong, X. Yang, J. Zhao, and Y. Y. Tang, Embedding a family of disjoint 3D meshes into a crossed cube, Information Sciences, Vol. 178, No. 11, 2008, pp. 2396-2405.
[8] S. Dutt and J. P. Hayes, An automorphic approach to the design of fault-tolerance Multiprocessor, Proc. 19th Inter. Symp. on Fault-Tolerant Computing, 1989.
[9] M. J. Duff, CLIP4: A Large Scale Integrated Circuit Array Parallel Processor, IEEE International Joint Conference on Pattern Recognition, 1976, pp. 728-733.
[10] M. J. Duff, Real Applications on CLIP4, in Integrated Technology for Parallel Image Processing, Academic Press London, 1985, pp. 153-165.
[11] T. Hameenanttila, X.-L. Guan, J. D. Carothers, and J.-X. Chen, The Flexible Hypercube: A New Fault-Tolerant Architecture for Parallel Computing, Journal of Parallel and Distributed Computing, Vol. 37, 1996, pp. 213-220.
[12] J. Hastad, T. Leighton, and M. Newman, Reconfiguring a Hypercube in the Presence of Faults, ACM Theory of Computing, 1987, pp. 274-284.
[13] J. P. Hayes, and T.N. Mudge, Hypercube supercomputing, Proc. IEEE, Vol. 77, 1989, pp. 1829-1842.
[14] H.P. Katseff, "Incomplete Hypercubes," IEEE Trans. on Computers, Vol. 37, 1988, pp. 604-608.
[15] J. Kuskin, et al., The Stanford FLASH Multiprocessor, Proceedings of the $21^{\text {st }}$ Annual

International Symposium on Computer Architecture, 1994, pp. 302-313.
[16] F. T. Leighton, Introduction to parallel algorithms and architectures: Arrays, Trees, Hypercubes, MORGAN KAUFMANN PUBLISHERS, Inc., 1992.
[17] D. Lenoski, et al., The StanfordDASH Multiprocessor, Computer, Vol. 224, 1971, pp. 63-79.
[18] J.-C. Lin, "Fault-Tolerant Mapping of a Mesh in a Flexible Hypercube", WSEAS Transactions on Computers, Vol. 8, 2009, pp. 1587-1596.
[19] J.-C. Lin, "Simulation of Cycles in the IEH Graph," International Journal of Hjgh Speed Computing, Vo1. 10, No. 3, pp. 327-342 (1999).
[20] J.-C. Lin, S. K.C. Lo, S.-J. Wu, and H.-C. Keh, "Distributed Fault-Tolerant embeddings of rings in Incrementally Extensible Hypercubes with Unbounded Expansion", Tamkang Journal of Science and Engineering, Vol. 9, No. 2, pp. 121-128, 2006.
[21] J.-C. Lin, S.-J. Wu, H.-C. Keh, and L. Wang, "Fault-Tolerant Meshes and Tori Embedded in a Faulty Supercube", WSEAS Transactions on Computers, Vol. 9, No. 5, pp. 445-454, 2010.
[22] C. D. Park, and K.-Y. Chwa, Hamiltonian properties on the class of hypercube-like networks, Information Processing Letters, Vol. 91, 2004, pp. 11-17.
[23] F. P. Preparata, and J. Vuillemin, "The cube-connected cycles: A versatile network for parallel computation," Commun. ACM, Vol. 24, 1981, pp. 300-309.
[24] D. A. Rennels, On Implemanting Fault-tolerance in binary hypercubes, Proc. 16th Inter. Symp. on Fault-tolerant Computing, 1986, pp. 344-349.
[25] Y. Saad, and M. Schultz, Topological properties of Hypercube, IEEE Trans. on Computers, Vol. 37, 1988, pp. 867-871.
[26] J. L. C. Sanz, The SIMD Model of Parallel Computation, Springer-Verlag New-York, Inc., 1994.
[27] C. Seitz, The Cosmic Cube, Commun. ACM, Vol. 28, 1985, pp. 22-33.
[28] A. Sen, Supercube: An Optimally Fault Tolerant Network Architecture, Acta Informatica, Vol. 26, 1989, pp. 741-748.
[29] A. Sen, A. Sengupta and S. Bandyopadhyay, Generalized Supercube: An incrementally expandable interconnection network, Proceedings of the Third Symposium on Frontiers of Massively Parallel Computation-Frontiers'90, 1990, pp. 384-387.
[30] H. Sullivan, T. Bashkow, A large scale, homogeneous, fully distributed parallel machine, I, Proc. 4th Symp. Computer Architecture, ACM, 1977, pp. 105-177.
[31] S. Sur and P. K. Srimani, Incrementally Extensible Hypercube Networks and Their Fault Tolerance, Mathematical and Computer Modelling, Vol 23, 1996, pp. 1-15.
[32] S. Sur, and P. K. Srimani, IEH graphs: A novel generalization of hypercube graphs, Acta Informatica, Volume 32, 1995, pp 597-609.
[33] L. W. Tucker and G. G. Robertson, Architecture and applications of the connection machine, IEEE Comput., Vol. 21, 1988, pp.26-38.
[34] N.-F. Tzeng and H.-L. Chen, Fast Compaction in Hypercubes, IEEE Trans. on parallel and distributed systems, Vol. 9, No. 1, 1998, pp. 50-55.
[35] S.-H. Wang, Y.-R. Leu, and S.-Y. Kuo, Distributed Fault-Tolerant Embedding of Several Topologies in Hypercubes, Journal of Information Science and Engineering, Vol. 20, No. 4, 2004, pp. 707-732.
[36] L. D. Wittie, Communications structures for largenetworks of microcomputers, IEEE Trans. Comput., Vol. C-30, 1981, pp.264-273.
[37] C. Xu and F. C. M. Lau, Load Balancing in Parallel Computers-Theory and Practice, Kluwer Academic Publishers, Inc., 1997.
[38] P.-J. Yang, S.-B. Tien, and C.S. Raghavendra, Embedding of Rings and Meshes onto Faulty Hypercube Using Free Dimensions, IEEE Trans. on Computers, Vol. 43, No. 5, 1994, pp. 608-618.

