Optimizing LC VCO Performances Through a Heuristic

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Abstract: - We propose a heuristic for the optimal sizing of LC VCO's. The heuristic is an algorithm driven methodology that allows us determining optimal sizes of inductors and channel widths that minimizes the VCO's phase noise while satisfying fixed constraints (maximum consumed power, occupied area…). The proposed optimization methodology was applied to size a cross-coupled differential voltage controlled oscillator. This latter, designed using AMS 0.35 µm technology, achieves -124.9 dBc/Hz at 1MHz offset from a 2.6 GHz carrier frequency with 8.2mW consumption power and -118.7 dBc/Hz at 1MHz offset from a 5.4 GHz carrier frequency with 8.0mW consumption power.

Key-Words: - LC-VCO, Heuristic, Phase noise.

1 Introduction

The integrated inductance-capacitance (LC) voltage-controlled oscillator (VCO) is a common functional block in modern radio frequency communication systems. It is one of the main blocks forming the frequency synthesizer used to up and down convert signals.

Due to the evolution of wireless communication system, a high level of performances must be ensured by VCOs, mainly their phase noise and their power consumption. In fact, due to the ever-increasing demand for bandwidth, very stringent requirements are placed on the spectral purity of local oscillators [1]. Efforts to improve the phase-noise performance of integrated LC VCOs have resulted in a large number of realizations. Despite these endeavors, VCO design is still a complicated task since multiple interdependent variables and constants have to be handled. Besides, the growth of the telecommunication market imposes shortening the design delay. In this context, computer-aided optimization technique using geometric programming has been used to efficiently find the optimum design for certain LC oscillator topologies [2], [3]. Despite its efficiency, it provides limited physical insight into choosing the optimum design. To overcome these limitations, we propose an optimization methodology based in a physical standpoint study that allows us optimally sizing components composing LC VCOs, in order to minimize the phase noise while satisfying imposed constraints.

The paper is organized as follows: section II presents the cross coupled LC VCOs that was chosen as an application example for the proposed heuristic. Section III details constraints and performance function models that were taken into account in the optimization algorithm. Section IV presents the proposed heuristic. Section V presents the simulation results and compares the performance of our VCO to that of other reported LC oscillators to prove the adequacy of our design methodology. Finally, in section VI, we give some concluding remarks.

2 LC VCO Description

When dealing with high frequency applications, LC VCO circuits are preferred to other proposed oscillator structures, such as ring oscillators [4]. Different structures of LC oscillators have been already studied. The comparison presented in [5] shows that CMOS cross-coupled differential oscillator provides better noise performance than NMOS cross-coupled oscillator. In fact, the CMOS cross-coupled LC-VCO offers better rise- and fall-time symmetry, which results in a smaller $1/f^3$ noise corner [5]. In addition, the VCO bias current must be doubled for the NMOS structure to obtain the same tank amplitude as in CMOS structure.

Fig.1. presents a CMOS LC VCO circuit. This oscillator is mainly composed of a tank resonator

formed by inductors L1 and L2 and capacitors C1 and C2. The double cross-connected NMOS (M1-M2) and PMOS (M3-M4) differential pairs provide the negative resistance to compensate the tank loss [1]. The oscillation frequency range is controlled through two MOS accumulation varactors in series, C1 and C2. The accumulation mode varactor provides higher capacitance per unit area, better quality factor and wider tuning range when compared to reverse-biased PN junction and MOS depletion/inversion varactors [6].

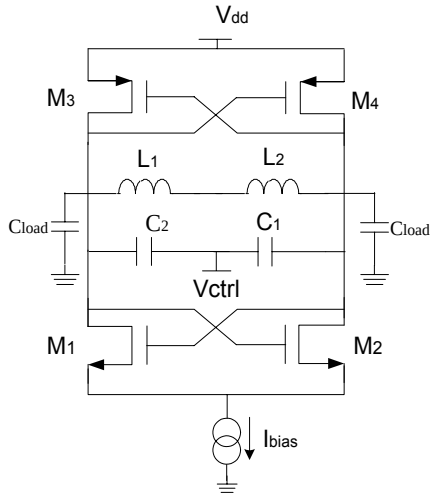

Fig.1.The cross coupled LC VCO circuit

2.1 Varactor equivalent model

LC VCO presented at fig. 1 comprises two varactors, C1 and C2. These MOS varactors can be modeled with a capacitor C_v in series with a parasitic resistor R_{sv} [1].
The resistance R_{sv} for the accumulation mode is calculated with the geometric varactor parameters: channel width (W_v), channel length ($l_{channel}$) and finger number (N_g); and with the sheet resistances of the n-well ($R_{nw,\square}$) and silicided polysilicon gate layer ($R_{poly,\square}$) [7].

$$R_{sv} = \frac{1}{12}\frac{1}{N_g}\left(R_{nw,\square}\frac{l_{channel}}{\frac{W_v}{N_g}} + R_{poly,\square}\frac{\frac{W_v}{N_g}}{l_{channel}} \right) \quad (1)$$

2.2 Inductor equivalent model

The VCO oscillation frequency and resistive loss are highly influenced by parasitic elements of the inductor. That's why we adopt in our study the symmetric π-model to describe the tank inductor (Fig.2). In this model, R_{pL}/C_{pL} and R_{sL}/C_{sL} are respectively the parallel and series parasitic resistances/capacitances of the inductor.

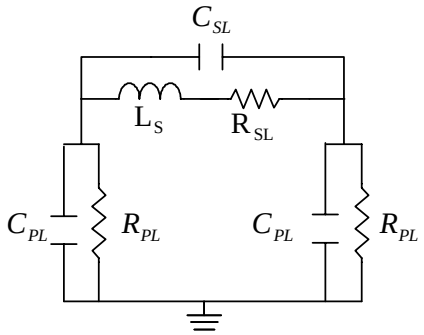

Fig.2. Inductor π-model

3 Systems Constraints and Performance Functions Formulation

In addition to inherent functional constraints, such as tank amplitude, frequency oscillation, tuning range and startup condition, the design of VCOs requires satisfying some other constraints that are imposed by the application. Three major constraints are commonly at the aim of interest, i.e. phase noise, power consumption and occupied area.
Below, we present these conditions and constraints.

- Since maximum autonomy is required for the emission reception transceiver, minimization of consumed power is necessary. This leads to the limitation of the circuit's bias current (I_{bias}), thus:

$$I_{bias} \le I_{max} \quad (2)$$

where I_{max} is the maximum bias current that is determined by the maximum allowed consumption power.

- In order to provide a high voltage swing, V_{tank}, for the stage connected at the output of the VCO, a minimum value of the tank amplitude $V_{tank,min}$ is fixed:

$$V_{tank} \ge V_{tank,min} \quad (3)$$

- The oscillation tuning range of the LC VCO pulsation ω, [ω_{min}, ω_{max}] is fixed according to the application, thus, the expression (4) must be satisfied.

$$\underbrace{\frac{1}{\sqrt{L_{tank}C_{tank,max}}}}_{\omega_{min}} \le \omega \le \underbrace{\frac{1}{\sqrt{L_{tank}C_{tank,min}}}}_{\omega_{max}} \quad (4)$$

where L_{tank} and C_{tank} denote the total tank inductor and capacitor respectively.

- The startup condition is given by [1]:

$$g_{active} \ge \alpha_{min} g_{tank,max} \quad (5)$$

where $\alpha_{min} \in [2,3]$ is the small-signal loop gain, g_{active} and g_{tank} are the active and the tank conductance respectively.

- The VCO occupied area is fixed by the used inductors. A maximum value for each inductor diameter (d_{max}) is imposed. This condition is also a determined factor in the integration of the oscillator.

$$d \leq d_{max} \tag{6}$$

- Each component forming the VCO can be considered as a noise source. The total phase noise level must be less than a specified maximum value that depends on the application specifications. Its expression is given by (7) [8]:

$$L\{f_{offset}\} = \frac{1}{8\pi^2 f_{offset}^2} \frac{1}{q_{max}^2} \sum_n \left(\frac{\overline{i_n^2}}{\Delta f} \Gamma_{rms,n}^2 \right) \leq L\{f_{offset}\}_{spec} \tag{7}$$

where f_{offset} is the offset frequency from the carrier and q_{max} is the total charge swing of the tank. The impulse sensitivity function Γ (ISF), represents the time-varying sensitivity of the oscillator's phase to perturbations. $\Gamma_{rms,n}$ is the root mean square (RMS) value of the ISF of the n^{th} noise source. The $i^2_n/\Delta f$ terms in the sum represent the equivalent differential noise power spectral density issued from drain current noise, inductor noise, and varactor noise.

4 The Optimization Approach

The proposed heuristic is based on a stochastic approach that consists of randomly generating test vectors formed by unknowns of the optimization problem. This is necessary to face the large number of possible combinations of candidate solutions.
Each test vector serves to compute companion formula, i.e. values of parasitic components, etc.
A data base is integrated in the optimization process. It consists of parasitic elements forming the inductor. These values were computed for different operating frequencies, using ASITIC software [9].
If the test vector satisfies imposed constraints such as transistor saturation conditions, it is memorized in an archive.
In order to avoid an excessive growth of the archive, a sorting routine is added to the program, thus only a predetermined number of solutions is memorized.
The optimizing process takes end the stopping criterion is verified. i.e. if the archive is not updated after a certain number of iterations.
Figure 3 presents the flowchart of the proposed heuristic.

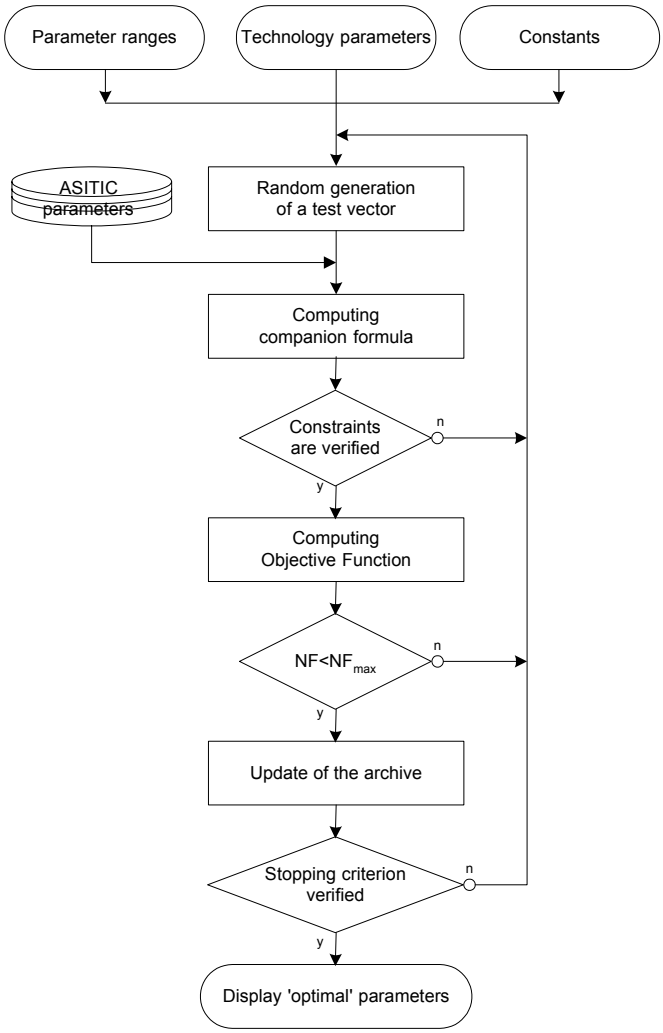

Fig.3. Flowchart of the proposed heuristic

4.1 Design variables ranges

The test vector is formed by the bias current, MOS transistor width and the inductor value, which variation ranges are fixed by the user/technology. Since parasitic elements are not fixed randomly but depended on the inductor value, we start with the optimization of inductor surface using ASITIC software. So, we obtain automatically all the geometric parameters, parasitic resistors (R_S and R_{SL}) and capacitors (C_S) corresponding to the model provided by ASITIC (Fig.4). Then, R_{pL} and C_{pL} corresponding to the parallel π-model can be calculated using the following equations:

$$R_{PL} = \frac{1 + (\omega R_S C_S)^2}{\omega^2 R_S C_S^2} \tag{8}$$

$$C_{PL} = \frac{C_S}{1+(\omega R_S C_S)^2} \quad (9)$$

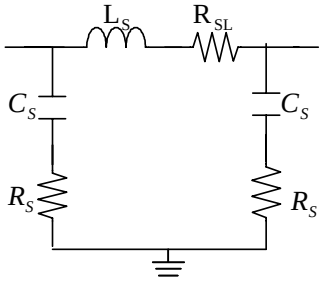

Fig.4. Inductor model provided by ASITIC

4.2 Constraints formulation

Mainly two constraints have to be satisfied to ensure the functioning of a VCO: the start-up condition and the tank amplitude constraint. In the following we detail their formulations.

4.2.1 Start-up condition

From expression (4), with $\alpha_{min}=2$, this condition can be given by (10):

$$start\_up = g_{active} - 2g_{tank} \geq 0 \quad (10)$$

The active and tank conductances are calculated respectively by:

$$g_{active} = \frac{1}{2}\left[\sqrt{\mu_n C_{oxn}\frac{W_n}{l_{channel}}I_{bias}} + \sqrt{\mu_p C_{oxp}\frac{W_p}{l_{channel}}I_{bias}}\right] \quad (11)$$

$$g_{tank} = \frac{1}{2}\left((\lambda_n+\lambda_p)\left(\frac{I_{bias}}{2}\right)+g_v+g_L\right) \quad (12)$$

where W_n, W_p, μ_n, μ_p, C_{oxn}, C_{oxp}, λ_n and λ_p are respectively channel width, mobility charges, oxide capacitance and channel length modulation of NMOS and PMOS transistors forming active part. g_v is the varactor effective parallel conductance and g_L is the inductor effective parallel conductance. To improve the $1/f^3$ corner of phase noise, a symmetric active circuit with equal transconductances $g_{mn}=g_{mp}$ is used [9], which establishes a relation between W_p and W_n.

$$W_P = \frac{\mu_n}{\mu_p}W_n \quad (13)$$

Both channel length l_n and l_p of the NMOS and PMOS transistors are set to the minimum allowed by the technology ($l_{channel}$) to reduce parasitic capacitance and get the highest transconductance.

In (14), the inductor effective parallel conductance g_L is determined by:

$$g_L = \frac{1}{R_{pL}} + \frac{R_{sL}}{(2\pi f_0 L_s)^2} \quad (14)$$

where R_{sL} and R_{pL} are respectively the inductor parasitic series and parallel resistances.
And the varactor effective parallel conductance g_v is given by:

$$g_v = (C_{v,max}\,2\pi f_0)^2 R_{sv} \quad (15)$$

where $C_{v,max}$ is the maximum MOS varactor value and R_{sv} is the MOS varactor parasitic series resistance given by (1).
Since the maximum total capacitance value $C_{tank,max}$, is the sum of varactors capacitance C_v, parasitic capacitances of inductors C_{pL}, NMOS and PMOS gate to source capacitances ($C_{gs,n}$ and $C_{gs,p}$) and the load, the maximum MOS varactor value $C_{v,max}$ can be expressed as:

$$C_{v,max} = 2C_{tank,max} - (C_{gs,n} + C_{gs,p} + C_{pL} + C_{load}) \quad (16)$$

where the total capacitance value $C_{tank,max}$, can be given by:

$$C_{tank,max} = \frac{1}{(2\pi f_{min})^2 L_{tank}} \quad (17)$$

Knowing that the maximum MOS varactor value equals $C_{ox}W_v l_{channel}$, the transistor channel width is given by:

$$W_v = \frac{C_{v,max}}{C_{oxp} l_{channel}} \quad (18)$$

4.2.2 Tank amplitude constraint

From expression (2), this constraint is expressed by:

$$V_{tank} - V_{tank,min} \geq 0 \quad (19)$$

where the tank amplitude is given by [5].

$$V_{tank} = \frac{4}{\pi}\frac{I_{bias}}{g_{tank}} \quad (20)$$

4.2.3 Objective function

The objective function is the phase noise $L\{f_{offset}\}$ which must be less than the phase noise

specification required by the application $L\{f_{offset}\}(spec)$.

$$L\{f_{offset}\} = 10\log_{10}(AB) \le L\{f_{offset}\}_{(spec)} \quad (21)$$

where A is given by:

$$A = \left(\frac{1}{16\pi^2 f_{offset}^2} \frac{L_{tank}^2 (2\pi f_0)^4}{V_{tank}^2} \right) \quad (22)$$

and B is given by:

$$B = \left(2KTg_L + 2KTg_V + 2KT\gamma\left(g_{d0,n} + g_{d0,p}\right)\right) \quad (23)$$

where $g_{d0,n}$ and $g_{d0,p}$, the channel conductances at zero V_{DS} for NMOS and PMOS transistors respectively [10], are expressed for short-channel transistors by:

$$g_{d0n} = \frac{I_{bias}}{l_{channel} E_{sat,n}} \quad (22)$$

$$g_{d0p} = \frac{I_{bias}}{l_{channel} E_{sat,p}} \quad (23)$$

with $E_{sat,n}$ and $E_{sat,p}$ are the saturation electric field for NMOS and PMOS transistor respectively.

5 Optimized and Simulation Results

The proposed heuristic was implemented in C^{++}. Design parameters' ranges are given in Table 1.
The parameters' optimization will be done for two frequency ranges:

- The first one between, ω_{min}= 2.4GHz and ω_{max}= 2.8GHz
- The second one between, ω_{min}=5GHz and ω_{max}=5.8GHz.

The parasitic elements values of inductor, i.e. resistances and capacitances, were determined using ASITIC software for different values of inductor. These values correspond to the discretization of the inductor's value range. Table 2 and Table 3 present these inductors parameters respectively for the first and second applications cited above.

Table 1. Design Parameters Ranges

Bias current	$I_{bias} \in [1mA, \ 4mA]$
NMOS width	$W_n \in [10\mu m, \ 100\mu m]$
Inductor value	$L_{tot} \in [1\,nH, \ 6\,nH]$

Optimal obtained parameters' values and performances corresponding to the first and second application are presented respectively in tables 4 and 5.

Table 2. Inductor parameters at 2.6 GHz

L_1=L_2 [nH]	1	1.5	2	2.5	3
R_{SL} [Ω]	5.34	3.26	4	4.43	6.5
R_S [KΩ]	2.4	1	1.17	0.9	1.45
C_S [fF]	184	131	155	200	82
Q_L	3	6.47	6.7	6.75	6.11

Table 3. Inductor parameters at 5.4 GHz

L_1=L_2 [nH]	1	1.5	2	2.5	3
R_{SL} [Ω]	4.35	6.17	3.86	5	5.78
R_S [KΩ]	1.85	3	1	1.4	1.1
C_S [fF]	44.3	51.59	158	170	148
Q_L	6.78	7.24	8.26	8.44	7.16

Table 4. Optimal parameters values for the frequency range 2.4 Ghz to 2.8 Ghz

	I_{bias} (mA)	**L_{tot} (nH)**	**W_n (µm)**	**W_p (µm)**	**W_v (µm)**	**L{1Mhz} (dBc/Hz)**
1	3	4	97.2	312.1	765	-126.0
2	3.4	3	75.4	242.2	1212	-125.5
3	3.8	3	71.6	230.1	1224	-126.4

Table 5. Optimal parameters values for the frequency range 5 Ghz to 5.8 Ghz

	I_{bias} (mA)	**L_{tot} (nH)**	**W_n (µm)**	**W_p (µm)**	**W_v (µm)**	**L{1Mhz} (dBc/Hz)**
1	3	2	30	96.3	331	-119.2
2	3	2	27.6	88.7	297	-119.2
3	3.4	2	32.4	104	324.6	-120

ADS simulation results using AMS CMOS 0.35µm technology and 2.5V voltage power supply are presented in Fig.5, Fig.7 and Fig.9 corresponding to the second row of table IV optimized parameters', and in Fig.6, Fig.7 and Fig.8 corresponding to the second row of table 5 optimized parameters'.
Fig.5 shows that the VCO output signal oscillates between 0.83V and 2.29V giving tank amplitude equals to 1.49V for the first frequency range, while Fig.6 shows that the VCO output signal oscillates between 0.7V and 2.45V giving a tank amplitude equals to 1.75V for second frequency range.

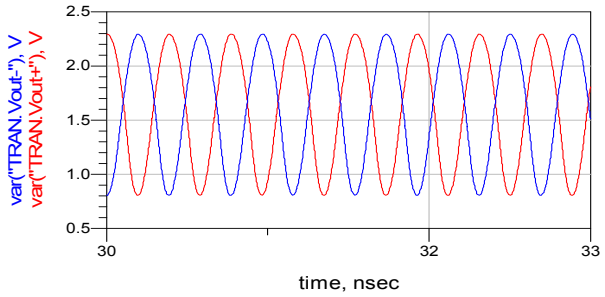

Fig.5. Output signal at 2.6 Ghz

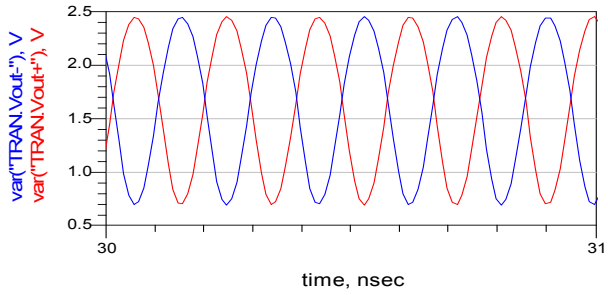

Fig.6. Output signal at 5.4 GHz

In Fig.7 and 8, the frequencies versus control voltage yielding respectively a tuning range of 15% under 2.5Vpower voltage supply for the first frequency range and a tuning range of 10.5% under 2.8V supply for second frequency range are presented.
At the center frequency, i.e f_0=2.6 GHz, the oscillator phase noise, illustrated in Fig.11, achieves -124.9 dBc/Hz, -120.4 dBc/Hz and -104 dBc/Hz respectively at 1MHz, 600KHz and 100KHz offset frequencies. While at the center frequency, i.e f_0=5.4 GHz, the oscillator phase noise, which is presented in Fig.10, achieves -118.75 dBc/Hz, -114.07 dBc/Hz and -96.36 dBc/Hz respectively at 1MHz, 600KHz and 100KHz offset frequencies.

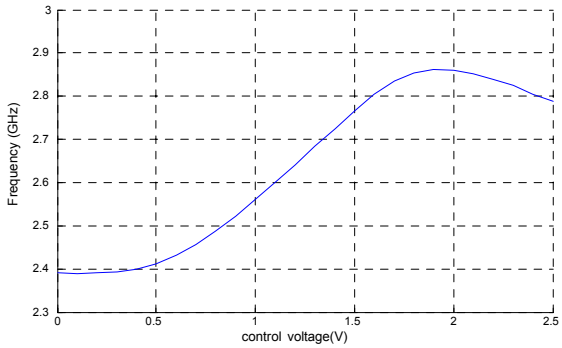

Fig.7. First application VCO characteristic

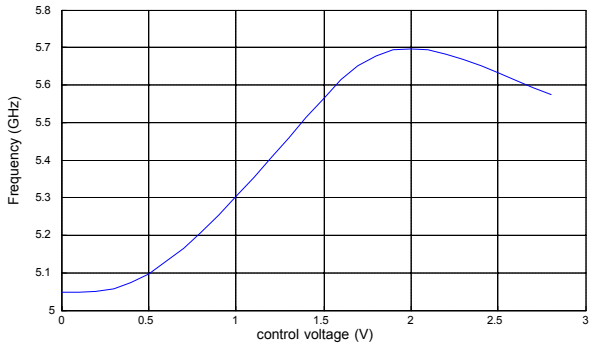

Fig.8. WiMAX VCO characteristic

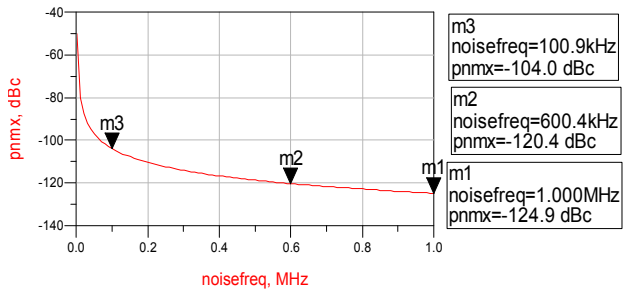

Fig.9. Oscillator phase noise at 2.6GHz.

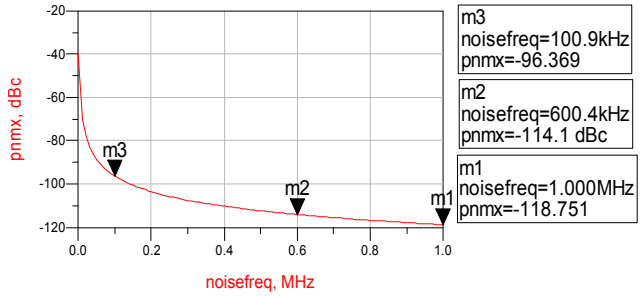

Fig.10. Oscillator phase noise at 5.4GHz.

Table 6 presents a comparison between theoretical (proposed heuristic) and simulation (ADS software) results. We notice the good agreement between both results.
Commonly, a figure of merit (FOM) is used to compare obtained performances. Its expression is given by (24) [1]:

$$FOM = L\{f_{offset}\}[dBc/Hz] + 10\log(P[mw]) - 20\log\left(\frac{f_0}{f_{offset}}\right) \quad (24)$$

Table 7 presents a comparison between performances obtained using the proposed heuristic and some of published papers.

Table 6.Comparison between theoretical and simulation results

		Heuristic	**ADS software**
L{1Mhz} (dBc/Hz)	**2.6 GHz**	-125.47	-124.94
	5.4 GHz	-119.15	-118.75

Table 7. Comparison between VCOs Performances

Ref.	**Tech.**	**F_0 [GHz]**	**P [mW]**	**Phase noise [dBc/Hz]**	**FOM [dBc/Hz]**
This work CMOS 0.35 µm		**2.6**	**8.2**	**-124.9 @1MHz**	**184.1**
		5.4	**8.0**	**-118.7 @1MHz**	**184.4**
[11]	SiGe BJT process	2.4	41.2	-128 @1MHz	179.5
[1]	CMOS 0.35µm	2.6	10	-119.4 @1MHz	177.7
[12]	CMOS 0.35µm	2.2	6.3	-115 @600KHz	178.2
[13]	CMOS 0.18µm	5.8	8.1	-110 @1MHz	176
[14]	CMOS 0.13µm	5.2	2.5	-114 @1MHz	184.9
[15]	CMOS 90nm	5.6	14	-108 @1MHz	172
[16]	CMOS 0.18µm	5.6	5.8	-116.6 @1MHz	184

6 Conclusion

An optimization approach was proposed for the sizing of LC voltage controlled oscillators. It is a stochastic approach that consists of computing optimal values of LC VCO components that minimizes the phase noise while satisfying start-up and tank amplitude constraints. Two applications examples were presented. The presented application consists of optimizing phase noise of a cross coupled LC VCO. Good performances were reached for the frequency range [2.4GHz, 2.8GHz] and the frequency range [5.GHz, 5.8GHz]. They were compared to simulation results and to published works dealing with this kind of VCO's lie.

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