Synthesis of Switched Current Memory Cells Using the Nullor Approach and Application to the Design of High Performance SI Sigma Delta Modulators

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Abstract: - This work presents the design of switched current sigma delta modulators. The nullor approach is adopted to synthesize voltage followers used to design translinear-loop-based switched current memory cells. Besides, it is proposed an approach for computing optimal biases and sizing of transistors forming the modulator. This heuristic allowed us sampling a second order modulator up to 80MHz, ensuring more than 60dB of SNR.

Key-words: - Switched current technique, Voltage follower, Nullor, Heuristic, Sigma Delta Modulator.

1. Introduction

Advances in the very low scale integration field enable designing complex integrated circuits. VLSI technologies are now maturing with a current emphasis towards nano-structure and sophisticated applications combining digital as well as analog circuits on a unique chip [1].

Switched mode techniques are well suited to provide an interface between digital and analog realms. In the switched mode field, mainly two implementations are possible: the switched current (SI) and the switched capacitor (SC) techniques.

Switched current technique [2] is relatively a new analogue sampled data technique that overcomes some problems associated with its counterpart; the switched capacitor technique [3-5]. However there still remains a shortfall when compared to the best of SCs.

Since their introduction, a wide variety of SI circuit structures have been studied. In this paper we focus on the synthesis of SI cells and their use to design high performance SI sigma delta $(\Sigma\Delta)$ modulators [6].

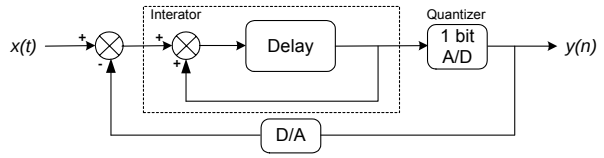


Figure 1. First order sigma delta modulator.

The basic $\Sigma\Delta$ modulator consists of a summing node, an integrator, a quantizer and a digital to analog converter (D/A), as it is shown in figure 1. A discrete time integrator is based on the use of a delay unit that can be designed using switched current memory cells. Indeed, a SI cell perform a Sample/Hold effect, i.e. a half delay ($z^{-½}$). Thus, a full delay (z^{-1}) can be realized by cascading two SI memory cells.

The basic SI memory cell, namely the conventional second generation class A cell, which is depicted at figure 2, was improved by adopting the class AB lie (see figure 3). Thus, the dynamic range of the cell, which couldn't exceed the bias current, can reach four times this latter [2,7]. Consequently, the cell's yield was highly increased.

However, this topology still suffer from non-idealities; mainly input to output conductance ratio error, i.e. variation of the voltage at node *x* (figure 2) when the cell's switches between the acquisition and the restitution phases. To further improve the SI cell's performances, a craft that consists of stabilizing this potential by virtually applying a voltage source at this node, was proposed [2]. The idea consists of using a translinear loop that instantiates the replication of a reference DC voltage at the input-output node (*x*).

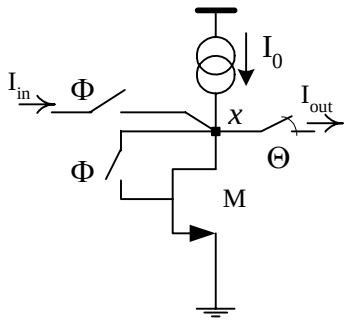


Figure 2. The 2nd generation class A memory cell. Θ and Φ are two non overlapping clocks.

In this brief we first deal, in section 2, with synthesizing translinear voltage followers VFs and their manipulation to design class AB switched current memory cells. The nullor approach is adopted for this purpose. Since the switched current cell presents the basic sub-circuit forming a sigma delta modulator and knowing that performances of this latter are highly dependent of the ones of the basic cell, in section 3, we deal with optimizing performances of the cell. A heuristic that allows us computing optimal cell's parameters is detailed is this section. Section 4 presents the designed SI sigma delta modulator and gives simulation results showing good reached performances. Finally, conclusion remarks are summarized in section 5.

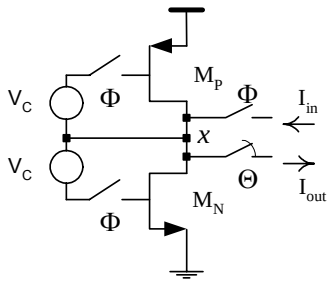
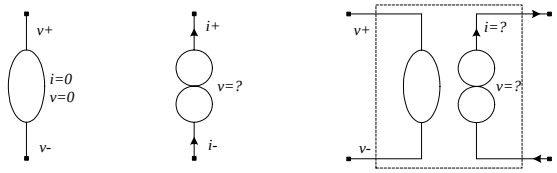


Figure 3. The class AB SI memory cell.

2. Synthesis of voltage followers

Voltage followers (VFs) as well as current followers (CFs) have been very useful to implement novel analog applications. VFs can be designed automatically by manipulation of nullators and norators [8,9].

A nullator is an element which does not allow current flow through it. In addition, the voltage across its terminals is zero under all conditions. A norator has an arbitrary voltage across it. This element has no constitutive equation. Together, the nullator and the norator form a nullor [10,11]. Figure 4 illustrates these 'weird' elements.



(a) (b) (c)

Figure 4. The (a) nullator, (b) norator, (c) nullor representations.

It has been established that the nullor can be considered as a universal active element [12]. This means that together with a set of resistors and capacitors, we can implement (ideally) all functions, e.g. a MOS transistor, as shown in figure 5. Voltage followers (VFs) can be synthesized by a correct manipulation of nullators.

At a first level of abstraction, a VF can be modeled by a single nullator as shown in figure 6.a [11]. Figure 6.b shows a useful topology to model the most abstract behavior of the VF using four nullators.

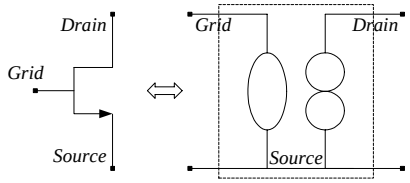


Figure 5. Modeling the behavior of an ideal MOS transistor.

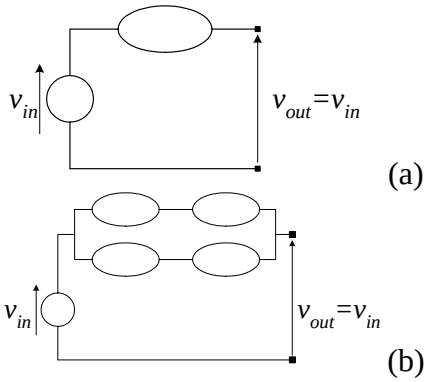
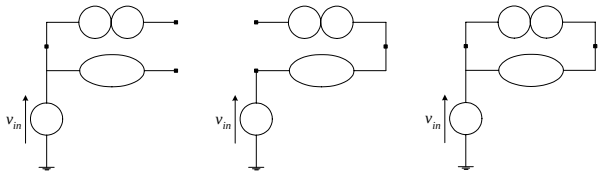


Figure 6. The Nullator equivalent circuits to describe a VF.

Tlelo and coworkers have proposed in [8] a systematic method for the computational synthesis of CMOS VFs. It mainly consists of the following steps:

- Generation of the small signal equivalent circuit by selection of nullators:

Since the voltage across a nullator is zero, one or several nullators can be used to model the behavior of a generic VF, as it is shown by figure 6. However, since a nullator by existing alone does not have a physical meaning, for synthesis purposes nullator-norator joined-pairs must be generated by addition of one norator to each nullator, as it is shown by figure 7. Furthermore, the generation of the small signal circuitry consists of forming joined-pairs to generic VF modeled by adopting nullators descriptions. It is easy to demonstrate that 3^N combinations are possible to form nullator-norator joined-pairs by addition of one norator to each nullator. *N* is the number of nullators.



(a) (b) (c)

Figure 7. Generation of small-signal circuitries.

• Generation/addition of the bias circuitry:
The bias circuitry is generated by addition of DC voltage and current bias to a small-signal circuitry composed of nullator-norator joined-pairs [13]. For instance, two kinds of bias circuitries are possible. Figure 8 illustrates these circuitries.

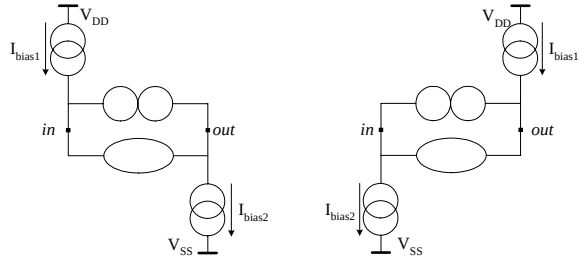
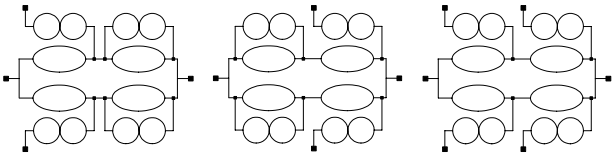


Figure 8. Generation of bias circuitry for joined-pair of figure 7.c.

• Synthesis of the nullors using MOS transistors:
In a biased circuit, each nullator-norator joined-pair can be synthesized by a MOS transistor, where the joined terminals are associated to the source terminal, while the other terminals of the nullator and norator, are associated to the gate and drain terminals.
We refer the reader to [8] for further details about the synthesis process.



(a) (b) (c)

Figure 9. Three of the 81 possibilities to form joined-pairs from figure 6.b.

Thus, by forming joined pairs for the VF shown in figure 6-b, translinear loops can be constructed. These are well suited for designing practical VFs.
Furthermore, 81 combinations are possible and suitable for the VF from figure 6-b. However, during the addition of the bias circuitry and the synthesis of each nullator-norator pair, only some topologies are useful.
By beginning from figure 6-b, and applying the synthesis method, in figure 9 are shown three possible combinations of nullator-norator joined pairs.
Among all possible VF topologies and after generating the bias circuitry and by synthesizing the nullor equivalents and biases using MOS transistors, in figure 10 are shown three VFs. The first one (a) is the well-known translinear-loop topology that has been widely used to implement practical analog signal processing applications. The second (b) is a new one composed of two complementary differential pairs, and the third (c) has been used in its bipolar version to realize the commercially available CFOA AD844 (http://www.analog.com/en/prod/0,2877,AD844,00.html).

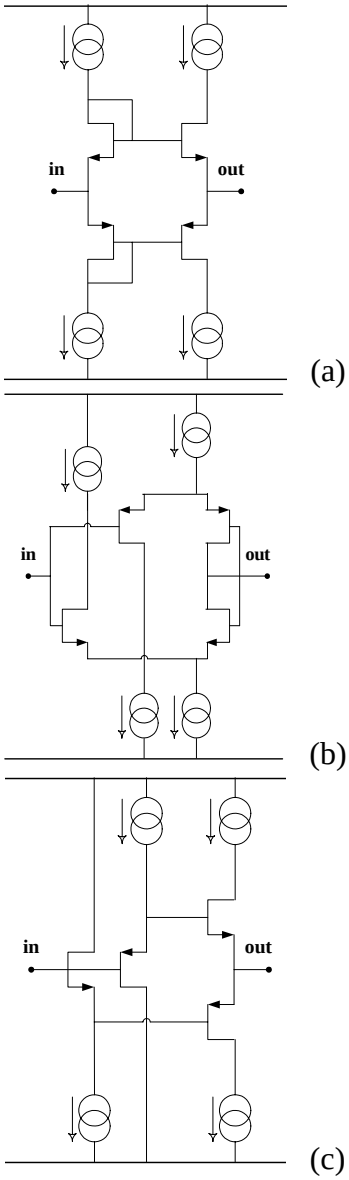


Figure 10. Three VFs synthesized from figure 6.b.

3. Design of switched current class AB memory cells

As it was introduced above, the functioning of the class AB cell is similar to the class A cell except that it comprises two memory transistors. Class AB memory cells were proposed to overcome limitations of the conventional class A cell; mainly the input dynamic range. It has been already proven that for the class AB lie, input currents can reach four times the bias current [7]. However, and due to the switching between the acquisition and the restitution phases, topology of the whole circuit changes and consequently the voltage of the input-output node varies considerably [2]; a fact that may

considerably damage the circuit's performances. In order to annihilate these potential variations, a voltage follower offers a good solution to control the potential of this node (when combined to the class AB memory stage). Thus, using the three designed VFs shown in figure 10, we designed three class AB SI memory cells. Figure 11 shows these memory cells. Besides the bias role, the added floating source (Vc) ensures that an identical voltage changes at NMOS and PMOS gates. It is realized using an isolated diode connected PMOS transistor [14].

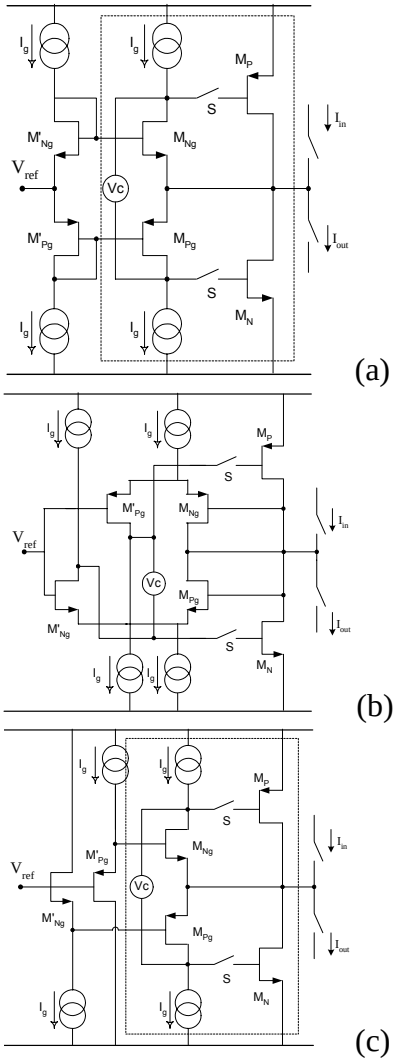


Figure 11. SI cells designed using the VFs from figure 7.

Unlike cells presented in figures 10.a and 10.c that offer low impedance on the input-output node, the cell of figure 10.b has a higher memorizing capacitance which can be exploited to minimize charge injection due to the switching of the voltage switches. Thus this cell can be optimized for low frequency-high precision applications. Figure 10.a is the class AB grounded gate SI memory cell proposed in [15], where two memory transistors ensure the class AB memory and the four transistors embedded in the translinear loop instantiate the replication of the reference voltage (V_{ref}) at the input-output node. Cells presented by figures 10.b and 10.c are novel cells.

Knowing that resolution of ΣΔ modulators is mainly decided by oversampling ratio (OSR), levels of the quantizer, and order of the modulator, in the following we focus on the use of both last evoked cells since their topologies are better applicants for high frequency applications.

4. The Optimization approach

Even though switched current technique has overcome some of limitations of its counterpart, i.e. the switched capacitor technique, SI cells still suffer from non-idealities, mainly noise, settling time error and charge injection [2,15]. Technical solutions were proposed to minimize the effect of the last evoked problem. They consist of the use of dummy transistors that minimizes the switching charge injected in the grid to source capacitance of the memory transistors. In the following we focus on optimizing the other performances, i.e. minimizing settling time and maximizing the cell's signal to noise ratio (SNR). These 'performances' form the objective functions to optimize (OFs). Expressions (1) and (2) give current transfer function of the class AB cell and SNR expression. These expressions can be considered valid for both cells (figures 11.a and 11.c) since these performances mainly rely on the sub-circuit delimited with dashed line box.

$$\frac{i_{in}}{i_{mem}} = 1 + \frac{\left(g_{mg} + g_{0g}\right)\, C + g_{0g}.C_g}{g_m.g_{mg}}\, s + \frac{C.C_g}{g_m.g_{mg}}\, s^2 = 1 + \frac{1}{2.\xi}.\frac{s}{\omega_0} + \frac{s^2}{{\omega_0}^2} \quad (1)$$

where $\omega_0 = \sqrt{\frac{g_0 g_{0g} g_s + g_m g_s \left(g_{0g} + g_{mg}\right)}{\left(g_0 + g_s\right) C.C_g}}$ and

$$\xi = \frac{1}{2}.\frac{\left[\left(g_{0g}+g_{mg}\right)\left(g_0+g_s\right)+g_0.g_s\right]C+g_{0g}\left(g_0+g_s\right)C_g}{\sqrt{\left[g_0 g_{0g} g_s+g_m g_s\left(g_{0g}+g_{mg}\right)\right]\left(g_0+g_s\right)C.C_g}}.$$

i_{in} and i_{mem} refer to the input and memorized currents. (g_0, g_m), (g_{0g}, g_{mg}), (C, C_g) represent conductances, transconductances and gate to source capacitances of the grounded gate (M_{Ng}, M_{Pg}) and memory (M_N, M_P) transistors respectively. g_s represents *on*-conductance of the voltage switch (*S*). *s* is Laplace operator.

We notice that minimizing the cell's response time can be performed by minimizing the reduced time one by maximizing the proper pulsation ω_0 and

minimizing $\left(\xi - \sqrt{2}/2\right)$. This latter expression will be introduced as a constraint to satisfy in the optimization algorithm by imposing $\left|\xi - \sqrt{2}/2\right| < \varepsilon$. $\varepsilon << 1$.

$$SNR = 10\log \frac{\left|\left(4I_0\right)^2\right|}{\left|kT\dfrac{4\left(G_m\right)^4}{3.C\left(G_m + \dfrac{G_0 G_{0g}}{G_{mg}}\right)^2}\right|} \quad (2)$$

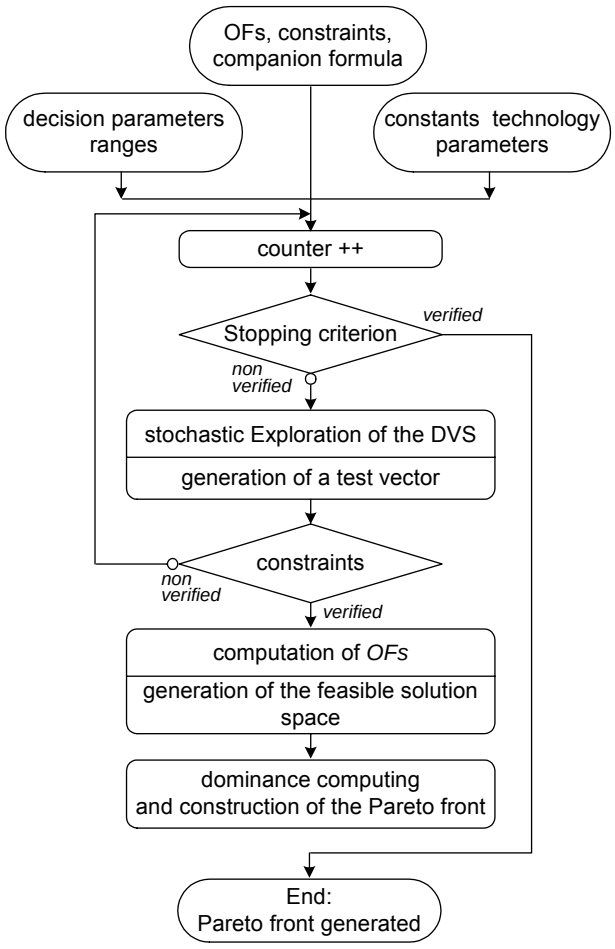


Figure 12. Flowchart of the heuristic.

The adopted heuristic is an algorithm driven methodology based on a stochastic approach. Indeed, in order to face the large number of possible parameters values that have to be tested, we used a random approach to explore the decision variable space (DVS) to generate test vectors.

The proposed heuristic mainly consists of the three following steps:

1. random generation of a test parameter vector. This latter comprises the problem unknowns, i.e. widths and lengths of MOS transistors forming the memory cell, and the VF-based translinear loop bias current I_g.
2. store test vector and OFs values (when constraints are verified).
3. generate the Pareto front by applying a dominance selection procedure[1].

Figure 12 presents the flowchart of the proposed heuristic. The algorithm was implemented in C++.

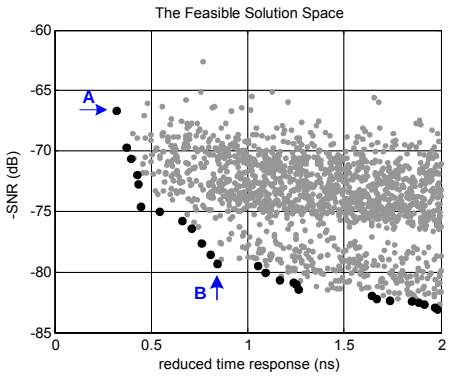


Figure 13. The feasible solution space.

Figure 13 shows the feasible solution space (-SNR *vs* reduced response time), where the black spots represent the Pareto boarder. We notice that the problem for maximizing SNR is transformed to minimizing –SNR.

The heuristic's algorithm supplies a table presenting Pareto solutions and their correspondent antecedents, i.e. parameters' values. Notice that additional degrees of freedom are provided to the designer to choose his 'optimal' parameter vector within the set of the non-dominated solutions. For instance, an additional criterion can be the occupied area.

The following figures, presenting simulations of the cells of figures 11.a and 11.c, are performed using Spice software and correspond to the 'optimal' solution (A) in figure 13 (solution corresponding to the lowest response time). Simulation conditions and 'optimal' device scaling are given in tables I and II respectively. According to figures 14 and 15, the cell's SNRs equal 67.9dB and 62.2dB, when input current equals $100e^{-6}\sin(9e^{3}\pi t)$ and sampled at 80MHz (each cell was loaded with an identical diode-connected cell). Figure 16 shows transient grid voltage of the NMOS memory transistor at the acquisition phase. Time responses are less than 300 ps for both cells.

[1] Definition of Pareto optimality is given in Appendix.

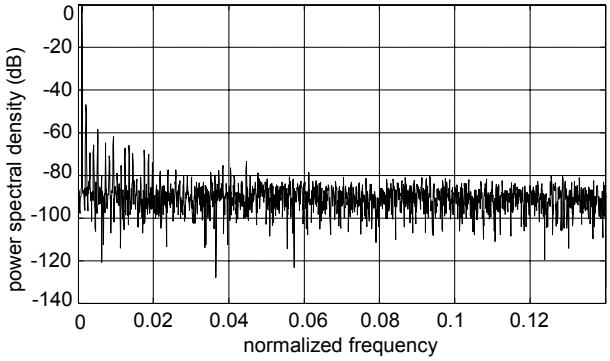


Figure 14. Output power spectral density of the SI cell (fig. 11.a) sampled at 80MHz.

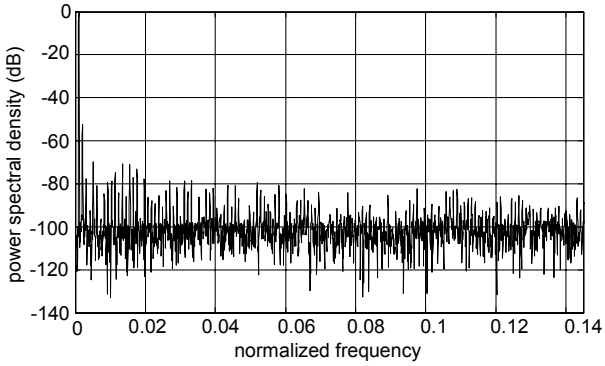


Figure 15. Output power spectral density of the SI cell (fig. 11.c) sampled at 80MHz.

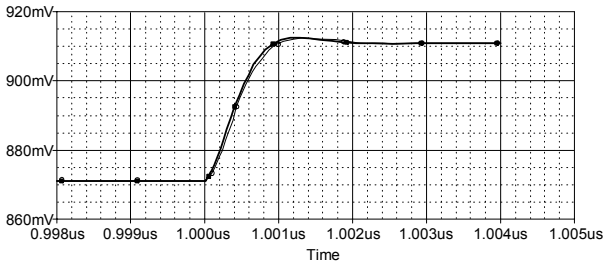


Figure 16. The cell's transient NMOS gate voltage response.

As it was mentioned above, Pareto front offers the designer the possibility to choose 'his' optimal solution among a set of optimal ones. In contrary, the weighting method, which is widely used, can only provide a unique 'optimal' solution. Besides, performances of this approach depend on the kind of the feasible solution space (convex or not). In [15] a sizing of the cell of figure 11.a was proposed (using the weighting approach). It corresponds to the one of solution B (figure 13). Figures 17 and 18 present output power spectral densities for both cells, where we adopted the same sizing for the second SI cell. Thus, for a 1MHz sampling frequency and a $100e^{-6}\sin(9e^{3}\pi t)$ input current, obtained SNRs equal 72.8dB for both cells.

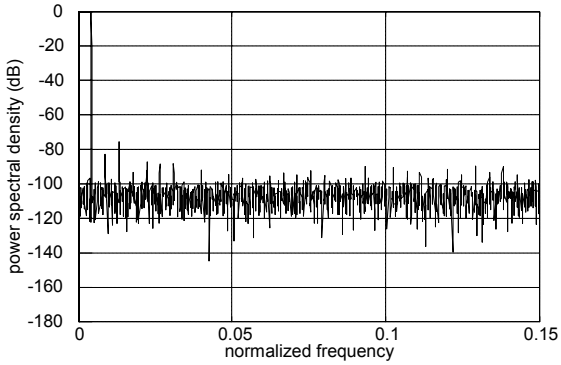


Figure 17. Output power spectral density of the SI cell (fig. 11.a) sampled at 1MHz.

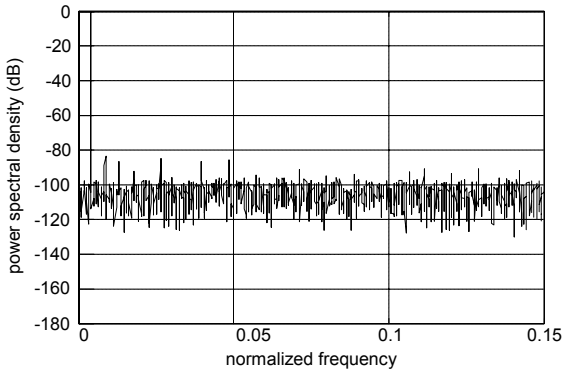


Figure 18. Output power spectral density of the SI cell (fig. 11.c) sampled at 1MHz.

Table I. Simulation conditions.

Technology	0.35µm
Supply voltage	Single 3.3v

Table II. Optimal device scaling (in µm): point A. I_g=49.15µA

L_N/W_N	L_P/W_P	L_{Ng}/W_{Ng}	L_{Pg}/W_{Pg}
2.10/11.55	1.25/19.05	1.70/5.55	1.05/9.15

Table III. Optimal device scaling (in µm): point B I_g=60µA

L_N/W_N	L_P/W_P	L_{Ng}/W_{Ng}	L_{Pg}/W_{Pg}
57.85/39.95	95.35/24.25	5.80/0.60	6.55/1.00

5. Design of a sigma delta modulator

In the SI approach, the memory cell is the fundamental building block of the sigma delta modulator [6,16]. Accordingly, performances of the $\Sigma\Delta$ modulator are tightly dependent on those of the SI used cell. In the following we present the design of a second order $\Sigma\Delta$ SI modulator using cells presented at figures 11.a and 11.c, and adopting 'optimal' sizing presented in table II for both cells. Figure 19 shows the block diagram of the designed modulator. At figures 20 and 21 we

present both forward and backward integrators designed using the cell of figure 11.c. Figures 22 and 23 show the transistor level and the functioning principle of the used quantizer and DAC respectively [17].

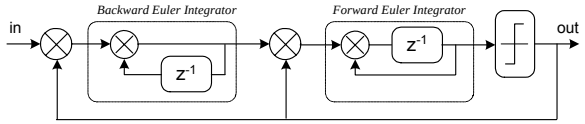


Figure 19. The block diagram of a classic second order ΣΔ modulator.

It is important to put the light on the good reached performances obtained using both SI memory cells. Indeed, in both cases, both second order switched current ΣΔ modulator can be sampled up to 80MHz. From figures 24 and 25, we notice comparable aspects of noise rejection. We also measure SNR peaks of 65.4dB and 60.6dB respectively for modulators designed using cells of figures 11.a and 11.c respectively. The simulations were performed for a 83kHz sinusoidal input current which amplitude equals 100µA. FFTs were computed for 16384 points for all cases.

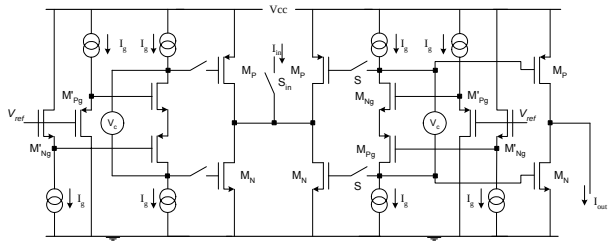


Figure 20. The forward SI integrator.

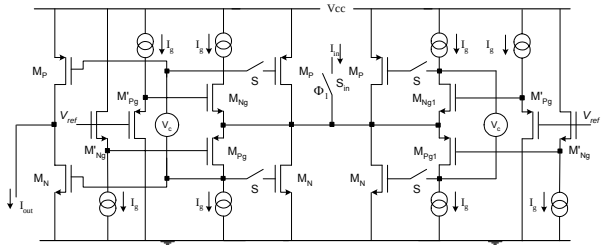


Figure 21. The backward SI integrator.

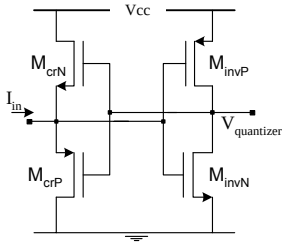


Figure 22. The quantizer.

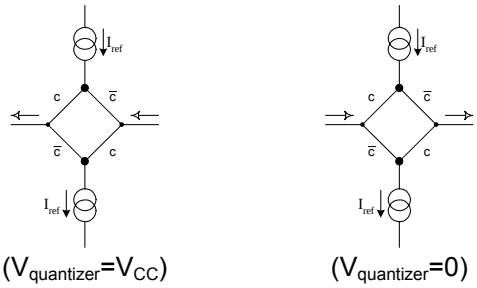


Figure 23. Functioning principle of the DAC.

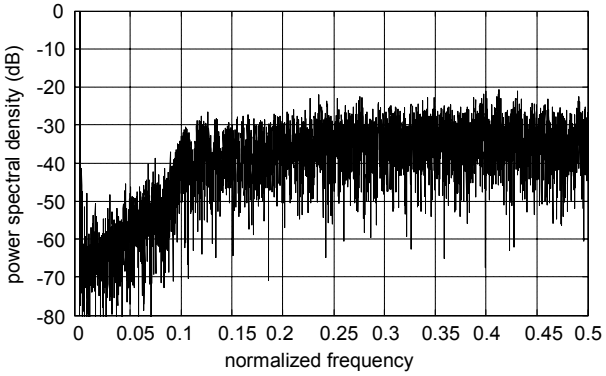


Figure 24. The modulator output power spectral density: cell of figure 11.a sampled at 80MHz.

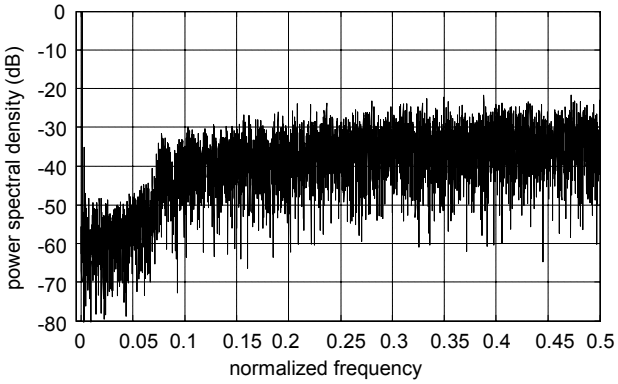


Figure 25. The modulator output power spectral density: cell of figure 11.c sampled at 80MHz.

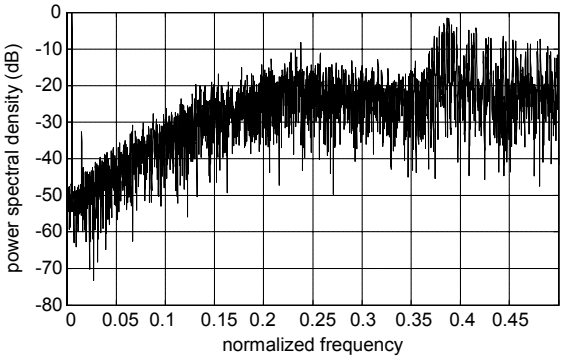


Figure 26. The modulator output power spectral density: cell of figure 11.a sampled at 1MHz.

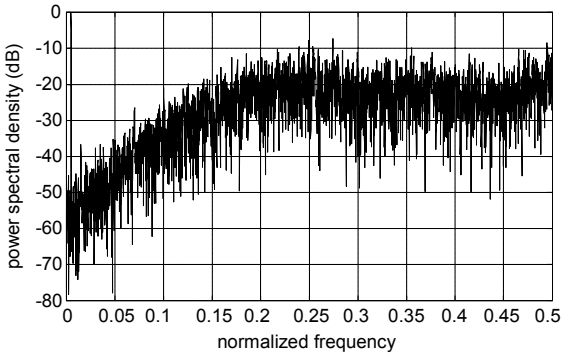


Figure 27. The modulator output power spectral density: cell of figure 11.c sampled at 1MHz.

At figures 26 and 27 we present a second application where the modulator was designed using sizes corresponding to those presented in [15] (see table III). The figures illustrate output-current power spectral densities, where the sampling frequency equals to 1MHz. We notice comparable aspects of noise rejection. SNR peaks are equal to 60dB and 50dB respectively for a 5kHz sinusoidal current input signal.

6. Conclusion

The presented work introduced the computational synthesis of voltage followers using joined pairs (nullators-norators) forming translinear loops. Three VFs were synthesized. They were used to implement three switched current class AB memory cells. Further, a heuristic was proposed, thanks to which performances of SI cells were maximized. The proposed optimization approach generated the Pareto front in the hyperspace linking two conflicting performances, i.e. SNR and time response. Since the memory cell is the fundamental building block of a $\Sigma\Delta$ SI modulator, second order SI modulators were designed using two 'optimised' SI cells. Spice simulations were presented to show good reached performances for the memory cells and the SI modulators, where it was proven that these circuits can be sampled up to 80MHz, while providing good behaviour against noise.

Appendix

Definition of Pareto-optimal front (taken from [18])

The concept of Pareto optimality is important to the analog sizing process because it usually aims at the minimization of several objectives simultaneously, i.e.,

$$\underset{x}{Minimize} \quad f(x) = [f_1(x) \cdots f_n(x)]^T$$

Such that $c(x) \geq 0$.

where $f \in \Re^n$, $c \in \Re^q$ and $x \in \Re^m$. $n \geq 2$.

This multiple-criteria or multiple-objective optimization problem leads to tradeoff situations where it is only possible to improve one performance at the cost of another.

A vector $a = [a_1 \cdots a_n]^T$ is considered superior to a vector $b = [b_1 \cdots b_n]^T$ if it dominates *b*, i.e.,

$$a \prec b \Leftrightarrow \underset{i \in \{1,\cdots,n\}}{\forall} (ai \leq bi) \wedge \underset{i \in \{1,\cdots,n\}}{\exists} (a_i < b_i)$$

With this definition, a performance vector f^* is Pareto-optimal if it is nondominated within the feasible solution space $\Im$, i.e.,

$$\neg \underset{f \in \Im}{\exists} f \prec f^*.$$

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