High performance voltage – mode multifunction filter with minimum component count

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Abstract: This paper presents a new second order multifunction filter using one active element, requiring only 'twelve' CMOS transistors, and four passive elements. The proposed circuit realizes voltage-mode low-pass, high-pass and band-pass functions with the advantages of minimum component count structure, high Q possibility, and high frequency potential. The proposed circuit is verified through PSPICE simulation results

Keywords: Analog filtering, multifunction filters, low cost, differential voltage current conveyor

1 Introduction

A number of filtering applications are now being handled with DSP techniques and digital filters, but there are still numerous situations where analog continuous time filters are either a necessity or provide a more economical solution. Among these are the interface circuits which connect the real world analog signals to the digital signal processor and provide band-limiting before the signals can be sampled for further processing with digital techniques, and reconstruction back to the analog world. Similarly, filtering requirements at very high frequencies require analog techniques where digital circuitry is not realistic and economical [1]. Over last two decades, current-mode active elements have become very useful for analog filtering applications due to their wide bandwidths, high slew rates and low power consumption. Several such active elements have evolved namely, current conveyors, current feedback amplifiers, current differencing buffered amplifier, current differencing transconductance amplifier, differential voltage current conveyors and many more [2-10]. Multifunction filters with capability of providing different filter responses are useful because of their versatility. As far as the topic of this paper is concerned, the multifunction filters based on a single active element are of interest. Such voltage-mode filters using different active elements have been reported in the literature [2-5]. The circuits presented in ref. [2, 4, 5] require more than four passive components, whereas, the circuit of ref. [3] is a minimum component count work.

This paper proposes new multifunction filter with minimum component count (four passive and one active), but the active element used (DVCC) has simpler realization than the one (FDCCII) used in the available circuit [3]. The simplicity refers to the number of transistors used in implementation. The circuit of ref. [3] is a single input multi output with high input impedance and grounded components, unlike the other category of multi input single output circuits [2,4,5]. The proposed circuit falls in the latter category of the available works [2, 4, 5], but with the distinct advantage of using a minimum component count. PSPICE simulation results using 0.5μ CMOS parameters are given to support the new proposed circuit.

2 Proposed Circuit

2.1 Circuit description

The differential voltage current conveyor (DVCC) is a special type of second-generation current conveyor with differential input capability at Y terminal. A DVCC with only Z+ stage is characterized by the following relationship.

$$V_{Y1}-V_{Y2} = V_X;\ I_{Y1}=I_{Y2} = 0;\ I_Z = I_X. \quad (1)$$

The CMOS implementation is shown in Figure 1. DVCC has recently become popular due to the differential input handling capability unlike the CCII [8]. Thereafter many applications of this active element were reported [9-11]. However, a voltage-mode second order multifunction filter employing a single DVCC has not been attempted in wealth of recent literature yet [12-15]. The new proposed multifunction filter circuit is shown in Figure 2. The circuit uses only Z+ stage thus resulting in a very simple configuration, requiring only 'twelve'

transistors for the active element. The circuit analysis using eqn. (1) yields the following output voltage expression:

$$V_o = \frac{s^2 V_2 + s\left(\frac{V_2}{R_1C_1} + \frac{V_1}{R_2C_2} - \frac{V_3}{R_1C_2}\right) + \frac{V_1}{R_1R_2C_1C_2}}{s^2 + s\left(\frac{1}{R_1C_1} + \frac{1}{R_2C_2} - \frac{2}{R_1C_2}\right) + \frac{1}{R_1R_2C_1C_2}} \quad (2)$$

Equation (2) suggests that the circuit of Figure 2 realize following filter functions with input and component conditions:

(i) $V_3=V_{in}$; $V_1=V_2=0$: BP
(ii) $V_3=V_2=V_{in}$; $V_1=0$; $C_1=C_2$: HP
(iii) $V_3=V_1=V_{in}$; $V_2=0$; $R_1=R_2$: LP

Thus the three basic filtering functions are realized. The LP and HP function realization require matching conditions in form of equal resistors and capacitors respectively. The filter parameters, namely pole-frequency, quality factor are as follows:

$$\omega_o = \frac{1}{\sqrt{R_1R_2C_1C_2}}; \quad Q = \frac{\sqrt{R_1R_2C_1C_2}}{R_1C_1 + R_2(C_2 - 2C_1)} \quad (3)$$

It is to be noted that the new circuit is a unique addition to the literature as a low cost versatile filter. As far as the realization of other two second order functions is concerned, it should not be seen as a drawback keeping in view the simplicity of the new circuit. Next, it may be argued that the circuit lacks the ideal high input impedance [10-14]. It is a well known fact that, with a three input single output system, using a simple (and single) active element along with four components, fulfilling this requirement is not possible. Similar arguments hold true for the use or otherwise of grounded components.

2.2 Circuit Design

The circuit can be designed for a desired Q (even, Q>1). For example, the realization of high-pass function requires equal capacitor design, in which case Q becomes:

$$Q = \frac{\sqrt{R_1R_2}}{(R_1 - R_2)} \quad (4)$$

Equation (4) suggests that Q> 1 is quite possible with proper design. This design is also suited for realizing band-pass function, though capacitive matching is not a restriction in that case. Similarly, for low-pass function, equal resistor design is required for realization. In this case Q becomes:

$$Q = \frac{\sqrt{C_1C_2}}{(C_2 - C_1)} \quad . \quad (5)$$

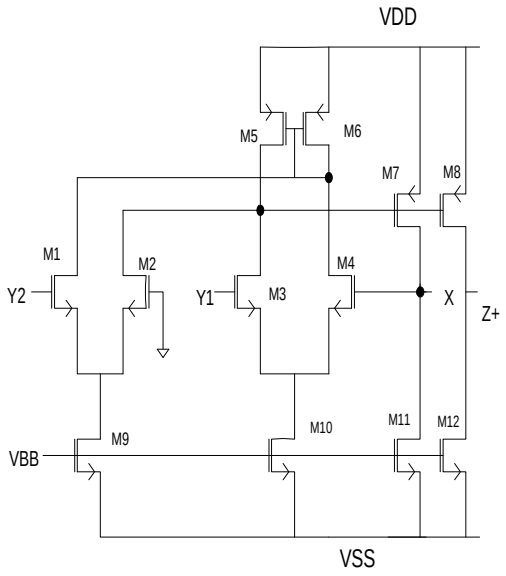

Fig. 1: DVCC implementation.

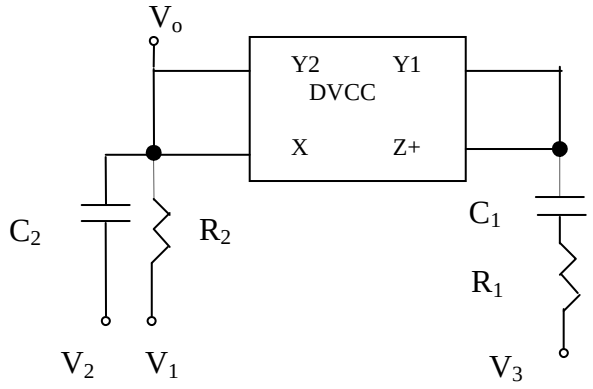

Fig. 2: Proposed multifunction filter.

Equation (5) imply that Q>1 is possible with proper design. Next, the filter gains are analyzed from eqn. (2) and found as:

$H_{LP}=H_{HP}=1; H_{BP}=-R_2/(R_1-R_2)$ (6)

For band-pass response, the above gain is for equal capacitor design.

2.3 Sensitivity analysis

Sensitivity figures of the filter parameters (eqn. 3) for the proposed circuit are next analyzed. Pole-frequency sensitivity is found to be 0.5 for all

elements. Pole-Q sensitivity for resistive and capacitive elements is respectively found as:

$$S_{R2}^{Q} = -S_{R1}^{Q} = \frac{R_1C_1 - R_2(C_2 - 2C_1)}{2[R_1C_1 + R_2(C_2 - 2C_1)]} \quad (7)$$

$$S_{C2}^{Q} = -S_{C1}^{Q} = \frac{R_1C_1 - R_2(C_2 + 2C_1)}{2[R_1C_1 + R_2(C_2 - 2C_1)]} \quad (8)$$

For equal capacitor design, the sensitivity of pole-Q to resistive elements becomes:

$$S_{R2}^{Q} = -S_{R1}^{Q} = \frac{R_1 + R_2}{2(R_1 - R_2)} \quad (9)$$

$$S_{C2}^{Q} = -S_{C1}^{Q} = \frac{R_1 - 3R_2}{2(R_1 - R_2)} \quad (10)$$

Thus the above eqns. (9-10) apply to the high-pass and band-pass design; though capacitive matching is not a condition for band-pass design. Further, it is emphasized that the sensitivity (in eqns. 9-10) can never become infinite, as the resistors cannot be taken equal for a practical high-pass circuit design (please refer eqn. 4). Next, for the equal resistor design, the sensitivity figures become:

$$S_{R2}^{Q} = -S_{R1}^{Q} = \frac{3C_1 - C_2}{2(C_2 - C_1)} \quad (11)$$

$$S_{C2}^{Q} = -S_{C1}^{Q} = -\frac{(C_2 + C_1)}{2(C_2 - C_1)} \quad (12)$$

The above eqns. (11-12) apply to the low-pass design which requires resistive matching. Again, the eqns. (11-12) does not imply infinite sensitivity as the capacitors cannot be equal for low-pass design (please refer eqn. 5). The numerical values of the sensitivities for the design used for presentation of results shall be given in the following section.

3 Simulation Results

3.1 Band-pass and high-pass

The proposed circuit is simulated using the CMOS implementation of Fig. 1 and device parameters as also listed in Table 1 and 2. The same has been successfully employed in many of the recently reported works based on DVCC applications [9-11]. The supply voltage used is ±2.5V. The circuit was designed with C_1=C_2=1pF for high-pass and band-pass responses. The resistors used were R_1=41.6KΩ and R_2=20KΩ so as to result in the pole-frequency as 5.6MHz and pole-Q as 1.4. The gain plots for band-pass and high pass functions are shown in Figure 3 and 4 respectively. The pole-frequency as obtained from figures 3 and 4 is found as 5.6MHz and pole-Q is 1.4, which very well match with the designed values. Input/Output wave-shapes for band-pass filter function are also given in Figure 5 at the centre frequency of 5.6MHz. The THD at the output is 1.2%. Good results were obtained even for higher amplitudes of signal. As far as the sensitivity of pole-Q for high-pass and band-pass design is concerned, it is 0.4 for capacitive elements and 1.4 (same as Q) for resistive elements.

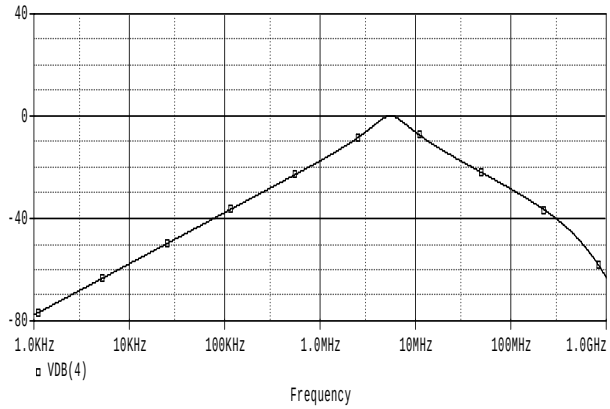

Fig. 3: Gain plot for band-pass filter.

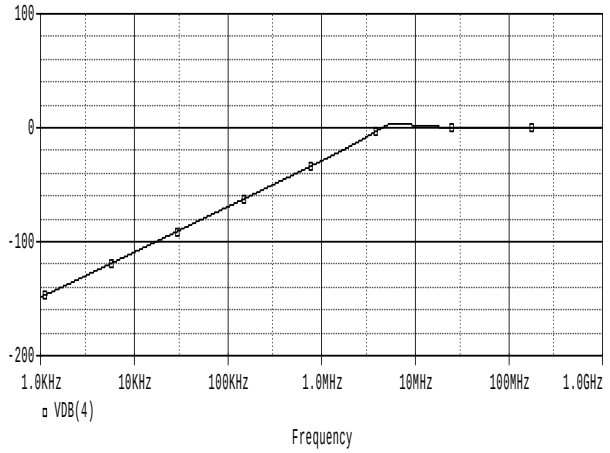

Fig. 4: Gain plot for high-pass filter.

3.2 Low-pass

Next the circuit was designed for low-pass function with R_1=R_2=20KΩ and C_1=1pF, and C_2=2pF. The designed pole-frequency was 5.6 MHz and pole-Q as 1.4. The simulated results for low-pass function are given in Figure 6, with the pole-frequency and pole-Q same as the designed values. The input/output waveforms for low-pass filter at 5MHz are also shown in Figure 7. The THD at the output is 1.1%. The sensitivity of pole-Q for the design is 0.5

for resistive elements and 1.5 for capacitive elements.

4 Practical considerations

4.1 DVCC non-idealities Having presented the new multifunction filter circuit along with its well convincing results, a more realistic viewpoint is taken into consideration by redefining a practical DVCC.

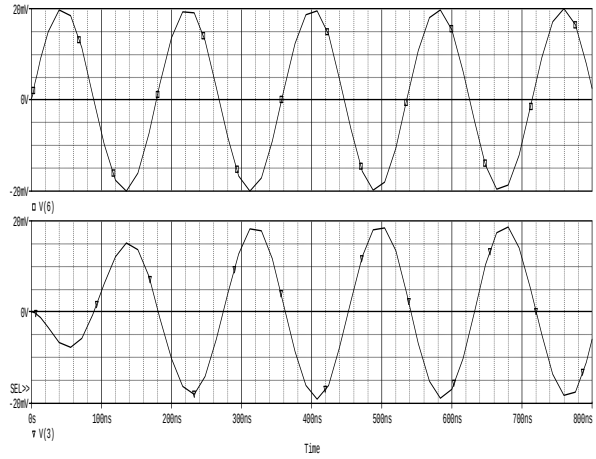

Fig. 5: Input/Output band-pass waveforms at 5.6MHz.

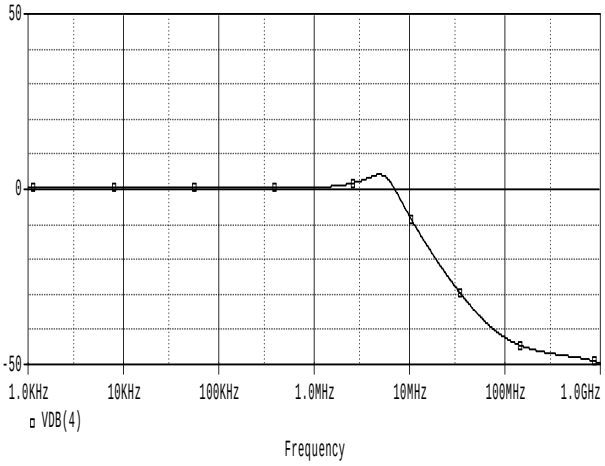

Fig. 6: Gain plot for low-pass filter.

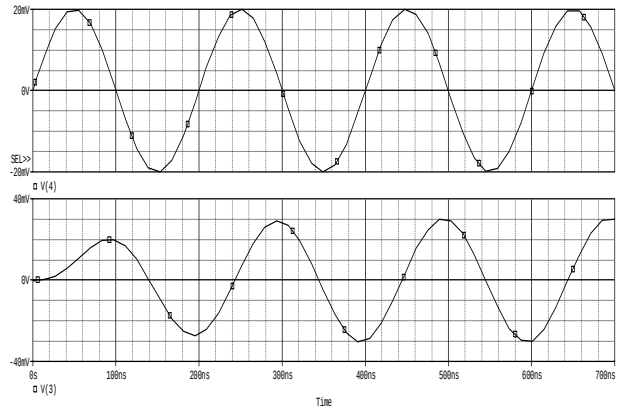

Fig.7: Input/Output low-pass waveforms at 5MHz.

A current conveyor is characterized by non-unity transfer gains that depend on the technology and the device dimensions. A DVCC with only Z+ output (as the proposed circuit does not use Z- output) can also be defined taking into account this practical aspect:

$$\beta_1 V_{Y1} - \beta_2 V_{Y2} = V_X;\ I_{Y1} = I_{Y2} = 0;\ I_Z = \alpha I_X \quad (9)$$

Here, β_1 and β_2 are the voltage transfer gains from Y1 and Y2 terminal respectively to the X terminal and α is the current transfer gain from X terminal to the Z+ terminal. The above transfer gains deviates unity by the voltage and current transfer errors, which are quite small and technology dependent. Moreover, the transfer gains, instead of being real, are actually frequency dependent with an upper bound on the usable frequency. For DVCC, these gains remain unity till 10's of MHz. Thus good results are obtained at the frequency of 5.6MHz as already evident in the previous section. A re-analysis of the proposed circuit results in modified output voltage expression, and the filter parameters as

$$\omega_o = \sqrt{\frac{\alpha}{R_1 R_2 C_1 C_2}};\quad Q = \frac{\sqrt{\alpha R_1 R_2 C_1 C_2}}{\alpha R_1 C_1 + R_2[C_2 - (1+\beta_2)C_1]} \quad (10)$$

Slight deviations are expected in the results due to the appearance of non-ideality terms in the above eqn. However, these deviations are negligible as also evident from the simulated results. In fact the results obtained do not reflect any deviation. The deviation, for instance in pole-frequency (MHz) is in third place of decimal. Similar statement holds for pole-Q as well. It is therefore quite evident that the proposed circuit is not adversely affected by the DVCC non-idealities.

4.2 DVCC Parasitics

The effect of various parasitic impedances at DVCC ports is next considered. Since V_3 is always to be connected to the signal input, port Z+ (along with Y_1) impedances comprising $R_Z//R_Y//C_Z//C_Y$ would be effective. Though port Y_2 (along with X) parasitic capacitance become ineffective when V_2=0 (it merges with C_2) but the parasitic resistance R_Y does appear across C_2. Similarly, the parasitic resistance at port Y_2 gets ineffective when V_1=0 (it merges with R_2), but C_Y does appear across R_2.

4.3 Inputs' selection

The new proposed multifunction filter enjoys a minimum component count and a very compact realization. There are certain aspects which need to

be practically considered. Firstly, the input impedance may not be high and even frequency dependent in certain cases. Secondly, one of the three inputs nodes (V_3) is always to be connected to the input signal; whereas, the rest two nodes need be switched for different filtering functions (eqn. 2 and subsequent discussion). A switching network may be employed at the inputs' end and the circuit may even be made digitally controllable with a two-bit control for selecting one of the two inputs namely V_1 or V_2. This aspect may further be utilized to also make the input impedance desirable for voltage mode operation by appropriate design of the switching network.

4.4 Integration aspect

Another important aspect to be considered is the feasibility of integrating the circuit. It is to be noted that the proposed circuit employs floating capacitors, which can be integrated using double-poly process. Next, the resistors need to be replaced with tunable active equivalents (in CMOS technology) for most practical purpose. The circuit can thus be made voltage controllable so as to tune the filter parameters through external control voltage(s). Therefore, the new multifunction filter is integrable in CMOS technology.

5 Conclusion

A novel voltage-mode multifunction filter circuit employing minimum number of active and passive components, realizing low-pass, band-pass and high-pass filter functions is proposed. The new circuit is verified through PSPICE simulation results. The proposed circuit is a useful addition to the literature as a low cost and high frequency filtering option with CMOS compatibility. It is expected to act as a useful building block for designing higher order filters as well.

Table 1: Device dimensions used

Transistors	L(μm)	W(μm)
M1, M2, M3, M4	1	1.6
M5, M6	1	8
M9, M10	1	29
M7, M8,	1	20
M11, M12	1	90

Table 2: Parameters used

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NMOS :
LEVEL=3  UO=460.5 TOX=1.0E-8 TPG=1
VTO=.62 JS=1.8E-6 XJ=.15E-6 RS=417
RSH=2.73 LD=0.04E-6  ETA=0
VMAX=130E3 NSUB=1.71E17 PB=0.761
PHI=0.905 THETA=0.129 GAMMA=0.69
KAPPA=0.1 AF=1 WD=0.11E-6 CJ=76.4E-5
MJ=0.357 CJSW=5.68E-10 MJSW=0.302
CGSO=1.38E-10 CGDO=1.38E-10
CGBO=3.45E-10 KF=3.07E-28 DELTA=.42
NFS=1.2E11
 PMOS:
 LEVEL=3  UO=100 TOX=1.0E-8 TPG=1
VTO=-0.58 JS=.38E-6  XJ=0.1E-6 RS=866
RSH=1.81 LD=0.03E-6 ETA=0
VMAX=113E3 NSUB=2.08E17 PB=0.991
PHI=0.905  THETA=0.120 GAMMA=0.76
KAPPA=2 AF=1 WD=0.14E-6 CJ=85E-5
MJ=0.429 CJSW=4.67E-10 MJSW=.631
CGSO=1.38E-10 CGDO=1.38E-10
CGBO=3.45E-10 KF=1.08E-29 DELTA=0.81
NFS=0.52E11
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