

Current-mode filters with high output impedance and employing only grounded components

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Abstract: This paper presents several new current-mode second order filters suited for low-Q applications. The new circuits employ only grounded components and possess high output impedance, ideal for current-mode cascading. Effects of non-idealities and parasitics are also discussed. The new circuits possess good active and passive sensitivity performance. PSPICE simulation results are included for verification of proposed circuits.

Keywords: Current-mode, analog signal processing, active filter, differential voltage current conveyor

1 Introduction

Current-mode circuits have become quite popular for their potential advantages over the voltage-mode counterparts [1-3]. Current-mode analog signal filtering has also received a lot of attention in the recent past. The technical literature has thus been flooded with numerous new circuit realizations [4-18]. Current-mode filters with high output impedance offer easy cascading and are quite desirable for realizing higher order filters as well. Recently CDTA has also been used for current-mode filtering application [5]. The circuit of ref. [6] realizes three basic filtering functions at high output impedance and uses all grounded components. The circuit in ref. [7] is based on minimum number of passive elements. Another current mode work employs only one active element in form of a CFOA [8]. One multifunction filter using two CDBAs was also reported [9]. Current mode universal filter of ref. [12] falls in a separate category of electronically tunable filters and also benefits from cascaded outputs and use of grounded components. An active element which has also emerged as a potential candidate for realizing filter circuits is differential voltage current conveyor [10-11, 13-16]. The works based on DVCC present a KHN biquad [10] and higher order low-pass filters [11] both benefiting from high output impedance outputs. Another very recent current-mode work also enjoys the use of only grounded components and high output impedance [15]. However, the work requires input current insertion at different nodes for realizing different functions. In some cases, additional active elements are required for making multiple copy of input current. Moreover, the work also suffers from

the drawback of using matching conditions for realizing two functions [15].

This paper presents several second order low-Q current mode filter circuits employing grounded components and with high output impedance. Low-Q filters find applications, for instance in anti-aliasing, graphic equalizers etc [8, 17]. Moreover the circuits using grounded components are beneficial from fabrication viewpoint. The non-ideal study and parasitic effects are also given. The new circuits are verified using PSPICE, a powerful tool for verifying new circuits based on active elements, which are either not commercially available or their implementation using available ICs is not very economical.

2 Proposed Circuits

The differential voltage current conveyor (DVCC) is characterized by the following port relationship [14]

$$V_x = V_{Y1} - V_{Y2}; I_{Y1} = I_{Y2} = 0; I_{Z+} = I_x; I_{Z-} = -I_x \quad (1)$$

The new proposed current-mode filter circuits are shown in Fig. 1. The new circuits are derived using the cascade approach, from the first order filters recently reported in literature [13]. The same are shown here as Fig. 2 for easy reference [13]. Circuit analysis using eqn. (1) yields the following current transfer functions for the circuits of Fig. 1.

$$\text{Fig. 1(a): } \frac{I_o}{I_{in}} = \frac{s^2}{D(s)} \quad (2a)$$

$$\text{Fig. 1(b): } \frac{I_o}{I_{in}} = \frac{1/4R_1R_2C_1C_2}{D(s)} \quad (2b)$$

$$\text{Fig. 1(c): } \frac{I_o}{I_{in}} = -\frac{s/2R_2C_2}{D(s)} \quad (2c)$$

Fig. 1(d):

$$\frac{I_o}{I_{in}} = \frac{s^2 - s(1/2R_1C_1 + 1/2R_2C_2) + 1/4R_1R_2C_1C_2}{D(s)} \quad (2d)$$

Fig. 1(e): $\frac{I_o}{I_{in}} = \frac{2(s^2 + 1/4R_1R_2C_1C_2)}{D(s)}$, (2e)

where

$$D(s) = s^2 + s(1/2R_1C_1 + 1/2R_2C_2) + 1/4R_1R_2C_1C_2 \quad (3)$$

It is seen from eqn. (2) that high-pass (HP), low-pass (LP), band-pass (BP), all-pass (AP) and band-reject (BR) filter functions are realized from the circuits of Figure 1 (a-e) respectively. It may be noted that BR and AP realization requires additional current followers (like the recent work of ref. 15) to duplicate the input current and finite current transfer gain (α) would cause for some non-ideality. The filter gains, pole-frequency and quality factor are found as:

Gains: $H_{HP}=H_{LP}=H_{AP}=1$; $H_{BR}=2$;
 $H_{BP} = -R_1C_1 / (R_1C_1 + R_2C_2)$ (4)

Polefrequency $\omega_o = 1/2\sqrt{R_1R_2C_1C_2}$ (5)

Bandwidth $\omega_o/Q = (1/2R_1C_1 + 1/2R_2C_2)$ (6)

Quality factor $Q = \frac{\sqrt{R_1R_2C_1C_2}}{2(R_1C_1 + R_2C_2)}$ (7)

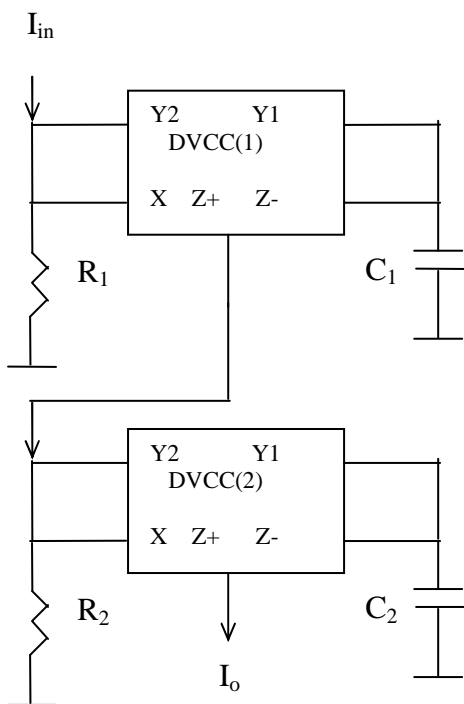


Fig. 1a: Proposed high-pass filter.

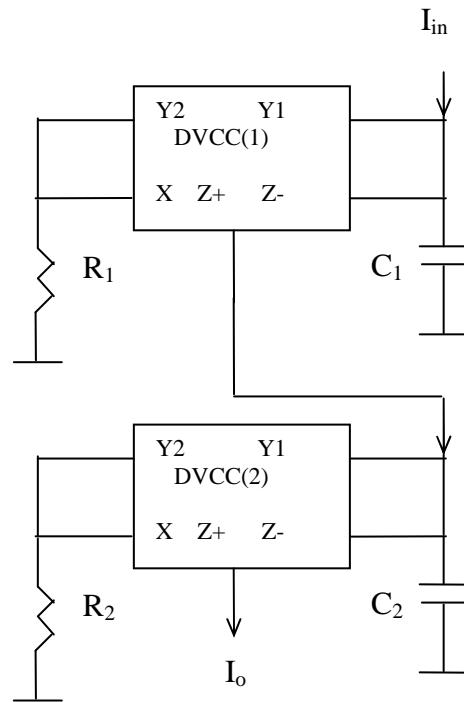


Fig. 1b: Proposed low-pass filter

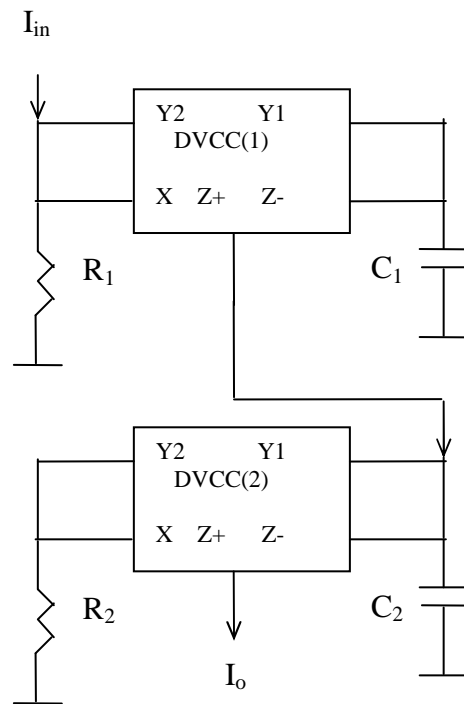


Fig. 1c: Proposed band-pass filter.

It is evident from eqns. (5-7) that the proposed circuits have low-Q capability. But it is not to be seen as a drawback, because of the simplicity of the realization approach, the circuit structure, along with the high output impedance feature. The sensitivity of pole-frequency and pole-Q to passive

components is within 0.5 in magnitude and becomes '0' for equal valued resistor and capacitor design. Thus the proposed circuits exhibit good sensitivity performance.

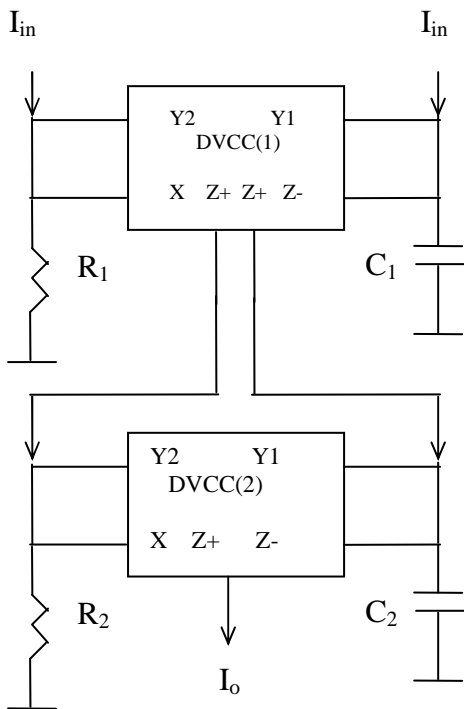


Fig. 1d: Proposed all-pass filter.

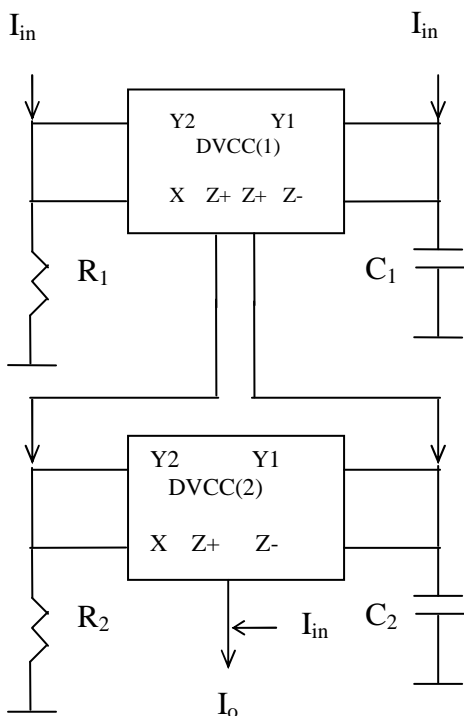
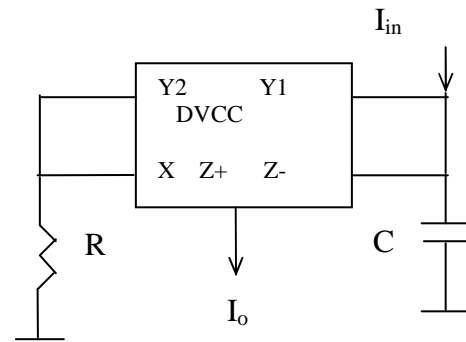
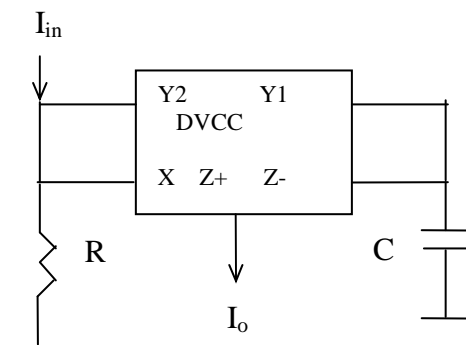


Fig. 1e: Proposed band-reject filter.

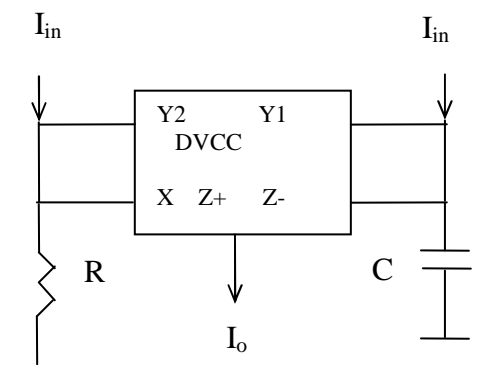
It is further to be noted that the circuits of Fig. 1(a-c) are based on DVCC with both Z+ and Z- outputs, but the all-pass and band-reject filters of Fig. 1 (d and e respectively) employ one of the two DVCCs with an additional Z+ stage. This is easily incorporated by using two additional steering transistors to implement an additional Z+ output in the DVCC implementation [13].



$$(a) \frac{I_o}{I_{in}} = \frac{1/2RC}{s + 1/2RC}$$



$$(b) \frac{I_o}{I_{in}} = \frac{-s}{s + 1/2RC}$$



$$(c) \frac{I_o}{I_{in}} = -\frac{s - 1/2RC}{s + 1/2RC}$$

Fig. 2: First order (a) Low-pass, (b) High-pass, and (c) All-pass building blocks used in the biquads filters of Fig. 1 [13].

3 Non-ideal study

3.1 DVCC non-idealities

The non-ideal DVCC is characterized by the following relationship.

$$V_x = \beta_1 V_{y1} - \beta_2 V_{y2}; I_{y1} = I_{y2} = 0; I_{z+} = \alpha_1 I_x; I_{z-} = -\alpha_2 I_x \quad (8)$$

The voltage transfer gains β_1 from Y_1 to X , and β_2 from Y_2 to X deviate from unity by voltage transfer errors. Similarly, the current transfer gains α_1 from X to $Z+$ and α_2 from X to $Z-$ deviate from unity by the current transfer errors [13]. These errors are expected to be quite low for an integrated DVCC, thus making voltage and current transfer gains to approach unity. The first three circuits of Figure 1 are re-analyzed using eqn. (8) to yield the following non-ideal current transfer functions.

$$\text{Fig.1(a): } \frac{I_o}{I_{in}} = \frac{\alpha_{11}\alpha_{12}s^2}{D(s)} \quad (9a)$$

$$\text{Fig.1(b): } \frac{I_o}{I_{in}} = \frac{\alpha_{11}\alpha_{12}\beta_{11}\beta_{12} / 4R_1R_2C_1C_2}{D(s)} \quad (9b)$$

$$\text{Fig.1(c): } \frac{I_o}{I_{in}} = -\frac{\alpha_{11}\alpha_{12}\beta_{12}s / 2R_2C_2}{D(s)} \quad (9c)$$

where

$$D(s) = s^2 + s(\alpha_2\beta_1/2R_1C_1 + \alpha_2\beta_2/2R_2C_2) + \alpha_2\alpha_1\beta_1\beta_2/4R_1R_2C_1C_2 \quad (10)$$

Similar results are obtained for the all-pass and band-reject, as these are only derived from the above. The sensitivity of filter parameters to the current and voltage transfer gains are analyzed and found within 0.5 in magnitude which suggests good sensitivity performance.

It is to be noted that the current and voltage transfer gains are frequency dependent, with a first order roll-off. These are however, found to be unity up to 10's of MHz and the exact value may vary for different technology and device dimensions.

3.2 DVCC Parasitics

Next, the effects of various parasitic capacitances are to be considered. It was recently shown that these parasitics do not adversely affect the basic circuit topology used in this work [13]. However, it is worth to be noted that parasitic capacitances at various ports do cause some concern. For instance, in all the proposed circuits, the port parasitic capacitances either merge with external capacitors or appear in shunt with external resistors. In the former case, since the external capacitors chosen in design are in excess to the expected parasitic capacitances, their effect is not noticeable. In the latter case, where these appear in shunt with external

resistors, the transfer functions actually get modified by way of an additional high frequency root. But again as this root lies at very high frequencies (since parasitic capacitance is in order of pF's and external resistor is also within a few Kohms), their effects do not get noticeable at working frequencies.

4 Simulation results

The new proposed circuits are verified through PSPICE simulations. The DVCC was simulated using the parameters as listed recent ref. [13]. The supply voltage used was $\pm 2.5V$. The circuits were designed with equal value capacitors of value 1nF, and equal resistors of value 1K Ω . The designed pole-frequency is 80 KHz and pole-Q is 0.5. The simulation results are shown in Figure 3-5. Figures 3-5 respectively shows the band-pass, band-reject and all-pass responses. The pole-frequency in each case is found to be 80 KHz, which matches the designed value. Next, the time domain responses for all-pass circuit are shown with input signal at pole-frequency. The input and output waveforms (Figure 6) are out of phase as desired for second order all-pass function at pole-frequency. Figure 7 shows the input/output waveforms at 1.8MHz, where the phase-shift becomes -360 $^\circ$, thus confirming circuit's performance even at high frequencies.

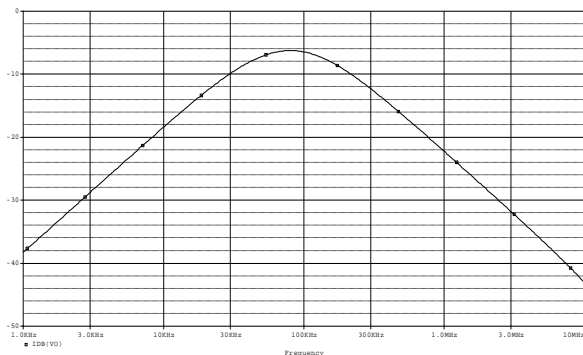


Fig. 3: Band-pass response.

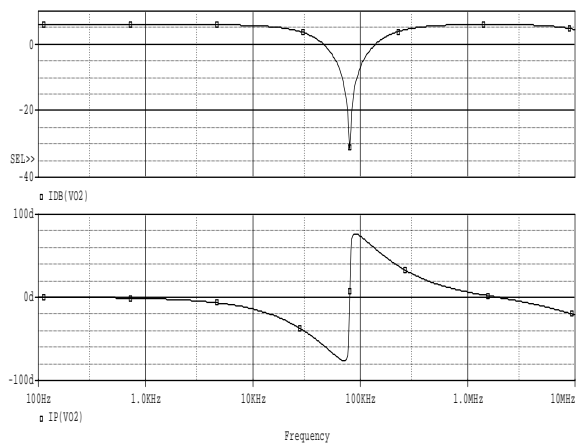


Fig. 4: Band-reject gain and phase response.

5 Conclusion

New current-mode second order filters, each using only two DVCCs and grounded passive components suited for low-Q (≤ 0.5) applications are proposed. The five new circuits realize all the standard second order filter functions at high output impedance. The new circuits are based on the recently reported first order filters [13]. The proposed circuits require no matching conditions for realizing any filtering function, unlike a recent work based on equal number of active and passive components [15]. The circuits also possess good sensitivity performance. Effects of DVCC non-idealities and parasitics are also discussed. PSPICE simulation results confirm the practical utility of the proposed circuits. Current-mode applications of DVCC continue to find recent attention in technical literature [19].

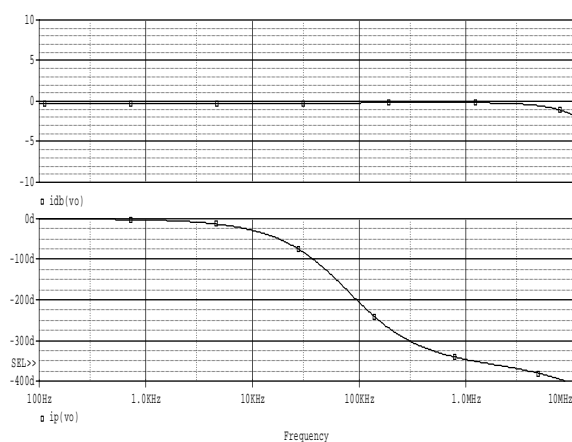


Fig. 5: All-pass gain and phase response.

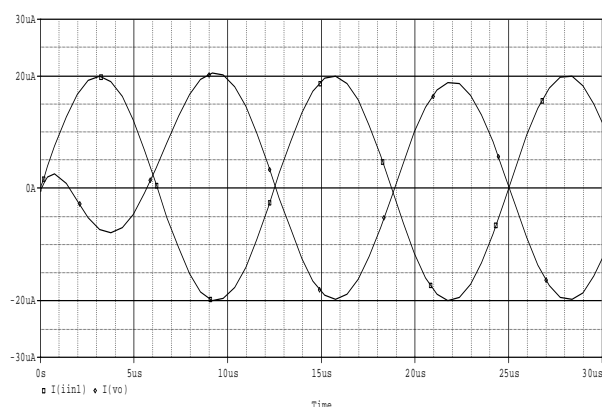


Fig. 6: Input/output of all-pass filter at pole-frequency (80KHz).

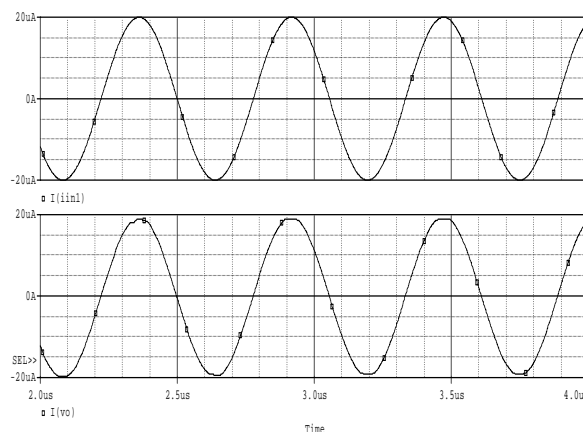


Fig. 7: Input/Output of all-pass filter at 1.8MHz.

Acknowledgements: The author is thankful to the anonymous reviewers for useful comments. The author is also grateful to the guest editors for recommending the paper.

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