Comparative Performance of Low Voltage CMOS - CFOA Suitable for Analog VLSI

R.K. NAGARIA, M. GOPI KRISHNA & RAKESH KR. SINGH
Department of Electronics and Communication Engineering
Motilal Nehru National Institute of Technology
Allahabad- 211004
INDIA
Ph(O): 0532-2271464
rkn@mnnit.ac.in, gopikrishna07@yahoo.com, rks_sat@rediffmail.com

Abstract: The performance of the low voltage CMOS-CFOA with different aspect ratios is presented in this paper.The solution works using a low supply voltage and provides a wide input/output swing as well as a high current driving capability. The circuit allows almost a rail-to-rail input and output operation and it provides high driving capabilities. The CFOA is operating at supply voltages of ± 0.75V.The circuit exhibits better than 100 MHz bandwidth and ± 1mA current drive capability. The CMOS CFOA is simulated in Pspice using 0.35µm and 0.25µm TSMC technology. The circuit exhibits better performance particularly greater bandwidth and low power consumption with improved dynamic range after resizing the aspect ratios using 0.35µm to 0.25µm CMOS technology. The simulation results are promising and the resized structure is suitable for analog/mixed-mode VLSI design.

Key Words- CMOS CFOA, High performance, Low Voltage, Low Power.

1. Introduction

The analysis and design of current feedback op-amp and current-conveyor integrated circuits [1-12] has given great importance, because these circuits exhibit better performance, mainly higher speed and better bandwidth, than classic voltage-mode operational amplifiers (VOA). The current feedback operational amplifier (CFOA) closed loop bandwidth is independent of its closed loop gain (provided that the feedback resistance is kept constant and much higher than the CFOA inverting input resistance) [6] unlike VOA-based circuits, which are limited by a constant gain-bandwidth product. The symbolic form of CFOA was shown in Fig. 1(a) and its four-port network which has a describing matrix of the following form:

$$\begin{bmatrix} I_y \\ V_x \\ I_z \\ V_o \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ V_z \\ I_o \end{bmatrix} \quad (1)$$

Several CMOS realizations for the CFOA have been reported in the literature [4-7], [9-12].

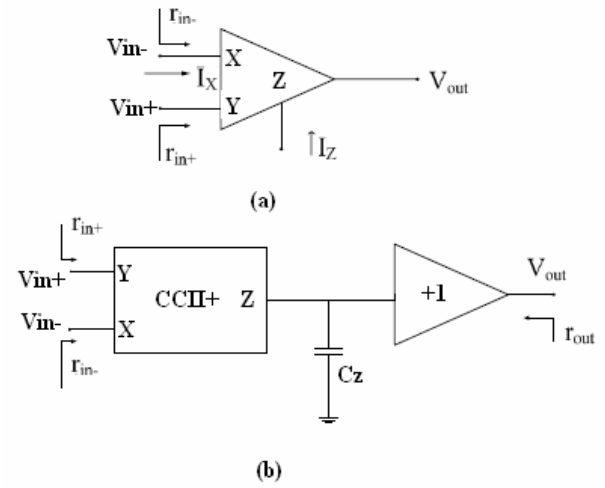


Figure 1. (a) Current feedback op-amp symbol, (b) CFOA block diagram

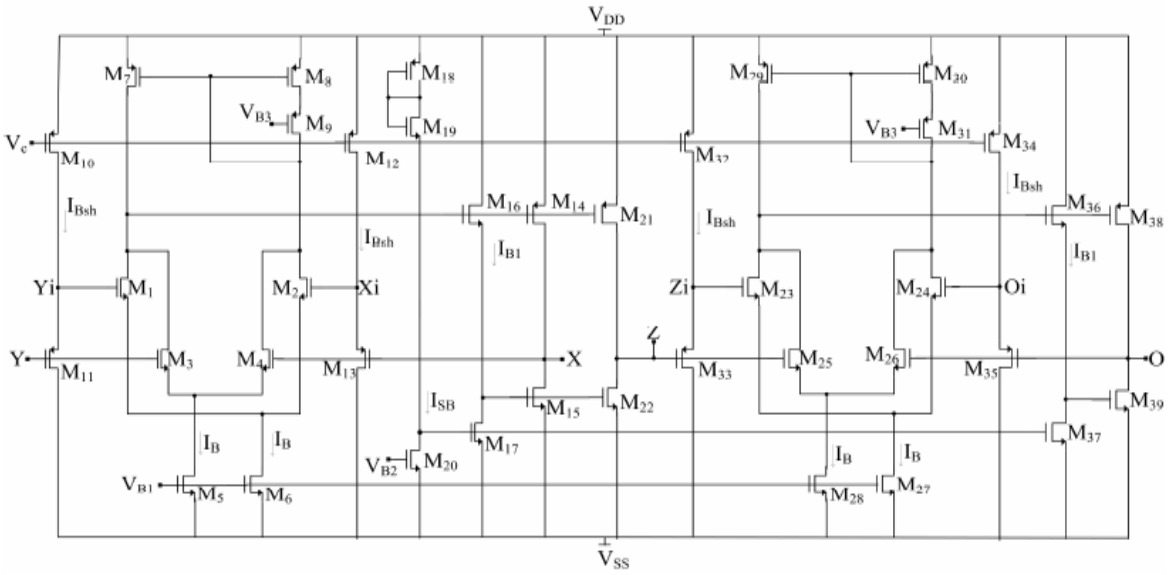


Figure 2. Structure of CMOS CFOA for different aspect ratios

The CFOA has always been seen as an extension of the second generation current conveyor (CCII); therefore, the design approach was to cascade a CCII+ with a voltage follower to realize the complete circuit [2]. Several CMOS CFOA implementations have been presented to provide offset compensation [4], high current drive capability [5-6] and bandwidth. The low-power/low-voltage issue, which is increasingly important in very large scale integrated (VLSI) circuits, was partially addressed in [9]. In this paper, a CMOS CFOA is discussed. The CFOA is capable of operating under a minimum supply voltage (|VTp|+VTn+VDS, sat) and with reduction in total power dissipation. The circuit includes a class AB output stage exhibiting high current drive capability and good power conversion efficiency. A rail-to-rail input and output voltage operation is also nearly achieved.

2. Circuit Description of CMOS CFOA

A CFOA can be realized by using the second generation current conveyor cascaded with a voltage follower [2], as shown in Fig. 1(b). The CMOS realization of the proposed CFOA, shown in Fig. (2), consists of two matched parallel connected n-differential pairs (M_1, M_2) and (M_3, M_4), two matched biasing current source transistors (M_5, M_6), cascoded current mirror formed of two matched transistors (M_7, M_8), transistor (M_9), and two pairs of matched source followers transistors (M_{10}, M_{11}) and (M_{12}, M_{13}). Transistors M_5 and M_6 carry equal biasing currents (I_B), while transistors (M_{10}, M_{11}) and (M_{12}, M_{13}) produce a positive voltage shift for the input voltage applied on transistor M_{11} and M_{13}, respectively. All transistors are operating in the saturation region, the gates controls the shifting value as follows,

$$V_{Yi} = V_Y + (V_{DD} - V_C) \quad (2)$$

$$V_{Xi} = V_X + (V_{DD} - V_C) \quad (3)$$

Where V_{Yi} and V_{Xi} are the output voltages from the source followers, V_Y is the high input impedance voltage, and V_X is the low input impedance terminal. For V_Y and V_X voltages are close to the negative supply voltage V_{SS} ($V_{SS} \leq V_Y, V_X < 2V_{Tn} + V_{SS}$), the current source transistor M_5 and, hence, the differential pair M_3 and M_4 are cut-off. Then, the small and large signal behavior of the whole circuit result only from the contribution of the differential pair M_1 and M_2, biased with current source transistor M_6. When V_Y and V_X voltages are in between negative and positive supply voltages ($2V_{Tn} + V_{SS} \leq V_Y, V_X < V_C + 2V_{Tn} + 2V_{DD}$), both input pairs (M_1-M_2) and (M_3-M_4) are active and the small and large signal behavior of the whole circuit

result from the contribution of both differential pairs. 3: Finally, when V_Y and V_X are very close to V_{DD} the positive supply voltage ($V_C + 2V_{Tn} - 2V_{DD} \leq V_Y, V_X \leq V_{DD}$), the current sources of the shifters M_{10} and M_{12} are cut-off. Therefore, the small and large signal behavior of the whole circuit contribution result only from the differential pair M_3 and M_4 biased with current source transistor M_5. This ensures a rail-to rail operation.

The structure of the CFOA input stage (voltage follower) requires that the X terminal must have low input impedance. A suitable buffer circuit should be used to fulfill this condition and to provide a rail-to-rail swing capability. Transistors (M_{14}-M_{20}) fulfill the required buffering action with a rail-to-rail swing capability. Transistors M_{14} and M_{15} form the push pull output stage at the X terminal, transistors M_{16} and M_{17} are level shifting transistors providing proper biasing for transistor M_{15}. This push-pull action of M_{14} and M_{15} reduce the power dissipation.. The standby power consumption of the overall circuit for dual power supply is given by:

$$P_{SB} = 2V_{DD}(4I_{SB} + 4I_B + 4I_{Bsh} + 2I_{B1}) \quad (4)$$

The last term in the above equation is the current passing through the level shifting transistors (M_{16} and M_{17}). This current can be kept small by choosing small aspect ratio for transistors (M_{16} and M_{17}). The class AB output stage enables the circuit to drive the heavy resistive and capacitive load with low standby power dissipation and no slewing. Transistors M_7 and M_8 force the currents in transistors M_1 and M_3 to be equal to the currents in transistors M_2 and M_4.Therefore,

$$I_{M1} + I_{M3} = I_{M2} + I_{M4} \quad (5)$$

From (5), the matched differential pair transistors are carrying equal currents. Therefore,

$$V_X = V_Y \quad (6)$$

The current follower stage, as shown in Fig. (2) is made up of transistors (M_{21}, M_{22}). They are conveyed the X terminal current into the Z terminal current. Therefore,

$$I_Z = I_X \quad (7)$$

Finally, a suitable buffer must be available between the Z and O terminals and consisting from transistors M_{23} to M_{39}. This yield,

$$V_o = V_z \quad (8)$$

3. Small Signal Analysis of CMOS CFOA

A generalized small-signal model of the proposed CMOS CFOA is shown in Fig. (3). For Small signal analysis when both differential stages are properly working, the open loop gain T(s) is given by

$$T(s) = \left(\left(\frac{g_{m11} \times R_{ds1}}{1 + g_{m11} \times R_{ds1}} \right) \times g_{m1} + g_{m3} \right) \times R_{ds2} \times g_{m14} \times R_{ds3} \quad (9)$$

Where $R_{ds1} = (r_{ds11} \,//\, r_{ds10})$, $R_{ds2} = (r_{ds7} \,//\, r_{ds1} \,//\, r_{ds3})$ and $R_{ds3} = (r_{ds14} \,//\, r_{ds15})$ and r_{ds} is the drain to source resistance , g_m is the transconductance.

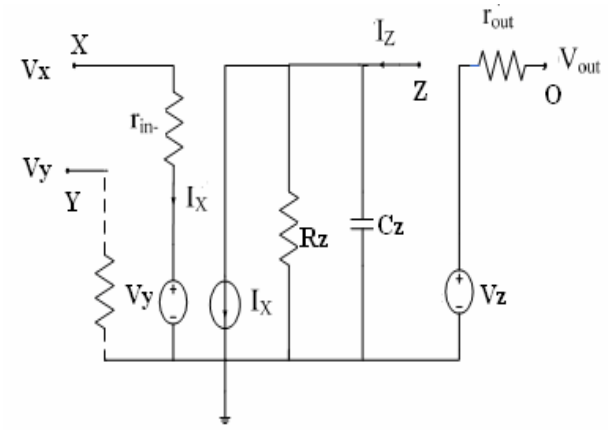


Figure (3). Small signal model of Proposed CMOS CFOA

The Voltage gain between the terminals Y and X becomes

$$A_v(s) = \frac{V_x(s)}{V_y(s)} = \frac{1}{\left(1 + \frac{1}{T(s)}\right)} \quad (10)$$

For high Values of T(s), $A_v(s)$ tends to 1.The CFOA input resistance at the X terminal and the output resistance at the O terminal is approximately given by

$$r_{out} = (r_{ds14} \,//\, r_{ds15}) = r_x \quad (11)$$

As a result, r_x greatly reduced and now has an insignificant effect on the closed loop gain of the CFOA The CFOA output resistance at terminal Z is simply obtained as

$$R_z = (r_{ds21} // r_{ds22}) \quad (12)$$

The CFOA dc open-loop gain can be given as

$$T(0) = \frac{R_z}{r_x + r_{out}} = \frac{R_z}{2r_{out}} \quad (13)$$

4. Simulation Results

The performance of the CFOA circuit was verified by performing PSpice simulations with supply voltages ±0.75 V using 0.35µm and 0.25µm TSMC CMOS technology parameters and transistor aspect ratios for both processes are given in Table 1. Fig. (4) and Fig. (5) shows the output voltage swing of the proposed CFOA when used to realize the amplifier with different gains. The input voltage was applied at the non-inverting input terminal Y, the output voltage obtained at the O terminal. The inverting input is terminated with 2 kΩ, while the Z terminal is terminated with resistance values of 2 kΩ, 4 kΩ. The total standby power dissipation is 0.503 mW and 0.41mW for 0.35µm and 0.25µm technology which is shown in Fig. (6). The magnitude response of the CFOA when it is used to realize a variable gain amplifier, where V_{in} is the AC-varying signal with 1 V peak to peak magnitude and the inverting terminal is terminated with a 1 kΩ and the Z terminal is terminated with a variable resistance with values of 0.75 kΩ, 1.5 kΩ, 3 kΩ, and 6 kΩ is shown in Fig. (7). The CFOA shows a constant bandwidth for different gains. The CFOA has a 3 dB bandwidth of 11.3 MHz and 100 MHz for 0.35µm and 0.25 µm. Fig.(8) gives the transient response for 50 MHz square wave input. It is noted that the output voltage follows the input indicating the slew rate of about 20 V/µs. Fig.(9) gives the Offset voltage at X terminal when Y and Z are grounded which is of 35mV and 20 mV for 0.35 µm and 0.25 µm Technologies respectively. Fig.(10) gives the Resistance at X terminal which is of 120 Ω and 60 Ω for 0.35 µm and 0.25 µm Technologies. Table 2 gives a performance comparison between the CFOA of 0.35µm CMOS Technology and 0.25µm CMOS Technology.

Table 1. Transistor Aspect Ratios of the CFOA

Transistor	**W (µm)**		**L (µm)**		**Aspect Ratio (W/L)**	
	0.35 µm	**0.25 µm**	**0.35 µm**	**0.25 µm**	**0.35 µm**	**0.25 µm**
M_1-M_4	14	25	0.7	0.25	20	100
M_5, M_6, M_{25}, M_{28}	1.4	5	1.4	0.25	1	20
M_{10}-M_{12}, M_{32}-M_{35}	140	150	1.4	0.75	100	200
M_7 - M_9	140	100	1.4	0.75	100	133
M_{18}, M_{38}	350	250	1.4	3	250	83
M_{16}, M_{17}, M_{36}, M_{37}	1.4	1	1.4	1	1	1
M_{19}, M_{15}, M_{20}, M_{22}, M_{39}	140	85	1.4	3.5	100	24
M_{23}, M_{24}, M_{26}, M_{27}	14	20	0.7	0.25	20	80
M_{13}	140	140	1.4	0.75	100	187
M_{29} - M_{31}	140	120	1.4	0.75	100	160
M_{14}, M_{21}	350	250	1.4	3.5	250	71

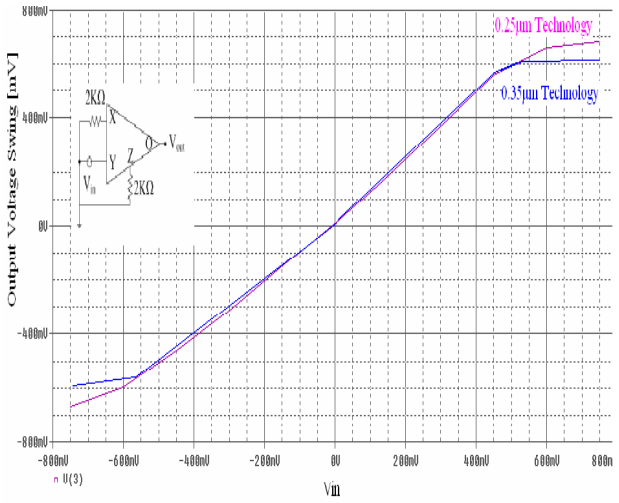


Figure (4). Output Voltage Swing

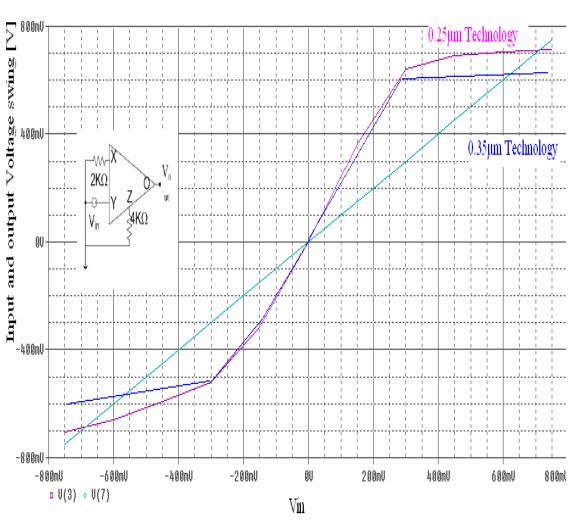


Figure (5). The Input and Output Voltage Swing for CFOA based Amplifier

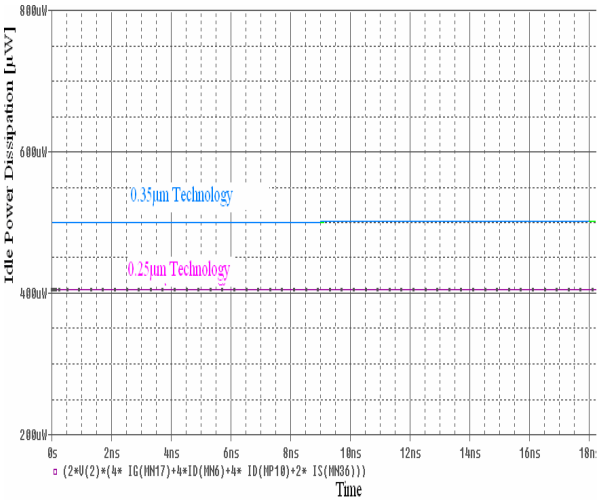


Figure (6). Total Power Dissipation

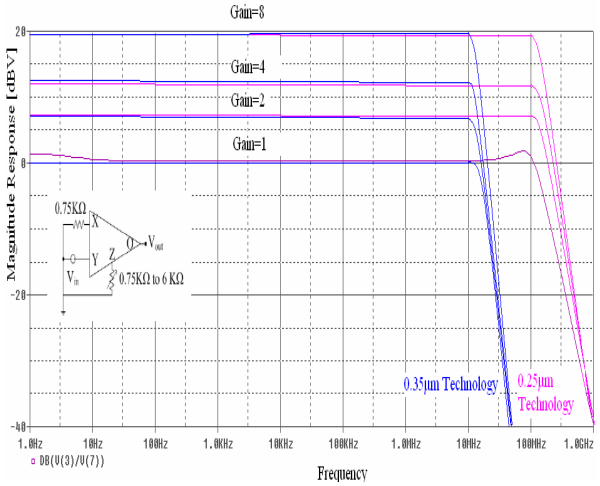
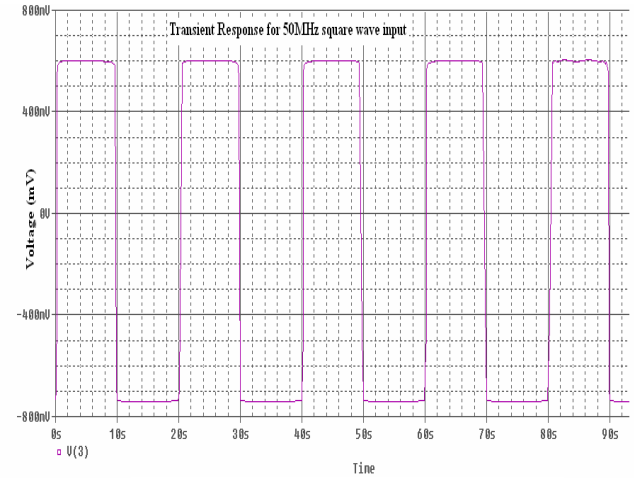


Figure (7). The magnitude response of the CFOA based variable gain amplifier



Time period (nano second)

Figure (8). Transient Response for 50 MHz square wave input

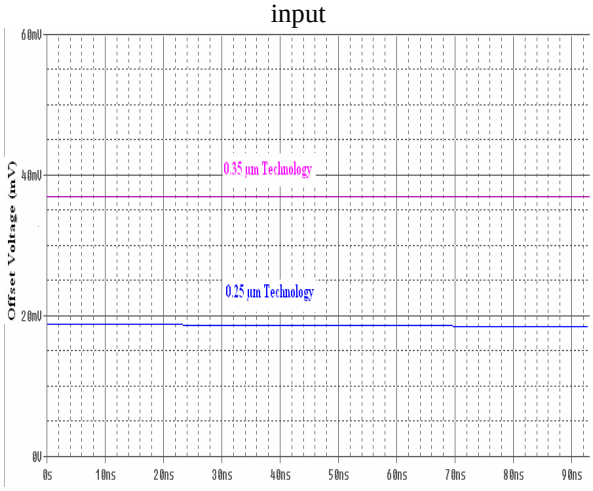


Figure (9). Offset Voltage at X terminal when Y and Z are grounded

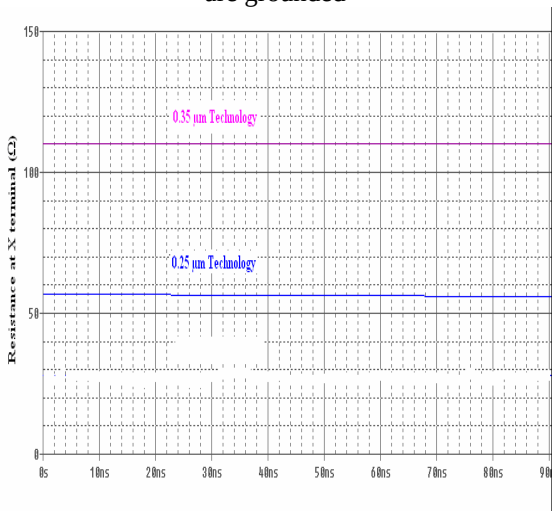


Figure (10). X terminal Resistance

Table 2. Performance Comparison

CFOA Parameter	**0.35 µm**	**0.25 µm**
Output Dynamic Range	± 0.6 V	± 0.7 V
Idle Power dissipation	0.503 mW	0.41 mW
CFOA Bandwidth	11.3 MHz	100 MHz
R_x	120 Ω	60 Ω
Offset Voltage at X terminal	< 40 mV	< 20 mV
Slew Rate	20 V/µs	20 V/µs

5. Conclusion

A CMOS CFOA was presented, analyzed and simulated which uses both 0.35µm and 0.25µm CMOS technology and the results are compared. The CFOA has improved the input stage open-loop bandwidth, Output Swing, Current Driving Capabilities with low power dissipation. The above CMOS CFOA can be used in Filters, Chaotic Nonlinear circuits, Integrators/Differentiatiors, Sinusoidal Oscillators, Analog Dividers which gives better performance when compared with traditional designs. A comparison has given for the parameters of CFOA between 0.35µm and 0.25µm CMOS technology . The new aspect ratios for 0.25µm CMOS technology has significantly improved the performance of CMOS CFOA over 0.35 µm

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