Configurable Analog Block based on CFOA and its Application

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Abstract: **-** A proposed configurable analog block (CAB) is presented, simulated and analyzed. The CAB consists of a CMOS current feedback operational amplifier (CFOA), presented by the authors, as the main active block, programmable four MOS nonlinearity cancellation cells, programmable capacitor array and MOSFET switches. Using the CABs, the universal field programmable analog array (FPAA) could be constructed, which can realize many signal-processing functions including variable gain amplifiers, filters. To show the reliability of the proposed CAB, a low-pass, band-pass, high-pass filter structure has been realized using the proposed CAB.

Key-Words: -CMOS, current feedback operational amplifier, configurable analog blocks, nonlinearity cancellation, filters.

1 Introduction

The role of analog integrated circuits in modem electronic systems remains important, even though digital circuits dominate the market for VLSI solutions. Analog systems have always played an essential role in interfacing digital electronics to the real world in applications such as analog signal processing and conditioning, industrial process, motion control and biomedical measurements [1]-[17]. An important advantage of digital integrated circuits has been their relative ease of design over analog circuits. In particular, since digital circuit design is amenable to automation, several CAD- compatible digital integrated circuit design methodologies have been developed, including design-for-testability, design optimization, rapid prototyping in Field-Programmable Gate Arrays (FPGAs) and, more recently, hardware synthesis from behavioral descriptions.

The drive towards shorter design cycles for analog integrated circuits has demanded the development of high performance analog circuits that are reconfigurable and suitable for CAD methodologies [1].

There have been some programmable analog circuits in the literature [1]-[11] as well as commercial chips (MPAA020 from Motorola, AN10E40 from Anadigm). However, general-purpose FPAAs suitable for high-frequency signal processing applications were rare [9].

Analog circuits based on the continuous time current feedback operational amplifier (CFOA) technique are suitable for high frequency applications [13]. Having a CFOA with four MOS nonlinearity cancellation cell [18-19] and programmable capacitor arrays, it is possible to build filters for wide frequency range.

The CFOA is a versatile building block for continuous time analog signal processing. The CFOA closed-loop bandwidth is independent of its close-loop gain (provided that the feedback resistance is kept constant and much higher than the CFOA inverting input resistance) [13] unlike VOA-based circuits, which are limited by a constant gain-bandwidth product. The current feedback operational amplifier (CFOA), is a four-port network with a describing matrix of the form,

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \\ V_O \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \\ I_O \end{bmatrix} \quad (1)$$

Several CMOS realizations for the CFOA have been reported in the literature [11]-[17].In this paper, a new CMOS configurable analog block (CAB) based on CFOA suitable for filtering applications has been presented. Using the proposed CAB, different filter structures have been configured to realize different responses.

The paper is organized as follows; in section 2 the proposed CAB architecture has been presented. In section 3, to show the reliability of the proposed CAB, a second order low-pass, band-pass, and high-pass filter has been realized using the proposed CAB. Finally, the conclusion is drawn in Section 4.

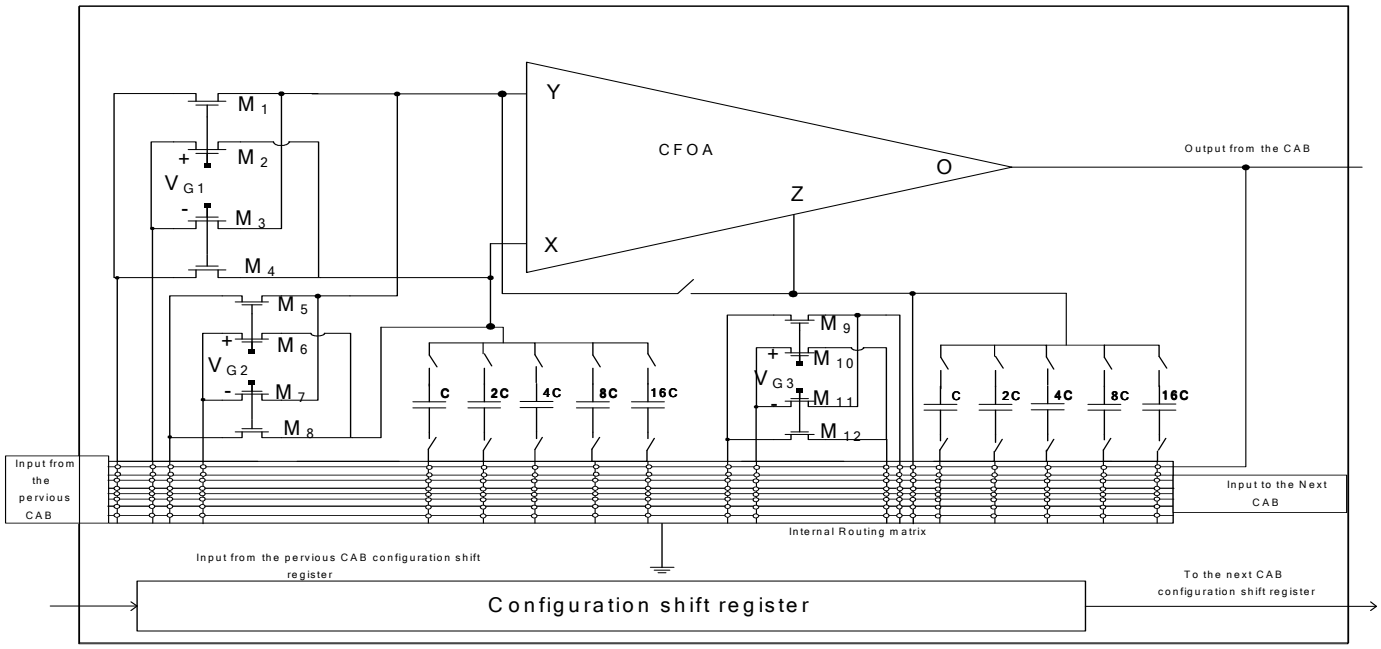


Fig.1 Proposed Configurable Analog Block (CAB).

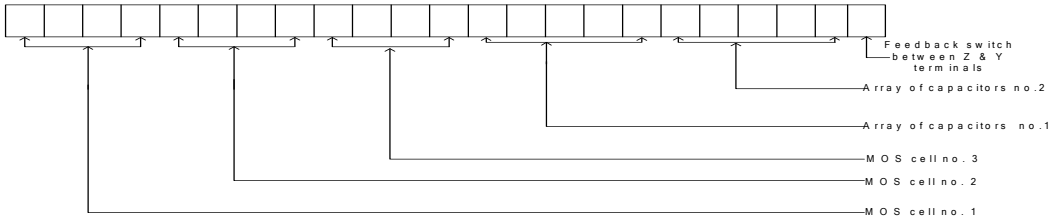


Fig. 2 The CAB Configuration Shift registers.

2 Proposed Configurable Analog Block (CAB)

The configurable blocks were designed to provide a sufficiently flexible, generic architecture while optimizing certain frequently used signal processing blocks.

Fig. 1 shows the proposed analog CAB, Each CAB could be viewed as a functional block consists of one CFOA as an active block, three programmable MOS nonlinearity cancellation cells, two programmable capacitor arrays, a configuration shift register and a set of MOSFET switches. This CAB could be used to realize different filters responses and also some analog functions like subtraction, addition, integration …etc.

The CAB interconnection matrix has been designed to give internal interconnections flexibility and guaranteed high frequency performance for the CAB. Each input for the CFOA block could be connected to the input directly or to another port from the CAB through internal switching matrix. Also, the output terminal could be connected as feedback to any input terminals in the CAB or outside the CAB. All the inputs could be connected to internal ground line through the switching matrix. All the connections could be configured using the configuration shift register. Fig. 2 gives the CAB configuration shift register consisting of 22 controlling bits. The first four bits are used to configure the Y terminal; the next four bits configure the X terminal, while the last array of resistors connected to the Z terminal is configured by the next four bits.

The two capacitor arrays are configured using ten bits (5 bits for each array). The configuration shift register is connected serially to the pervious and next CABs shift register. The first CAB in the upper left of the chip is connected to a serial programmable pin to load a bit stream of binary data serially to program the FPAA chip. Depending on the application the configuration switches could be programmed to provide the required functional block. In the next subsections the main components of the CAB will be illustrated.

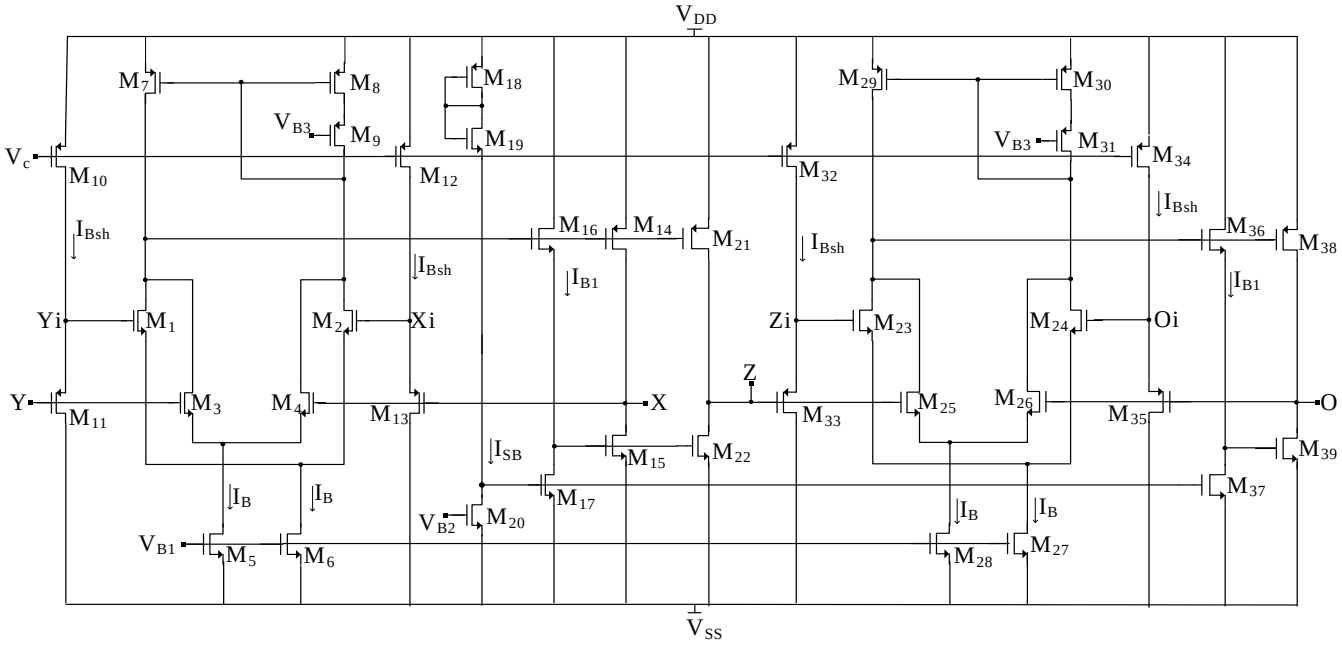


Fig. 3 The CMOS realization of the CFOA presented in [12].

2.1 CMOS Realization of the CFOA

The active block used in the proposed CAB is CFOA. The CMOS realization of the CFOA used here has been presented by the authors in [12], as shown in fig. 3, consists of two matched parallel connected n-differential pairs (M_1, M_2) and (M_3, M_4), two matched biasing current source transistors (M_5, M_6), cascoded current mirror formed of two matched transistors (M_7, M_8), and transistor (M_9), two pairs of matched source followers transistors (M_{10}, M_{11}) and (M_{12}, M_{13}). Transistors M_5 and M_6 carry equal bias currents (I_B) while transistors (M_{10}, M_{11}) and (M_{12}, M_{13}) produce a positive voltage shift for the input voltage applied on transistor M_{11} and $M_{13,}$ respectively. All transistors are operating in the saturation region; the control voltage V_C applied to transistors M_{10} and M_{12} gates controls the shifting value as follows,

$$V_{Yi} = V_Y + (V_{DD} - V_C) \quad (2)$$

$$V_{Xi} = V_X + (V_{DD} - V_C) \quad (3)$$

where V_{Yi} and V_{Xi} are the output voltage from the source followers, V_Y is the high input impedance voltage, and V_X is the low input impedance terminal. The circuit regions of operation could be explained as follows, for V_Y, V_X voltage close to the negative supply voltage V_{SS} ($V_{SS} \le V_Y, V_X < 2V_{Tn} + V_{SS}$), So the current source transistor M_5 and, hence, the differential pair M_3 and M_4 are cut-off. Then, the small and large signal behavior of the whole circuit result only from the contribution of the differential pair M_1 and M_2, biased with current source transistor M_6. In the middle range ($2V_{Tn} + V_{SS} \le V_Y, V_X < V_C + 2V_{Tn} - 2V_{DD}$), both input pairs ($M_1$-$M_2$) and ($M_3$-$M_4$) are active and the small and large signal behavior of the whole circuit result from the contribution of both differential pairs. Finally when V_Y, V_X very close to V_{DD} the positive supply voltage ($V_C + 2V_{Tn} - 2V_{DD} \le V_Y, V_X \le V_{DD}$), the current sources of the shifters M_{10} and M_{12} are cut-off. Therefore, the small- and large signal behavior of the whole circuit contribution result only from the differential pair M_3 and M_4 biased with current source transistor M_5. This ensures a rail-to rail operation. It is apparent, that this structure does not provide constant transconductance over the variations of the input voltages $V_{Y,}$ V_X. A feed forward section could be added to guarantee a constant transconductance over the variations of the input voltages $V_{Y,}$ V_X. However this is not a real drawback so long as the loop gain is sufficiently high. Indeed, variations of the open loop parameter were greatly reduced by feedback action. The structure of the CFOA input stage (voltage follower) requires that the X terminal must have low input impedance. So, a suitable buffer circuit should be used to fulfill this condition and to provide a rail-to-rail swing capability. Transistors (M_{14}-M_{20}) fulfill the required buffering action with a rail-to-rail swing capability, as shown in Fig. 3. The parameters of the CFOA are summarized in Table 1.

TABLE 1 PARAMTERS OF THE CFOA[12]

PARAMETERS	CFOA [12]
CMOS Technology (TSMC)	0.25 µm
Power supply (V_{DD}, V_{SS})	(1.5 V, -1.5 V)
Total Power dissipation	0.456 mW
Input Voltage Dynamic range	-0.65 V to 0.65 V
The X terminal offset voltage while Y and Z are grounded	< 20 mV
Current driving capability	-1mA, +1mA
R_X	< 40 Ω
The CFOA Bandwidth	120 MHz

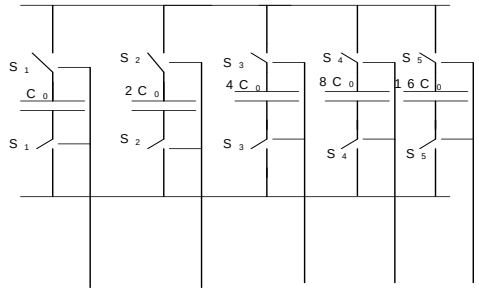


Fig. 4 Programmable Capacitor array.

2.2 Programmable Capacitor Array

The programmable capacitor array (PCA) is shown in Fig. 4. It consists of capacitors C_0 and switches S_n. The capacitor array built of an appropriate number of capacitors connected in parallel. Switches are realized using MOSFETs. When switch S_n, where n is the switch number ∈ {1, 5} is closed the equivalent capacitance to the array could be expressed as

$$C_{array} = \sum_{n=1}^{5} S_n C_n \quad (4)$$

where S_n is equal to 1 when switches are closed and equal to 0 when switches are open. The minimum equivalent capacitance equal to C_0 and the maximum is equal to $31C_0$.

The equivalent capacitance including the parasitic capacitance is obtains as follows, $C_{eq} = C_{array} + C_{par}$ where C_{par} is the parasitic capacitance of connections when all switches open and C_{array} is the equivalent capacitance of the array.

2.3The MOS Transistor Nonlinearities Cancellation cell

An NMOS transistor, with its gate connected to a control voltage V_G. The terminal voltages V_1 and V_2 are assumed to remain below V_G by at least the threshold voltage of the transistor V_T to allow operation in the non-saturation region. The current in the non-saturation region is given by [18-19]

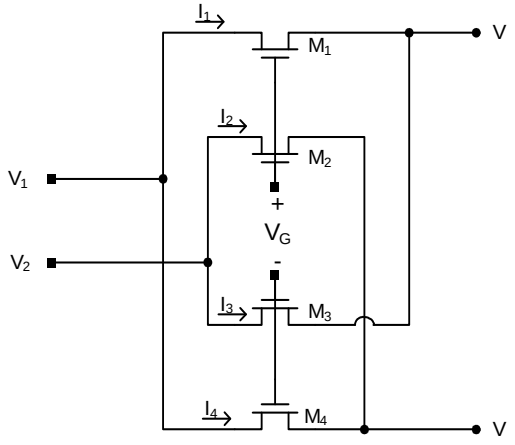


Fig. 5 Four MOS transistors circuit with full non-linearities' cancellation.

$$I = K(V_G - V_T)(V_1 - V_2) + a_1(V_1^2 - V_2^2) + a_2(V_1^3 - V_2^3) + \ldots \quad (5)$$

K is the transconductance parameter of the NMOS transistor and is given by

$$K = \mu_n C_{OX}\left(\frac{W}{L}\right)$$

where (W/L) is the transistor aspect ratio, C_{OX} is the gate oxide capacitance per unit area and μ_n is the electron mobility.

Many different techniques have been proposed for eliminating the effect of the nonlinearities [18-19]. The circuit shown in Fig. 5 [18-19] performs a complete cancellation of the nonlinearities and the linearized current is given by,

$$I = (I_1 + I_3) - (I_2 + I_4) = KV_G(V_1 - V_2) \quad \text{for } V_G - V_T \geq \max(V, V_1, V_2) \quad (6)$$

So, the transconductance of the circuit given in Fig. 5 could be controlled using the voltage V_G. Three cells have been used in the CAB and could be configured according to the applications needed.

3 Application

To show the reliability of the proposed CAB, it is used to realize a second-order low-pass, band-pass, and high-pass filter structure as shown in Fig. 6.
By direct analysis the following equation could be obtained as follows,

$$\frac{V_{HP}}{V_{in}} = \frac{s^2 \frac{K_3 V_{G3}}{K_6 V_{G6}}}{s^2 + s\frac{K_1 K_4 V_{G1} V_{G4}}{C_1 K_6 V_{G6}} + \frac{K_1 K_2 V_{G1} V_{G2}}{C_1 C_2}} \quad (7)$$

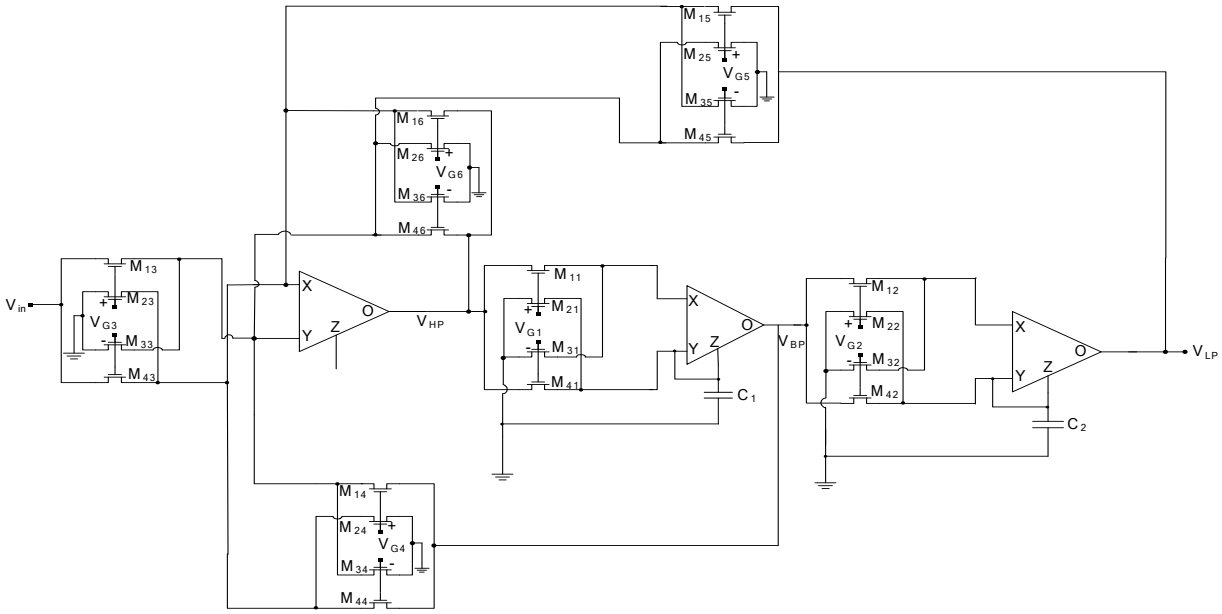


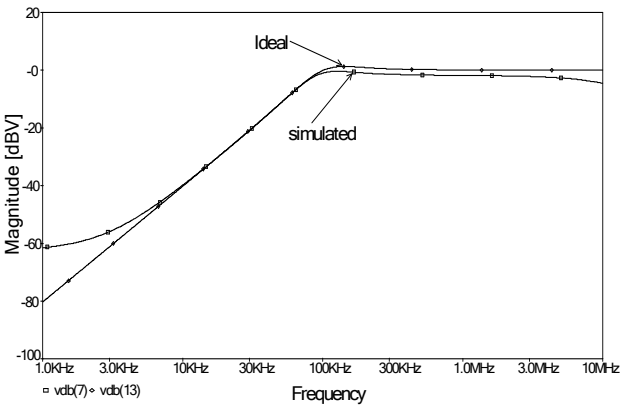
Fig. 6 Low-pass, bandpass and high pass filter structure using the proposed CAB.

$$\frac{V_{BP}}{V_{in}} = \frac{-s\dfrac{K_1K_3V_{G1}V_{G3}}{C_1K_6V_{G6}}}{s^2 + s\dfrac{K_1K_4V_{G1}V_{G4}}{C_1K_6V_{G6}} + \dfrac{K_1K_2V_{G1}V_{G2}}{C_1C_2}} \tag{8}$$

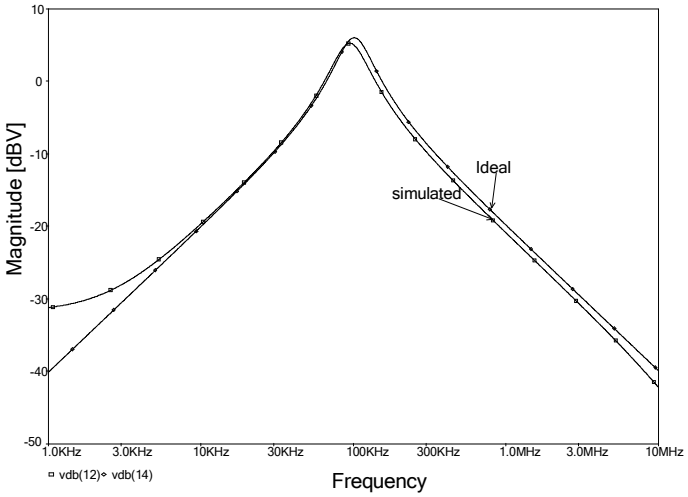
$$\frac{V_{LP}}{V_{in}} = \frac{\dfrac{K_1K_2K_3V_{G1}V_{G2}V_{G3}}{K_6V_{G6}}}{s^2 + s\dfrac{K_1K_4V_{G1}V_{G4}}{C_1K_6V_{G6}} + \dfrac{K_1K_2V_{G1}V_{G2}}{C_1C_2}} \tag{9}$$

Taking all K to be equal, the ωo, Q and gain H are given by:

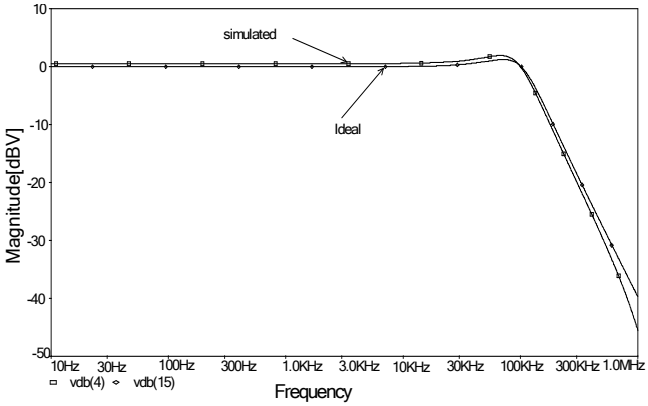
$$\omega_o = K\sqrt{\frac{V_{G1}.V_{G2}}{C_1C_2}}, Q = \frac{V_{G6}}{V_{G4}}\sqrt{\frac{C_1V_{G2}}{C_2V_{G1}}}, H = \frac{V_{G3}}{V_{G4}} \tag{10}$$



(a)



(b)



(c)

Fig.7 output voltage magnitude responses (a) high pass, (b) bandpass, (c) low pass.

The circuit shown in Fig. 6 has been simulated using PSpice and 0.25 μm CMOS technology model from MOSIS taking, Vg1=Vg2=Vg3=Vg5 =Vg6= 2.748V, Vg4=1.374V, K_n=251.479μA/V, W=2μm and L=4μm for all MOS transistors in fig.6 and C1=C2=0.545nF, f_0=100KHz and Q=2. The simulated responses are given in Figs. 7(a-c) with the ideal response. From the pervious filter realization, the proposed CAB could be programmed to realize different analog signal processing functions using special configurations bits. Also, fine tuning for f_o, Q, H could be controlled through voltagesV_{G1} to $V_{G6.}$

4 Conclusion

A new design for configurable analog block suitable for high frequency applications is introduced. The proposed CAB consists of a current feedback operational amplifier (CFOA) as a main active block, four MOS cell, programmable capacitor arrays and MOSFET switches. Using the proposed CAB, a realization of low-pass, band-pass, and high-pass filter has been presented and simulated.

References:

[1] H. Kutuk and S. Kang, "A field-programmable analog array (FPAA) using switched-capacitor techniques," IEEE ISCAS, 1996, pp. 41-44.

[2] E. Lee and P. G. Gulak, "Field-programmable analog array based on MOSFET transconductors," Electronics Letters, vol. 28, no. 1, pp. 28-29, Jan. 1992.

[3] C. Premont, R. Grisel, N. Abouchi, and J. Chante, "Current conveyor based field programmable analog array," Midwest Symposium on Circuits and Systems, pp. 18-21, Aug. 1996, Ames, Iowa.

[4] S.H. K. Embabi, X. Quan, N. Oki, A. Manjrekar, and E. Sanchez-Sinencio, "A Field programmable analog signal processing array," Midwest Symposium on Circuits and Systems, Aug. 1996, Ames, Iowa.

[5] F. J. Kub, K. K. Moon, I. A. Mack, and F. M. Long, "Programmable analog vector-matrix multipliers," IEEE Journal of Solid State Circuits, vol. 25, no. 1, pp. 207-214, Feb. 1990.

[6] S. Satyanarayana, Y. P. Tsividis, and H. P. Graf, "A Reconfigurable VLSI Neural Network," IEEE Journal of Solid-State Circuits, vol. 27, no. 1, pp. 67-81, Jan. 1992.

[7] E. Lee and P. G. Gulak, "A transconductor-based field programmable analog array," ISSCC Digest of Technical papers, pp. 198-199, Feb. 1995.

[8] E. Lee and G. Gulak, "A CMOS field-programmable analog array," IEEE Journal of Solid-State Circuits, vol. 26, no. 12, pp. 1860-1867, Dec. 1991.

[9] T. S. Hall, C. M. Twigg, J. D. Gray, P. Hasler, and D. V. Andreson, "Large scale field programmable analog arrays for analog signal processing," IEEE Trans. on Circuits and Systems-I, vol. 52, no.11, pp. 2298-2307, Nov. 2005.

[10] R. C. Chang, B. J. Sheu, J. Choi, and D. C-H. Chen, "Programmable weight building blocks for analog VLSI neural network Processors," Analog Integrated Circuits and Signal Process., vol. 9, no. 3, pp. 215-230, Apr. 1996.

[11] B. Pankiewicz, M. Wojcikowski, S. Szcepanski, and Y. Sun, "A field programmable analog array for CMOS continuous time OTA-C filter applications," IEEE Journal of Solid-State Circuits, vol. 37, no. 2, pp. 125-136, Feb. 2002.

[12] H. Madian, S. A. Mahmoud, and A. M. Soliman, "New 1.5V CMOS current feedback operational amplifier," ETRI journal, vol.29, no.2, Apr. 2007.

[13] Toumazu and J. Mahattanakul, “A theoretical study of the stability of high-frequency current feedback op-amp integrators,” IEEE Trans. Circuit Syst. I, vol. 43, pp. 2-12, 1996.

[14] S. A. Mahmoud and A. M. Soliman, “Novel MOS-C balanced-input balanced-output filter using the current feedback operational amplifier,” Int. J. Electron., vol. 84, pp. 479-485, 1998.

[15] M. Soliman, “Applications of the current feedback operational amplifier,” Analog Integrated Circuits Signal Processing, vol. 11, pp. 265-302, 1996.

[16] R. Mita, G. Palumbo, and S. Pennisi, ”Low-voltage high-drive CMOS current feedback op-amp,” IEEE Trans. Circuit Syst.-II, vol. 52, pp. 317-321, 2005.

[17] E. Bruun, “A dual current feedback op amp in CMOS current Conveyor,” Electron. Lett., vol. 34, pp. 2368-2369, 1998.

[18] Z. Czarnul, Modification of Banu- Tsividis, Continuous-time integrator structure, IEEE Transactions on Circuits and Systems, vol.33, 714-716, 1968.

[19] Z. Czarnul, Novel MOS resistive circuit for synthesis of fully integrated continuous-time filters, IEEE Transactions on Circuits and Systems, vol.33, 718-721, 1986.